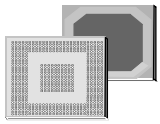
SPEAr1340

Dual-core Cortex A9 HMI embedded MPU

Datasheet – preliminary data

Features

- CPU subsystem:
  - 2x ARM Cortex A9 cores, up to 600 MHz
  - 32+32 KB L1 caches per core, with parity check
  - Shared 512 KB L2 cache
  - Accelerator coherence port (ACP)
- Network-on-chip bus matrix, up to 166 MHz
- 32 KB Boot ROM, 32+4 KB Static RAMs
- Memory interfaces:
  - DDR controller (DDR3-1066, DDR2-1066 @533MHz), 16-/32-bit, up to 2 GB address space
  - Serial NOR Flash controller
  - Parallel NAND Flash/NOR Flash/SRAM controller
- Connectivity:
  - 2 x USB 2.0 Host ports (integrated PHY)
  - 1 x USB 2.0 OTG port (integrated PHY)
  - 1 x Giga/Fast Ethernet port (external GMII/ RGMII/MII/RMII PHY)
  - 1 x PCIe 2.0 RC/EP port (integrated PHY)
  - 1 x 3Gb/s Serial ATA Host port (integrated PHY)
  - 1 x memory card interface: SD/SDIO/MMC, CF/CF+, xD
  - 2 x UART ports, with IrDA option
  - 2 x I2C bus controllers, master/slave
  - 1 x synchronous serial port, SPI/Microwire/TI protocols, master/slave
  - 2 x consumer electronic control (HDMI CEC) ports
  - 10-bit ADC: 8 ch. 1 Msps, with autoscan
  - Programmable bidirectional GPIO signals with interrupt capability
- HMI support:
  - LCD display controller, incl.support for Full HD, 1920 x 1080, 60 Hz, 24 bpp



PBGA (23 x 23 mm)

  - High-perf. 2D/3D GPU, up to 1080p
  - Hardware video decoder: multistandard up to 1080p, JPEG
  - Hardware video encoder: H.264 up to 1080p, JPEG
  - Video input parallel port, with alternate configuration for 4 x camera interfaces
  - Digital audio ports: up to 7.1 multichannel surround, I2S (8 in, 8 out) and S/PDIF
  - 6 x 6 keyboard controller
  - Resistive touchscreen interface
- Security:
  - C3 cryptographic accelerator
  - Secure boot support
  - JTAG disable option
- Miscellaneous functions:
  - Energy saving: power islands, clock gating, dynamic frequency scaling
  - 2 x DMA controllers (total 16 channels)
  - 11 x general purpose timers, 2 x watchdogs, 1 x real-time clock
  - 4 x PWM generators
  - Embedded sensor for junction temperature monitoring
  - OTP (one-time programmable) bits
  - Debug and trace interfaces: JTAG/PTM

Table 1. Device summary

Order code	Temp. range, °C	Package	Packing
SPEAr1340-2	-40 to 85	PBGA (23x23mm, pitch 0.8mm)	Tray

Contents

1 Description

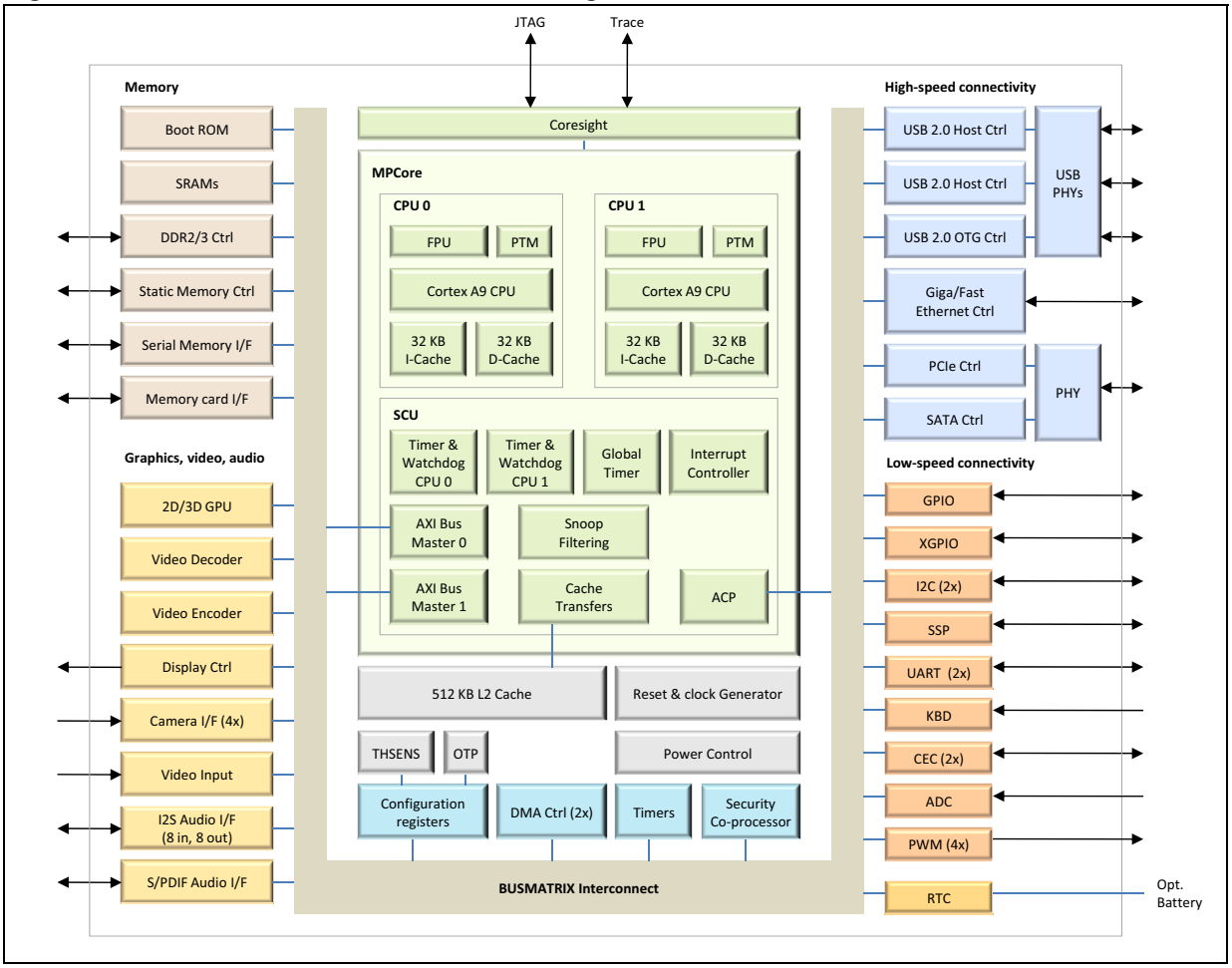
The SPEAr1340 device is a system-on-chip belonging to the SPEAr® (Structured Processor Enhanced Architecture) family of embedded microprocessors. The product is suitable for consumer and professional applications where an advanced human machine interface (HMI) combined with high performance are required, such as low-cost tablets, thin clients, media phones and industrial/printer smart panels.

The device is hardware-compliant to the support of both real-time (RTOS) and high-level (HLOS) operating systems, such as Android, Linux and Windows Embedded Compact 7.

The architecture of SPEAr1340 is based on several internal components, communicating through a multilayer interconnection matrix (BUSMATRIX). This switching structure enables different data flows to be carried out concurrently, improving the overall platform efficiency.

In particular, high-performance master agents are directly interconnected with the DDR memory controller in order to reduce access latency. The overall memory bandwidth assigned to each master port can be programmed and optimized through an internal weighted round-robin (WRR) arbitration scheme.

Figure 1. SPEAr1340 architectural block diagram



2 Device functions

2.1 CPU subsystem

The CPU subsystem is based on the ARM Cortex A9 processor, and has a dual-core configuration.

Main features:

Each core has the following features:

- ARM v7 CPU at 600 MHz
- 32 KB of L1 instruction CACHE with parity check
- 32 KB of L1 data CACHE with parity check
- Embedded FPU for single and double data precision scalar floating-point operations
- Memory management unit (MMU)
- ARM, Thumb2 and Thumb2-EE instruction set support
- Program Trace Macrocell (PTM) and CoreSight© component for software debug
- 32-bit timer with 8-bit prescaler
- Internal watchdog (working also as timer)

The dual core configuration is completed by a common set of components:

- Snoop control unit (SCU) to manage inter-process communication, cache-to-cache and system memory transfer, cache coherency
- Generic interrupt control (GIC) unit configured to support 128 independent interrupt sources with software configurable priority and routing between the two cores
- 64-bit global timer with 8-bit prescaler
- Accelerator coherence port (ACP)
- Parity support to detect runtime failures for other internal memories
- 512 KB of unified 8-way set associative L2 cache with support for ECC
- L2 Cache controller based on PL310 IP released by ARM
- Dual asynchronous 64-bit AMBA 3 AXI interface with possible filtering on the second one to use a single port for DDR memory access
- JTAG interface and Trace port: debug and trace can be inhibited through OTP

2.2 Multilayer interconnect matrix (BUSMATRIX)

The multilayer interconnect matrix is the connectivity infrastructure that enables data exchange between the various blocks of the device. The BUSMATRIX supports parallel communications between master and slave components, and ensures the maximum level of system throughput.

Main features:

- Hierarchical structure to meet the requirements of different system blocks and peripherals:
  - high performance low latency
  - high performance medium latency
  - medium performance medium/long latency
  - slow peripherals and configurations
- Power awareness through the power down request/acknowledgement of the power management module
- Single interrupt for outband signaling

2.3 Internal memories

SPEAr1340 integrates two embedded memories:

- 32 KB Boot ROM (BootROM)
- Static RAM areas (SRAM)

2.3.1 BootROM

BootROM refers to the on-chip 32 KB ROM as well as the booting firmware pre-stored in such memory. The supported booting devices are:

- Serial NOR Flash
- Parallel NOR Flash
- NAND Flash
- USB OTG
- UART
- SD/MMC

The BootROM firmware selects the booting device after reset by reading the status of the STRAP[3:0] pins.

2.3.2 Static RAMs (SRAM)

A part of these memory areas is used during the bootstrap phase by BootROM firmware. After booting, all SRAM areas are fully available for general purpose applications.

Main features:

- 32 KB of system RAM (SYSRAM0, single port)
  When all power islands are switched off, SYSRAM0 loses its data content.
- 4 KB of Always-on RAM (SYSRAM1, single port)
  When all power islands are switched off, SYSRAM1 maintains its data content.

2.4 Multiport DDR controller (MPMC)

MPMC is a high-performance multichannel memory controller able to support DDR2 and DDR3 memory devices. The multiport architecture ensures that memory is shared efficiently among different high-bandwidth client modules.

Main features:

- Supports both DDR3 and DDR2 devices; wide range of memory device cuts supported up to 2 GB (*Note: 1*)
- Two chip selects supported
- Programmable memory data path size of full memory 32-bit data width or half memory 16-bit data width
- Clock frequencies from 100 MHz to 533 MHz supported
- 6 AXI interfaces with a data interface width of 64 bits. Each port is configured with a thread ID of 4 bits
- Exclusive and locked accesses support
- Weighted round-robin arbitration scheme support to ensure high memory bandwidth utilization
- DRAM command processing
- Register port with an AHB interface with a data interface width of 32 bits
- A programmable register interface to control memory device parameters and protocols including auto pre-charge
- Full initialization of memory on memory controller reset
- Automatically maps user addresses to the DRAM memory in a contiguous block addressing starts at user address 0 and ends at the highest available address according to the size and number of DRAM devices present
- Fully pipelined command, read and write data interfaces to the memory controller
- Advanced bank look-ahead features for high memory throughput

Note: 1 When the 2GB address space is enabled, the ACP function is not available.

2.5 Serial NOR Flash controller (SMI)

The serial NOR Flash controller integrated in SPEAr1340 acts as an AHB slave interface (32-, 16- or 8-bit) to SPI-compatible off-chip memories. SMI allows the CPU to use these serial memories either as data storage or for code execution.

Main features:

- Supports a group of SPI-compatible Flash and EEPROM devices
- Acts always as an SPI master and up to 2 SPI slave memory devices are supported (through as many chip select signals), with up to 16 MB address space each.
- The SMI clock signal (*smi_clk_o*) is generated by SMI (and inputs to all slaves) using a clock provided by the AHB bus
- *smi_clk_o* can be controlled by a programmable 7-bit prescaler allowing 127 different clock frequencies.

2.6 Flexible static memory controller (FSMC)

The flexible static memory controller enables to interface external parallel Flash memories as well as static RAMs.

Main features:

- Support for parallel NAND Flash:
  - 8-bit or 16-bit data bus
  - 2 chip select signals
  - no limitation on NAND capacity (number of pages)
  - hardware ECC (error correction code) support, correcting up to 8 errors per page (512 bytes wide)
  - support for SLC (single-level cell) and MLC (multi-level cell) Flash devices, as far as compatible with available ECC features
- Support for parallel NOR Flash:
  - 8-bit or 16-bit data bus
  - 26-bit address bus
  - 2 chip select (CS) signals
  - Maximum capacity is 64 MB for each CS, hence up to 128 MB with 2 external Flash devices
- Support for asynchronous static RAMs (SRAMs):
  - 8-bit or 16-bit data bus
  - 26-bit address bus
  - 2 chip select (CS) signals
  - Maximum capacity is 64 MB for each CS, hence up to 128 MB with 2 external SRAM devices
- Support for multiplexed NOR and SRAM
- Write FIFO: 16 words depth, each word is 32 bits wide
- Independent read/write timings and protocol, allowing matching the widest variety of memories and timings
- Wait signal for timings handshake

2.7 USB 2.0 Host controllers (UHC)

The SPEAr1340 device integrates 2 USB Host interfaces. Each interface provides a high-speed Host controller (EHCI standard) and a full-speed/low-speed controller (OHCI standard). The UHC has 2 physical ports (2 separate instances) that are fully compliant with the Universal Serial Bus specification (version 2.0), and provides an interface to the industry-standard AHB bus.

Main features:

- A PHY interface implementing a USB 2.0 transceiver macro-cell interface plus (UTMI+) fully compliant with UTMI+ specification (revision 1.0), to execute serialization and de-serialization of transmissions over the USB line
- Either 30 MHz clock for 16-bit interface or 60 MHz for 8-bit interface supported by the UTMI + PHY interface
- A USB 2.0 host controller (UHC) connected to the AHB bus that generates the commands for the UTMI+PHY
- Complies with both the enhanced host controller interface (EHCI) specification (version 1.0) and the open host controller interface (OHCI) specification (version 1.0a)
- The UHC supports the 480 Mbps high-speed (HS) for USB 2.0 through an embedded EHCI Host Controller, as well as the 12 Mbps full-speed (FS) and the 1.5 Mbps low-speed (LS) for USB 1.1 through one integrated OHCI Host controller
- All clock synchronization is handled within the UHC
- An AHB slave for each controller (1 EHCI and 1 OHCI), acting as programming interface to access to control and status registers
- An AHB master for each controller (1 EHCI and 1 OHCI) for data transfer to system memory, supporting 8-, 16-, and 32-bit wide data transactions on the AHB bus
- 32-bit AHB bus addressing

2.8 USB 2.0 OTG port (UOC)

Main features:

- Complies with the On-The-Go supplement to the USB 2.0 specification (revision 1.3)
- Supports the Session Request Protocol (SRP)
- Supports the Host Negotiation Protocol (HNP)
- A PHY interface implementing the USB 2.0 transceiver macrocell interface (UTMI+ specification, revision 1.0 (Level 3)) to execute serialization and de-serialization of transmissions over the USB line
- Unidirectional and bidirectional 16-bit UTMI data bus interfaces
- Support for the following speeds:
  - High speed (HS): 480 Mbps
  - Full speed (FS): 12 Mbps
  - Low speed (LS): 1.5 Mbps (only in Host mode)
- Both of the DMA and slave-only modes are supported

2.9 Giga/Fast Ethernet port (GMAC)

The GMAC IP provides the capability to transmit and receive data over Ethernet.

Main features:

- Supports 10/100/1000 Mbps data transfer rates with the following PHY interfaces:
  - IEEE 802.3-compliant GMII/MII interface (default) to communicate with an external Gigabit/Fast Ethernet PHY
  - RGMII interface to communicate with an external gigabit PHY
  - RMII interface (specification version 1.2 from RMII consortium) to communicate with an external Fast Ethernet PHY (for 10/100 Mbps operations only)
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion
  - Optional forwarding of received pause control frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using back-pressure support
  - Frame bursting and frame extension in 1000 Mbps half-duplex operation
- Automatic CRC and pad generation controllable on a per-frame basis
- Provides options for automatic pad/CRC stripping on receive frames
- Supports a variety of flexible address filtering modes, such as:
  - Up to 31 48-bit SA address comparison check with masks for each byte
  - 64-bit hash filter for multicast and unicast (DA) addresses
  - Option to pass all multicast addressed frames
  - Promiscuous mode support to pass all frames without any filtering for network monitoring
  - Passes all incoming packets (per filter) with a status report
- Programmable frame length to support standard or jumbo Ethernet frames with up to 16 KB of size
- Programmable interframe gap (IFG) (40-96 bit times in steps of 8)
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Self-managed DMA transfers with an internal DMA block
- Separate transmission, reception, and control interfaces to the application
  - The host CPU uses a 32-bit AHB (AMBA 2.0) slave interface to access the GMAC subsystem control and status registers (CSRs)
  - The GMAC transfers data to system memory through a 32-bit AXI (AMBA 3.0) master interface
- Support for network statistics with RMON/MIB counters (RFC2819/RFC2665)
- A module for detection of LAN remote wake-up frames and AMD magic packet frames: power management module (PMT)
- A receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- An enhanced receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)

- An enhanced module to calculate and insert IPv4 header checksum and TCP, UDP, or ICMP checksum in frames transmitted in store-and-forward mode.
- A module to support Ethernet frame time stamping as described in IEEE 1588- 2002 and IEEE 1588-2008 (standard for precision networked clock synchronization). Sixty-four-bit time stamps are given in the transmit or receive status of each frame.
- MDIO master interface for PHY device configuration and management: station management agent (SMA), MDIO module
- Supports the standard IEEE P802.3az, version D2.0 for energy efficient Ethernet; allows physical layers to operate in the low-power idle (LPI) mode

The **MAC transaction level (MTL) block** consists of two sets of FIFOs: a transmit FIFO with programmable threshold capability, and a receive FIFO with a programmable threshold (default of 64 bytes). The MTL block has the following features:

- 32-bit transaction layer block that provides a bridge between the application and the GMAC
- Single-channel transmit and receive engines
- Synchronization for all clocks in the design (transmit, receive, and system clocks)
- Optimization for packet-oriented transfers with frame delimiters
- Four separate ports for system-side and GMAC side transmission and reception
- FIFO instantiation outside the top-level module to facilitate memory testing/instantiation
- 4 KB receive FIFO size on reception
- Supports receive status vectors insertion into the receive FIFO after the EOF transfer. This enables multiple-frame storage in the receive FIFO without requiring another FIFO to store those frames
- Configurable receive FIFO threshold (default fixed at 64 bytes) in cut-through or threshold mode
- Provides an option to filter all error frames on reception and not forward them to the application in store-and-forward mode.
- Provides an option to forward under-sized good frames
- Supports statistics by generating pulses for frames dropped or corrupted (due to overflow) in the receive FIFO
- 2 KB FIFO size on transmission
- Store and forward mechanism for transmission to the GMAC
- Threshold control for transmit buffer management
- Automatic retransmission of collision frames for transmission
- Discards frames on late collision, excessive collisions, excessive deferral, and under-run conditions
- Software control to flush TX FIFO

The **DMA block** exchanges data between the MTL block and host memory. The host can use a set of registers (DMA CSR) to control the DMA operations. The DMA block supports the following features:

- 32-bit data transfers
- Single-channel transmit and receive engines
- Fully synchronous design operating on a single system clock (except for CSR module, when a separate CSR clock is configured)
- Optimization for packet-oriented DMA transfers with frame delimiters

- Byte-aligned addressing for data buffer support
- Dual-buffer (ring) or linked-list (chained) descriptor chaining
- Descriptor architecture that allows large blocks of data transfer with minimum CPU intervention
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst size for transmit and receive DMA engines for optimal host bus utilization
- Programmable interrupt options for different operational conditions
- Complete per-frame transmit/receive interrupt control
- Round-robin or fixed-priority arbitration between receive and transmit engines
- Start/stop modes
- Separate ports for host CSR access and host data interface

The **GMAC audio video (AV)** enables transmission of time-sensitive traffic over bridged local area networks (LANs). The GMAC AV has the following features:

- Compliant to IEEE 802.1-AS standard, version D6.0: specifies the protocol and procedures used to ensure that the synchronization requirements are met for time-sensitive applications
- Compliant to IEEE 802.1-Qav standard, version D6.0: allows the bridges to provide time-sensitive and loss-sensitive real-time audio video data transmission (AV traffic). It specifies the priority regeneration and controlled bandwidth queue draining algorithms that are used in bridges and AV traffic sources
- Supports one additional channel (channel 1) on the transmit and receive paths for AV traffic in 100 Mbps and 1000 Mbps modes. The channel 0 is available by default and carries the legacy best-effort Ethernet traffic on the transmit side.
- Supports IEEE 802.1-Qav specified credit-based shaper (CBS) algorithm for the additional transmit channels
- Provides separate DMA, TxFIFO, and RxFIFO MTL for the additional channel (to avoid “head of line blocking” issues); the system-side interface remains the same.

The GMAC has the following additional features for monitoring, testing, and debugging:

- Supports internal loopback on the GMII/MII for debugging
- Provides DMA states (Tx and Rx) as status bits
- Provides debug status register that gives status of FSMs in transmit and receive data-paths and FIFO fill-levels
- Application abort status bits
- MMC (RMON) module in the GMAC core
- Current Tx/Rx buffer pointer as status registers
- Current Tx/Rx descriptor pointer as status registers
- Statistical counters that help in calculating the bandwidth served by each transmit channel when AV support is enabled

2.10 PCI Express controller (PCIe)

The PCI Express core incorporates a dual-mode (DM) core which can implement a PCIe interface for a PCIe Root Complex (RC) or Endpoint (EP). The dual-mode core can operate in EP or RC port modes, depending on value written in a register during PCIe configuration.

PCIe is compliant with the PCI Express Base 2.0 specification, but it is also compliant with the PCIe 1.1 specification.

The core features a proprietary user-configurable and high-performance application interface for generating and receiving PCIe traffic. It is available with standard AMBA 3 AXI interfaces.

Typical applications for a PCI Express device built with the DM core include:

- Motherboard components for desktop and mobile computers
- Graphics devices
- Add-in cards for desktop and mobile computers
- Components and add-in cards in server applications
- Embedded applications
- Data communications equipment
- Telecommunications equipment
- Storage devices
- Wireless devices
- Other applications

The DM core in EP mode supports PCI Express Legacy Endpoint devices. However, the application must ensure that the device obeys the Legacy Endpoint device rules defined in the PCI Express Base 2.0 specification.

Note: The core is not intended for use in a root complex integrated endpoint.

Main features (common to both EP and RC mode of the DM cores):

- Support for all non-optional features and some optional features defined in the PCI Express Base 2.0 specification.
- Ultra low transmit and receive latency
- Support a max payload size of 256 bytes
- 4 KB maximum request size
- Very high accessible bandwidth
- Support for both Gen1 (at 125 MHz) and Gen2 (at 250 MHz) operation
- 2.5 Gbps (Gen1) or 5.0 Gbps (gen2) Lane (x1)
- Automatic lane reversal as specified in the PCI Express 2.0 specification (transmit and receive)
- Polarity inversion on receive
- Multiple virtual channels (VCs) (maximum of 2)
- Multiple traffic classes (TCs)
- ECRC generation and checking
- PCI Express beacon and wake-up mechanism

- PCI power management
- PCI Express active state power management (ASPM)
- PCI Express advanced error reporting
- Vital product data (VPD)
- PCIe messages for both transmit and receive.
- External priority arbitration (in addition to the internally implemented transmit arbitration)
- Expansion ROM support

Additional features specific to RC mode

- Type 1 configuration space
- Application-initiated Lane reversal for situations where the core does not detect Lane 0 (for example, an x4 core connected to an x8 device that has its Lanes reversed)

Additional features specific to EP mode

- Completion time-out ranges
- Type 0 configuration space
- MSI interrupt capability

2.11 Serial ATA controller (SATA)

The SATA AHCI Core implements the serial advanced technology attachment (SATA) storage interface for physical storage devices.

Main features:

- SATA 3.0 Gb/s Gen II
- eSATA (external analog logic also needs to support eSATA)
- Compliant with the following specifications:
  - Serial ATA 3.0 (except FIS-based switching)
  - AHCI Revision 1.3 (except FIS-based switching)
  - AMBA 3 AXI interfaces
- User-defined PHY status and control ports
- RX data buffer for recovered clock systems
- Data alignment circuitry when RX data buffer is also included
- OOB signaling detection and generation
- 8b/10b encoding/decoding
- Asynchronous signal recovery, including retry polling
- Digital support of device hot-plugging
- Power management features including automatic partial-to-slumber transition
- BIST loopback modes
- Single SATA device
- Internal DMA engine per port
- Hardware-assisted native command queuing for up to 32 entries

- Port Multiplier with command-based switching
- Disabling RX and TX Data clocks during power down modes
- Integrated SATA link layer and transport layer logic
- Supports PIO, first party and legacy DMA modes
- Supports legacy command queuing
- Supports ATA and ATAPI master-only emulation mode (for instance, register and command compatible with these standards)
- Power-down mode
- Data scrambling
- CRC computation
- Automatic data flow control
- Far end loop-back re-timed

2.12 SATA/PCIe physical interface (MiPHY)

The MiPHY macrocell implements the lower (physical) layer protocols providing data transmission and reception over a dual differential pair cable. The TX (transmit) and RX (receive) serial channels operate plesiochronously (NRZ). The macrocell can be used in Host or Device applications.

Main features:

- Serial transceiver (PHYsical layer) serializer and deserializer
- Direct support for 1.5/ 3.0 and 1.25/ 2.5/ 5.0 Gbit/s bit rates
- 20-bit parallel interface
- Comma detect to provide word alignment of incoming serial stream
- SSC modulation
- Integrated impedance adaptation to transmission line characteristics
- Out-of-band (OOB) signaling
- Supported 1.2 V and 2.5 V power supply
- High-performance PLL (input reference 100 MHz for PCIe and 100 or 25 MHz for SATA)
- Programmable TX buffer pre-emphasis, slew-rate and amplitude
- Dedicated TX buffer regulator for:
  - Transmit buffer noise immunity
  - Buffer level stability

2.13 Memory card interfaces (MCIF)

MCIF is a hardware IP that interfaces with the most common memory cards on the market:

- SD/SDIO 2.0
- SDHC
- CF/CF+ Rev 4.1
- MMC 4.2/4.3
- xD

The device interface multiplexes different memory cards on the same IOs; only one memory card is accessible at a given time. At the board level, discrete elements are required to handle host-swap management.

Main features:

SD/SDIO/MMC controller

- Compliant with:
  - SD Host controller standard specification version 2.0
  - SDIO card specification version 2.0
  - SD memory card specification draft version 2.0
  - SD memory card security specification version 1.01
  - MMC specification version 3.31, 4.2 and 4.3
  - AMBA specification AHB (version 2.0)
- Data transfer with the system core through:
  - PIO mode on the Host AHB slave interface
  - DMA mode on the Host AHB master interface
- Host clock rate variable from 0 to 50 MHz
- Maximum data rate achievable:
  - 200 Mbps (sd4 bit mode)
  - 400 Mbps (mmc8 bit mode)
- Data transfer:
  - SD mode: 1 bit, 4 bit, and SPI mode
  - MMC mode: 1 bit, 4 bit, 8 bit, and SPI mode
- Cyclic redundancy check for commands (CRC7) and for data integrity (CRC16)
- Variable length data transfer
- Read wait control and suspend/resume operations supported
- Works with IO cards, read-only cards and read/write cards
- Supports MMC Plus and MMC Mobile
- Error correction code support for MMC 4.3 cards
- Card detection (insertion/removal)
- Card password protection
- Two 4K FIFO to aid data transfer between the CPU and the controller
- FIFO overrun and underrun handled by stopping the SD clock

CF/CF+ Host controller

- CF Specification Revision 4.1 compliance (True IDE Mode only)
- Multiword DMA to transfer data between the host and the CF/+ device
- Ultra DMA mode for accessing the CF/+ card using the 16-bit data path
- PIO timing mode0 through mode6
- Multiword DMA timing mode0 through mode4
- Ultra DMA timing mode0 through mode6
- Data transfers up to 256 (512 byte) blocks
- Variable-length data transfer in multiword DMA and Ultra DMA modes
- Interrupt-driven data transfers in PIO mode

xD Host controller (Xtreme Digital)

- Comfortable erase mechanism
- Programmable access timing
- Read, write, erase, read device ID, status and reset commands
- ECC generation and checking
- Multiblock programming and multiblock erase
- 1 Gbit, 2 Gbit support

2.14 UART ports

The SPEAr1340 device integrates 2 instances of an asynchronous serial port (UART) digital block, identified as UART0 and UART1.

Asynchronous serial ports are responsible for performing the main tasks in serial communications with computers. The device converts incoming parallel information into serial data and incoming serial information into parallel data that can be sent on a communication line connected to an external peripheral device.

The SPEAr1340 embedded MPU provides two independent UART controllers. One of the typical uses of UART is connecting the SPEAr-based platforms to debugging consoles, the communication with modems and the interfacing of Bluetooth, DECT or ZigBee chipsets. The UART features inside SPEAr1340 offer similar functionality to the industry-standard 16C650 UART device.

UART ports usually do not directly generate or receive the external signals used between different items of equipment. External interface devices are used to convert the logic level signals of the UART to and from the external signaling levels. External signals may be of many different forms, such as RS-232, infrared and wireless radio. In particular, the UART interfaces inside SPEAr1340 directly support (by software selection) the IrDA-compliant Serial InfraRed (SIR) protocol.

The UART supports standard asynchronous communication bits (start, stop, and parity), which are added prior to transmission and removed on reception.

Main features:

UART0 and UART1:

- Support baud rate up to UARTCLK/16
- Programmable baud rate generation (integer and fractional parts)
- Support three options on the UARTCLK clock frequency:
  - 48 MHz: maximum baud rate of 3 Mbps (48/16)
  - 24 MHz: maximum baud rate of 1.5 Mbps (24/16)
  - Programmable by software: up to 125 MHz with a maximum baud rate of 7.81 Mbps (125/16).
- Separate 16x8 transmit and 16x12 receive first-in, first-out memory buffers (FIFOs)
- Programmable FIFO disabling for 1-byte depth
- FIFO trigger levels selectable between 1/8, 1/4, 1/2, 3/4 and 7/8
- Independent masking of transmit FIFO, receive FIFO, receive time-out, and error condition interrupts
- Support for direct memory access (DMA)
- False start bit detection
- Line break generation and detection
- Programmable usage of IrDA SIR encoder/decoder:

  IrDA SIR ENDEC block provides:
  - Support of IrDA SIR ENDEC functions for data rates up to 115.2 Kbits/second half-duplex
  - Support of normal 3/16 and low-power bit durations
  - Programmable internal clock generator enabling division of reference clock by 1 to 256 for low-power mode bit duration
- Fully-programmable serial interface characteristics:
  - data can be 5, 6, 7, or 8 bits
  - even, odd, stick, or no-parity bit generation and detection
  - 1 or 2 stop bit generation

UART0 only:

- Programmable hardware flow control which uses the CTS input and the RTS output to automatically control the serial data flow
- Support modem status which uses:
  - Input signals: Clear To Send (CTS), Data Carrier Detect (DCD), Data Set Ready (DSR), and Ring Indicator (RI)
  - Output modem control lines: Request To Send (RTS), and Data Terminal Ready (DTR)
- Independent masking of modem status

2.15 I2C bus controllers (I2C)

The SPEAr1340 device integrates 2 instances of an I2C controller, identified as I2C0 and I2C1, which can be used to connect to the I2C bus peripheral.

Main features:

- Compliant to the I2C-bus specification from Philips
- Three different operating modes:
  - Standard-speed mode (data rates up to 100 Kb/s)
  - Fast-speed mode (data rates up to 400 Kb/s)
  - High-speed mode
- Clock synchronization
- Master or slave I2C operation mode
- Multimaster operation mode (bus arbitration)
- Support for direct memory access (DMA)
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transfers
- Slave bulk transfer mode
- Ignores CBUS addresses (an older ancestor of I2C that used to share the I2C bus)
- Buffer transmission and reception
- Interrupt or polled-mode operation
- Handles bit and byte waiting at all bus speeds
- Digital filter for the received SDA and SCL lines

2.16 Synchronous serial port (SSP)

The synchronous serial port block includes a master or slave interface to enable synchronous serial communication with slave or master peripherals.

Main features:

- Master or slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive first-in, first-out memory buffers, 16-bit wide, 8 locations deep
- Programmable choice of interface operation, SPI, Microwire, or TI synchronous serial
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO, and receive overrun interrupts
- Internal loopback test mode available
- Support for direct memory access (DMA)

2.17 A/D converter (ADC)

SPEAr1340 integrates an analog-to-digital converter.

Main features:

- Successive approximation A/D conversion
- 10-bit resolution for the analog cell which can be extended up to 12 bits with embedded oversampling techniques performed by the controller
- 1 MSPS
- 8 analog input channels (0 – 2.5 V)
- INL ± 1 LSB
- DNL ± 1 LSB
- Programmable conversion speed – minimum conversion time 1 µs
- Support for resistive touchscreen

2.18 HDMI CEC interfaces (CEC)

The SPEAr1340 device integrates 2 instances of a Consumer Electronics Control (CEC) digital block, identified as CEC0 and CEC1.

CEC is an asynchronous transfer mode adaptation layer (AAL) protocol that provides high-level control functions among the various audiovisual products in a user's environment. CEC operates at low speeds, with minimal processing and memory overhead.

Main features:

- AMBA 2.0 compatible
- One touch play: Play a device and make it the active source with the press of a button
- System standby: Set all devices to standby with the press of a button
- Preset transfer: Auto-configures device presets to match those of the TV
- One-touch record: Enables one-button recording
- Timer programming: Any device can program a recording device's timer
- System information: Devices can auto-configure their language and country settings
- Deck control: A device can control and interrogate a playback device
- Tuner control: A device can control the tuner of another device
- Vendor specific commands: Enables the use of vendor-defined commands
- On-screen display (OSD): A device can display text on the TV screen
- Device menu control: A device can control the menu of another device
- Routing control: Enables CEC switch control, to stream a new source device
- Remote control pass through: Enables the passing on of remote control commands to other devices
- Device OSD name transfer: System devices can request the preferred object-based storage device (OSD) name of other system devices

2.19 General purpose I/O (GPIO/XGPIO)

SPEAr1340 handles generic input/outputs in 3 ways. First, the device integrates 2 instances of a general purpose I/O (GPIO) digital block, identified as GPIOA and GPIOB. Second, an extended GPIO (XGPIO) feature is provided. Finally, it is possible to use the KBD controller in GPIO mode (this feature is documented in *Section 2.28: Keyboard controller (KBD)*).

The GPIO block provides 16 programmable inputs or outputs (8 for GPIOA and 8 for GPIOB). Each input/output can be controlled by software.

GPIO main features:

- 16 individually programmable input/output pins (by default input at reset)
- An APB slave acting as control interface in software mode
- Programmable interrupt generation capability on any number of pins
- Bit masking in both read and writes operation through address lines

The XGPIOs are individually programmable input/output pins (by default output) that can be controlled through an AHB slave interface.

XGPIO main features:

- 234 individually programmable input/output pins: XGPIO0 to XGPIO7, and XGPIO24 to XGPIO249 (by default output). There is just an exception for the bit XGPIO169 which is always an output.
- Programmable interrupt (rise or fall edge sensitive) generation on any number of pins
- An AHB slave interface as control

2.20 LCD display controller (CLCD)

The TFT LCD controller provides all the necessary control signals to interface directly to a variety of TFT LCD panels.

Main features:

- Wide range of programmable LCD panel resolutions
- Support for 1 port TFT LCD panel interfaces:
  - 18-bit digital (6-bit/color)
  - 24-bit digital (8-bit/color) CMOS
- Support for 2 Port TFT LCD panel interfaces (2nd port available by programmable signals)
- Support for up to 2 overlay windows.
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through the color palette to 18-bit LCD pixel
  - up to 18 bpp directly drive 18-bit LCD pixel
  - 24 bpp directly drive 24-bit LCD pixel
- Color Palette RAM to reduce Frame Buffer memory storage requirements bandwidth
- Programmable output format support:
  - RGB 6:6:6 or 5:6:5 or 5:5:5 on 18-bit digital interface
  - RGB 8:8:8 on 24-bit digital interface
- Programmable horizontal timing parameters:
  - horizontal front porch, back porch, sync width, pixels-per-line
  - horizontal sync polarity
- Programmable vertical timing parameters:
  - vertical front porch, back porch, sync width, lines-per-panel
  - vertical sync polarity
- Programmable pixel clock frequency up to 148MHz (1080p resolution)
- Programmable data enable timing signal:
  - derived from horizontal and vertical timing parameters
  - display enable polarity
- Power up and down sequencing support
- Programmable endianness
- Pulse width modulation for LCD panel LED backlight brightness control

2.21 Graphics processing unit (GPU)

The Mali GPU is a hardware accelerator for 2D and 3D graphics systems that forms the basis of a high performance graphics processing solution. When implemented as part of a system-on-chip (SoC) device, the GPU forms an integral part of the graphics solution. The GPU comprises the following:

- an ARM® Mali™200 pixel processor
- a MaliGP2 geometry processor
- a memory management unit (MMU)
- associated software (programmed using OpenVG or OpenGL base layers)

Main features (pixel processor):

- Programmable fragment shader
- Access to framebuffer from fragment shaders
- Alpha blending
- Arbitrary memory reads and writes
- Complete non-power-of-2 texture support
- Cube mapping
- Dynamic recursion
- Fast dynamic branching
- Fast trigonometric functions, including arctangent
- Full floating-point arithmetic
- Framebuffer blend with destination Alpha
- High dynamic range (HDR) textures and framebuffers
- Indexable texture samplers
- Line, quad, triangle, and point sprites
- Multiple render targets
- No limit on program length
- Perspective anisotropic filtering (AF)
- Perspective correct texturing
- Point sampling, bilinear, and trilinear filtering
- Programmable mipmap level-of-detail biasing and replacement
- Register indirect jumps
- Stencil buffering, 8-bit
- Two-sided stencil
- Unlimited dependent texture reads
- Virtualized texture samplers
- 4-level hierarchical Z and stencil operations
- 4 times and 16 times full scene anti-aliasing (FSAA)
- 4-bit per texel texture compression.

Geometry processor

- Programmable vertex shader
- Autonomous operation tile list generation
- Flexible input and output formats
- Indexed and non-indexed geometry input
- Primitive constructions with points, lines, triangles and quads.

Software

- Compatibility with the following graphics standards:
  - OpenGL ES 2.0
  - OpenGL ES 1.1
  - OpenVG 1.0

  The geometry processor must be programmed using OpenVG or Open GL base layers.

2.22 Video decoder (VDEC)

Main features:

- All algorithms in hardware - minimal CPU load
- Minimal power consumption - functional level clock gating and synthesis time clock gating (> 90% of registers under gating)

Supported video codecs:

- H.264 profile and level
  - Baseline, main and high profiles
  - Decoding up to 1080p/30fps(1)
- Scalable video coding (SVC):
  - Baseline and high profiles (base layer only)
- MPEG-4 visual profile and level
  - Simple and advanced simple profiles, levels 0 –5(2)
- H.263 profile and level
  - Profile 0, levels 10 –70 (image size up to 720x576)
- Sorenson Spark
- WMV9 / VC-1
  - Simple, main and advanced profiles, levels 0 -3
- MPEG-1&2 main profile
  - Low, medium and high levels
- RealVideo8/9/10
- DivX®3/4/5/6 support
  - Home theater profile qualification
- VP6, VP7 versions 0-3
- VP8 version 2 (WebM)
- AVS Jizhun Profile
- JPEG, all common sampling formats
  - Baseline interleaved

1. Achievable resolution and frame rate depending on specific stream content and system load.
2. Global motion compensation (GMC) is not supported.

Supported post-processing features:

- Input image source
  - Internal source (combined mode): G1decoder
  - External source (standalone mode): for example, a software decoder or camera interface
- Input image size
  - Combined mode: 48 x 48 to 8176 x 8176 (66.8 Mpixels)
  - Standalone mode: width from 48 to 8176, height from 48 to 8176 (maximum size limited to 16.7 Mpixels)
- Output image size
  - 16 x 16 to 1920 x 1088
- Image scaling
  - Bicubic polynomial interpolation for upscaling
  - Proprietary averaging filter for downscaling
  - Arbitrary, non-integer scaling ratio separately for both dimensions
- YCbCr to RGB color conversion
  - BT.601-5 compliant
  - BT.709 compliant
  - User definable conversion coefficient
- Dithering
  - 2x2 ordered spatial dithering for 4-, 5- and 6-bit RGB channel precision
- Alpha blending
  - Output image can be alpha blended with two rectangular areas
- Deinterlacing
  - Conditional spatial deinterlace filtering; supports only YCbCr 4:2:0 input format
- linear RGB image contrast, brightness and color saturation adjustment
- Deblocking filter for MPEG-4 simple profile /H.263 / Sorenson
  - Using a modified H.264 in-loop filter as a postprocessing filter; filtering has to be performed in combined mode.
- Image cropping / digital zoom
  - User definable start position, height and width
  - Usable only for JPEG or stand-alone mode
- Output image masking
- Image rotation
  - Rotation 90, 180 or 270 degrees
  - Horizontal/vertical flip

2.23 Video encoder (VENC)

A multiformat video encoder is integrated in SPEAr1340 with 64-bit AXI master and 32-bit AHB slave interfaces. It supports H.264 high profile video resolution up to 1080p and JPEG still picture up to 64 Mpixel.

Main features:

- H.264 profile and level
  - Baseline, main and high profiles, levels 1- 4.0
- JPEG profile and level
  - Baseline (DCT sequential)
- Video stabilization
- I and P slices support
- CAVLC baseline and CABAC main profile
- Error resilience
  - Constrained intra prediction
  - Slices, multiple of macro blocks rows
- Maximum motion vector length
  - Vertical ±14 pixels
  - Horizontal ±30pixels
- 12 intra prediction modes
- Motion vector pixel accuracy
  - 720p resolution ¼ pixels
  - 1080p resolution ½ pixels
- Macroblock and sub-macroblock partitions: 16x16, 8x16, 16x8, 8x8, 4x8, 8x4,4x4
- Transforms 4x4 baseline, main and high profiles
- 1 reference frame support
- Maximum 1 slice group support
- Input data formats
  - Planar YCbCr 4:2:0, semiplanar YCbCr 4:2:0, interleaved YCbCr 4:2:2
- Output data formats
  - H.264 (Byte and NAL unit stream)
  - JPEG(JFIF file format 1.02 and non progressive JPEG)
- Supported image size
  - H.264: 96x96 to1920x1020
  - JPEG: 96x96 to 8192x8192
  - Step size 4 pixels
- Pre-processing features
  - YCbCr 4:2:2 to YCbCr 4:2:0 color space conversion for all YCbCr input formats
  - Cropping from 8192 x 8192 to any supported encoding size
  - Rotation of 90 or 270 degrees

2.24 Camera input interfaces (CAM)

The SPEAr1340 device integrates 4 instances of a camera input (CAM) digital block, identified as CAM1, CAM2, CAM3, CAM4.

Each CAM interface enables SPEAr1340 to interface with an external image sensor. An incoming image is stored in CAMIF memory per a programmed mode, and then transferred to external memory using system direct memory access.

Main features:

- AMBA 2.0 compatible
- Slave interface with connection to external system DMA
- 8-bit parallel data interface
- YCbCr4:2:2, RGB888 packed, RGB888 un-packed, RGB565, JPEG mode
- Video mode with all running frame
- Compliant with ITU-R BT.601 (External synchronization) as well as ITU-R BT.656 (embedded synchronization)
- Image cropping
- Programmable polarity of pixel clock and external synchronization signals (HSYNCH, VSYNCH)

Note: For 1080p 30 Hz video maximum pixel clock frequency for CAM required is (2x2200x1125x30)=148.5 MHz.

2.25 Video input parallel port (VIP)

The video input parallel port is used to interface with some external image sensors. Incoming images are stored inside its internal FIFO as per some programmed mode and then transferred to the external memory through the master interface.

Main features:

- Supports HDMI, DVI, DP and CVBS
- Supports output format RGB along with HSYNC, VSYNC and pixel clock
- Clock polarity configuration provided (Positive edge/Negative edge)
- HSYNC and VSYNC polarity configurable
- Handling of data enable signal
- Dual-port display in DVI mode for 16 bpp and 24 bpp supported
- Input bit width 16 bpp, 24 bpp and 32 bpp supported
- Only unpacked data format supported

2.26 I2S digital audio ports (I2S)

The I2S controller is a highly configurable IP for use in audio applications. It provides a simple interface to standard audio components.

Main features:

- Compliant to Philips I2S serial bus specifications
- I2S master for output operations and I2S slave for input operations
- Configurable number of stereo channels (up to 4) for both transmitter and receiver
- Supports up to 7.1 audio Tx and Rx
- Supports 12-/16-/20-/24-/32-bit audio data interface
- Fully synchronous design with serial clock and system clock
- Interrupt support for reporting FIFO and other conditions
- Programmable FIFO thresholds
- Supports data exchange to the system memory through DMA interface
- Software controlled block resets and enables
- Software controlled FIFO flush

2.27 S/PDIF digital audio port

The S/PDIF audio interface detects bi-phase encoded S/PDIF signals, and plays PCM audio data or audio encoded bit streams stored in memory in the S/PDIF format.

Main features:

Input

- Fully compliant with IEC-60958 for audio data
- Supports typical audio sampling frequencies, such as 32, 44.1, 48, 96, and 192 kHz.
- Programmable DMA trigger threshold
- VUCP storage can optionally be disabled
- Audio data can be stored in bit lengths of 16 to 24 bits

Output

- Compliant with IEC-60958 for audio data and IEC-61937 for compressed audio data
- Supports typical audio sampling frequencies such as 32, 44.1, 48, 96, and 192 kHz
- Supports one-bit audio mode (HDMI)
- Supports DTS-HD mode
- Programmable system DMA trigger limit
- Programmable VUCP insertion
- Supports 16/0 or 16/16 audio data format in memory

2.28 Keyboard controller (KBD)

The GPIO keyboard controller integrated in SPEAr1340 offers a 3-mode input and output port. It provides an12-bit GPIO, or 6x6 keyboard, or 2x2 keyboard plus 8-bit GPIO, and offers an interface to the industry standard APB bus.

Main features:

- AMBA APB interface
- GPIO or keyboard functionality with selection of any one of the two keyboard matrices:
  - 12-bit general purpose parallel port (GPIO) with input or output single pin programmability
  - 36 (6x6) keys keyboard
  - 4 (2x2) key keyboard plus 8-bit GPIO with input or output single pin programmability

2.29 Cryptographic co-processor (C3)

C3 is a multipurpose, instruction driven, programmable DMA-based co-processor. It is configured to accelerate cryptographic and network security functions.

Main features:

- AMBA AHB 2.0 master and slave interfaces
- Scatter and gather DMA engine (implemented only by MPCM channel)
- Instruction dispatchers
  - ID0 and ID1 available
  - ID2 and ID3 not available
- Internal RAM: 4Kx32
- Coupling/Chaining: 2 paths

The hardware accelerator crypto algorithms available in SPEAr1340 have the following channels supported by mentioned operations:

- **Channel 0**: Move channel
  - Supported operations: copy, AND, OR, XOR
  - Chained mode: either master or slave
  - Cascaded mode: both master and slave
  - Input FIFO: 8x32 bits
  - Output FIFO: 8x32 bits
- **Channel 1**: Data encryption standard (DES and TripleDES)
  - ID: 0x00002001
  - Supported algorithms: DES (56-bit keys, ECB and CBC encryption/decryption, no parity check) and TripleDES (168-bit keys, ECB and CBC encryption/decryption, EncDecEnc)
  - Input FIFO: 16x32 bits
  - Output FIFO: 16x32 bits
- **Channel 2:** MPCM for the advanced encryption standard (AES)
  - ID: 0x0000E000
  - Supported algorithms: AES (128-, 192-, 256-bit keys, ECB and CBC encryption/decryption, with programmable operation modes to support almost all possible modes, including Counter and XTS mode)
  - Memory for modes of operation: 512 words of 62 bits each
  - Input FIFO: 16x32 bits

  - Output FIFO: 16x32 bits
  - Read scatter/gather list: 4x32 bits
  - Write scatter/gather list: 4x32 bits
- **Channel 3:** Unified hash with HMAC (UHH)
  - ID: 0x00004014
  - Supported algorithms: HMAC MD5 (hash with 128-bit digest), HMAC SHA1 (hash with 160-bit digest) and HMAC SHA2 (SHA256 and SHA224 with 256- and 224-bit digest respectively)
  - Input FIFO: 16x32 bits
  - Output FIFO: 8x32 bits
- **Channel 4**: Unified hash 2 with HMAC (UHH2)
  - ID: 0x00011001
  - Supported algorithms: HMAC SHA384 (hash with 384-bit digest) and HMAC SHA512 (hash with 512-bit digest)
  - Input FIFO: 16x32 bits
  - Output FIFO: 8x32 bits
- **Channel 5**: Public key accelerator (PKA) v6
  - ID: 0x00006001
  - Supported algorithms: modular exponentiation for RSA and Diffie-Hellman (up to 2048 bits), scalar multiplication of elliptic curve points over prime fields for ECC (up to 384 bits) and Montgomery's parameter for finite field operations
  - Input FIFO: 8x32 bits
  - Output FIFO: 8x32 bits
- **Channel 6**: Random number generator (RNG)
  - ID: 0x0000F000
  - Generates a sequence of true random numbers, based on a contiguous analog oscillator; the sequence has a success ratio of more than 85 % for 20.000 bits, according to FIPS 140-1 tests
  - Monitors the entropy of the generated sequence
  - Input FIFO: 2x32 bits
  - Output FIFO: 4x32 bits
- **Channel 7**: empty

2.30 Real-time clock (RTC)

The RTC is a block that keeps track of the real time of day. It also functions as an alarm and a calendar. The time is displayed in 24-hour format, and time/calendar values are stored in binary-coded decimal format.

The time of day, alarm and calendar, status and control registers can all be accessed via a standard 32 APB bus. All read/write operations last 2 cycles.

RTC provides a self-isolation mode that is activated during power down. This allows RTC to continue its operation (except for the alarm interrupt feature that is not preserved) if power is not supplied to the rest of the circuit. This feature is realized by supplying separate power and clock connections.

A set of 16 general purpose registers (GP-Reg) are provided which can be used to save data during the power down state. GP-Reg-set runs on 32 K oscillator clock and powered by RTC battery. Each register is of 32 bits and addressed mapped on the 32-bit APB bus. A bit in status register reflects the status of any pending write to GP-Reg-set. This means that write operation to the GP-Reg-set should be sequential, so you should wait for this pending status bit to be cleared before writing again to GP-Reg-set.

Main features:

- Works on dedicated 32768 Hz external clock and power supply
- 9999- year calendar
- Leap years support
- Programmable alarm interrupt
- Power management and self-isolation
- Prescaler and timer registers bypass for TEST
- Time and date update monitors
- 16 general purpose registers which can be used to save data during power down state

2.31 DMA controllers (DMAC)

The SPEAr1340 device integrates 2 instances of a DMA controller (DMAC) digital block, identified as DMAC0 and DMAC .

The DMAC is an AHB-central DMA controller core that transfers data from a source peripheral to a destination peripheral over two AHB buses. A wrapper is designed to instantiate 2 DMAC cores (each with 2 AHB master interfaces), 2 ICMs (which arbitrate the same master interface of each DMAC) and a MUX (which manages multiple peripheral handshaking interfaces).

Main features:

- AMBA 2.0-compliant
- AHB slave interface – used to program the DMAC
- 8 channels, one per source and destination pair
- Unidirectional channels – data transfers in one direction only
- Programmable channel priority
- 2 independent AHB master interfaces
- Data bus width configured to 64 bits for each AHB master interface
- Configurable endianness for master interfaces
- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral DMA transfers
- Component ID parameters for configurable software driver support
- Programmable source and destination addresses (on AHB bus)
- Address increment, decrement or no change
- Multiblock transfers achieved through linked lists (block chaining)
- Independent source and destination selection of multiblock transfer type
- Scatter/Gather

- Single FIFO per channel for source and destination
- FIFO depth configured to 16 bytes for the first 4 channels and to 128 bytes for the last 4 channels
- D flip-flop-based FIFO
- Automatic data packing or unpacking to fit FIFO width
- Programmable source and destination for each channel
- Programmable transfer type for each channel (memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral)
- Programmable burst transaction size for each channel
- Programmable enable and disable of DMA channel
- Support for disabling channel without data loss
- Support for suspension of DMA operation
- Support for RETRY, SPLIT, and ERROR responses
- Programmable maximum burst transfer size per channel
- Maximum transaction size configured to 256 for all the channels
- Maximum block size configured to 4095 for all the channels
- Bus locking – can be programmed to be over the transaction, block, or DMA transfer level
- Channel locking – can be programmed to be over the transaction, block, or DMA transfer level
- 16 handshaking interfaces for source and destination peripherals
- Hardware and software handshaking interfaces
- Peripheral interrupt handshaking interface
- Handshaking interface supports single or burst DMA transactions
- Polarity control for hardware handshaking interface
- Enabling and disabling of individual DMA handshaking interface
- Programmable flow control at block transfer level (source, destination or DMAC core)
- Software control of source data pre-fetch when destination is flow controller
- Combined and separate interrupt requests
- Interrupt generation on DMA transfer (multiblock) completion, block transfer completion, single and burst transaction completion and error condition
- Support of interrupt enabling and masking.

2.32 General purpose timers (GPT)

The SPEAr1340 device integrates 4 instances of a general purpose timer (GPT) digital block, identified as GPT0, GPT1, GPT2, GPT3. Each instance is a dual timer, for total 8 independent timers.

General purpose timers can be used for precise timing measurement and for measurement of frequency of any input signal. They are essentially counters that increment based on the clock cycle and the timer prescaler. An application can monitor these counters to determine how much time has elapsed. GPT can have timer and capture mode capabilities.

Main features:

- It is constituted by 2 channels; each one consists of a programmable 16-bit counter and a dedicated 4-bit timer clock prescaler
- The programmable 4-bit prescaler unit performs a clock division by 1, 2, 4, 8, 16, 32, 64, 128 and 256
- Three interrupt sources (MATCH, REDG, and FEDG) are available for each timer channel. They are mapped to a single interrupt line for each channel but may be individually masked and acknowledged
- Each timer has a separate register set to control, enable and run each channel separately
- Three modes of operations are available for each timer channel:
  - Auto-reload mode
  - Single-shot mode
  - Capture function

2.33 PWM generators (PWM)

The PWM is a pulse-width modulation (PWM) timer module with four independent channels (PWM1, PWM2, PWM3, and PWM4). All four channels are functionally identical. Using a 16-bit counter, each PWM channel generates a rectangular output pulse with programmable duty factor (0 to 100%) and frequency.

The four channels can work either synchronously or asynchronously.

Main features:

- Four independent PWM channels
- Synchronous and asynchronous working modes
- Prescaler to define the input clock frequency for each timer
- Programmable duty factor from 0 to 100%
- Programmable pulse frequency
- APB slave interface for programming registers
- APB clock (PCLK ~ 83 MHz) as the prescaler source clock

2.34 Clock and reset system

This centralized structure provides system synchronization.

Main features:

- Six PLLs. Four of them are fully programmable and offer an EMI reduction mode (spread spectrum clock generation through dithering) that can replace all traditional EMI reduction techniques.
  - PLL1 programmable dithered pll, dedicated for Core1 & 2 & AXI/AHB bus & peripherals. Both core need to run at the same speed
  - PLL2 programmable dithered PLL, dedicated for the 125 MHz clock of the Gigabit Ethernet MAC
  - PLL3 programmable dithered PLL, for specific embedded IP functions
  - PLL4 programmable dithered PLL, dedicated for the DDR memory controller (Asynchronous access memory mode)
  - PLL5 low jitter, dedicated for the USB
  - PLL6 for the PCIe controllers
- Several synthesizers provide different frequencies for different IPs
- Fully programmable control of clock and reset signals for all slave blocks allowing sophisticated power management.

2.35 Reset and clock generator (RCG)

The reset and clock generator (RCG) provides the system clocks and resets. It is highly configurable through the miscellaneous registers.

Main features:

- Three main clock sources:
  - osci1: 24 MHz clock coming from internal oscillator connected to external quartz
  - osci2: 32 kHz clock coming from internal oscillator used for RTC block (optional)
  - osci3: 25/100 MHz clock coming from MIPHY macro (optional)
- Three programmable dithered PLLs (to reduce EMI):
  - PLL1: primarily used to generate the 1 GHz clock for the AMBA subsystem
  - PLL2, PLL3: primarily used to generate clocks for generic IPs
- Seven configurable clock generators:
  - SSCG1-4: used by generic IPs
  - SSCG5: for CPU clock
  - SSCG6: for CLCD clock
  - SSCG7: for AHB, APB clocks
- Three operating modes for AMBA clocks:
  - DOZE: the clock source is osci2 (osci1 after power on)
  - SLOW: the clock source is the osci1 or a divided version
  - NORMAL: the clock source is PLL1 (by default), PLL2, PLL3 or SSCG7
- Configurable clock gating and software reset for most peripherals
- Global software reset and watchdog reset

2.36 Power control module (PCM)

PCM is the core of the SPEAr1340 leakage power management system. Its role is to properly manage the power supply shutoff of the switchable sections of the embedded MPU.

Main features:

- Generation of supply switch control signals for SPEAr1340 power islands
- Generation of isolation control signals for SPEAr1340 power islands
- Generation of shutoff commands for external DDR 1V2 and 1V5/1V8 supply lines
- Acknowledge generation for user requested power island configuration
- Monitoring of voltage detector outputs for each power island
- Wake-up source management

2.37 Temperature sensor (THSENS)

The THSENS block is an embedded sensor for junction temperature monitoring.

Main features:

- Embeds a thermal sensor providing digital measurement of junction temperature
- Generates a “high-temperature” interrupt when junction temperature exceeds a software programmable higher bound threshold
- Generates a “low-temperature” interrupt when junction temperature is lower than a software programmable lower bound threshold
- Supports operating conditions ranging from –40 to 125°C
- Allows measurement of junction temperature starting at 20°C
- Allows offset correction of digital measurement (typical correction value 10)
- Software programmable power-down functionality for lower power consumption
- Continuous (periodic) sensing of temperature when not powered down

2.38 One-time programmable antifuse (OTP)

The OTP block is an array of one-time programmable antifuse memory cells. All OTP banks feature an embedded charge pump which provides internally the high voltage necessary for antifuse programming sessions. Therefore, it is not necessary to use an additional high voltage pad at the chip interface. OTP is software programmable, so no dedicated programming interface is needed at chip level.

Main features:

OTP embeds three 255-bit banks, with these features:

- BANK 1: 255-bit data bank with write-protect mechanism
- BANK 2: 255-bit data bank with write-protect mechanism
- BANK M: 255-bit bank, logically partitioned as follows:
  - 32 bits (16 + redundancy) used for BANK1/BANK2 write protection
  - 213 bits BootROM controlled
  - 2 bits reserved
  - 2 bits reserved for disabling TEST access to OTP
  - 2 bits reserved for disabling JTAG access
  - 4 bits BootROM controlled

3 Pin description

This chapter provides a full description of the ball characteristics and the signal multiplexing of SPEAr1340 device.

- *Section 3.1* shows the pin map of SPEAr1340.
- *Section 3.2* shows the association between balls and pads providing a detailed description of their terminal characteristics.
- *Section 3.3* describes the power supply pins.
- *Section 3.4* shows the multiplexing scheme for multiplexed IPs.
- *Section 3.5* describes the pinout for each IP, categorized by functionality.
- *Section 3.6* describes the strapping options configuration and the hardware Boot selection.

The following table explains the table headers and abbreviations used in this chapter.

Note: In this chapter "na" stands for "not applicable".

Table 2. Headers/abbreviations

Header	Description	Abbreviations
Ball	Ball number associated with each signal on the package.	–
Pin name	Name of signals multiplexed on each ball. Note that at reset and after reset release, all I/O pads (except for USB) are in input. To choose between the possible configurations, you need to program each IP by software. Please refer to *Section 3.4: Multiplexed signals description* and SPEAr1340 reference manuals for more information.	–
Signal type	Signal information (direction, type)	I= Input O= Output IO= Input/output S= Depending on strapping option D= Open drain PWR= Power supply GND= Ground Z= High-impedance

Table 2. Headers/abbreviations (continued)

Header	Description	Abbreviations
Pin type	Pad type information	ANA= Analog OSC= Oscillator SSTL= SSTL 1V5/1V8 IOTYPE1= 3V3 IOTYPE2= 3V3/1V8 IOTYPE3= 3V3/2V5 IOTYPE4= 3V3 TTL buffer REG OUT= Voltage regulator output ANA REF= Analog reference DED GND= Dedicated ground
PU/PD	Indicates the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down can be enabled or disabled via software.	PU= Pull-up PD= Pull-down Deact= Deactivated
Drive	Drive current capability	–
Slew	Signal transition	FAST= Fast slew NOM= Nominal slew
Direction	Indicates the direction of the pad.	I= Input O= Output IO= Input/output
Out value	Indicates the electrical value on the ball.	0= The buffer drives V_{OL} 1= The buffer drives V_{OH} H= High-impedance with an active pull-up resistor L= High-impedance with an active pull-down resistor Z= High-impedance
Supply name	The voltage supply that powers the pad. See *Table 4: Power supply signals description*.	–
Reset state	Indicates the state during reset	–
Reset rel. state	Indicates the state after reset	–
Reset mode	IO voltage setting during reset	–
Reset rel. mode	IO voltage setting after reset	–
Compensation cell	Compensation cell for reducing the spread of PVT (process, voltage and temperature) related parameters of the I/O pad. The compensation values are programmable in the registers of the related cell.	CC1= IO_COMP1_3V3 CC2= IO_COMP2_3V3 CC3= IO_COMP1_1V8_3V3 CC4= IO_COMP2_1V8_3V3 CC5= IO_COMP_2V5_3V3 CC6= IO_COMP_DDR

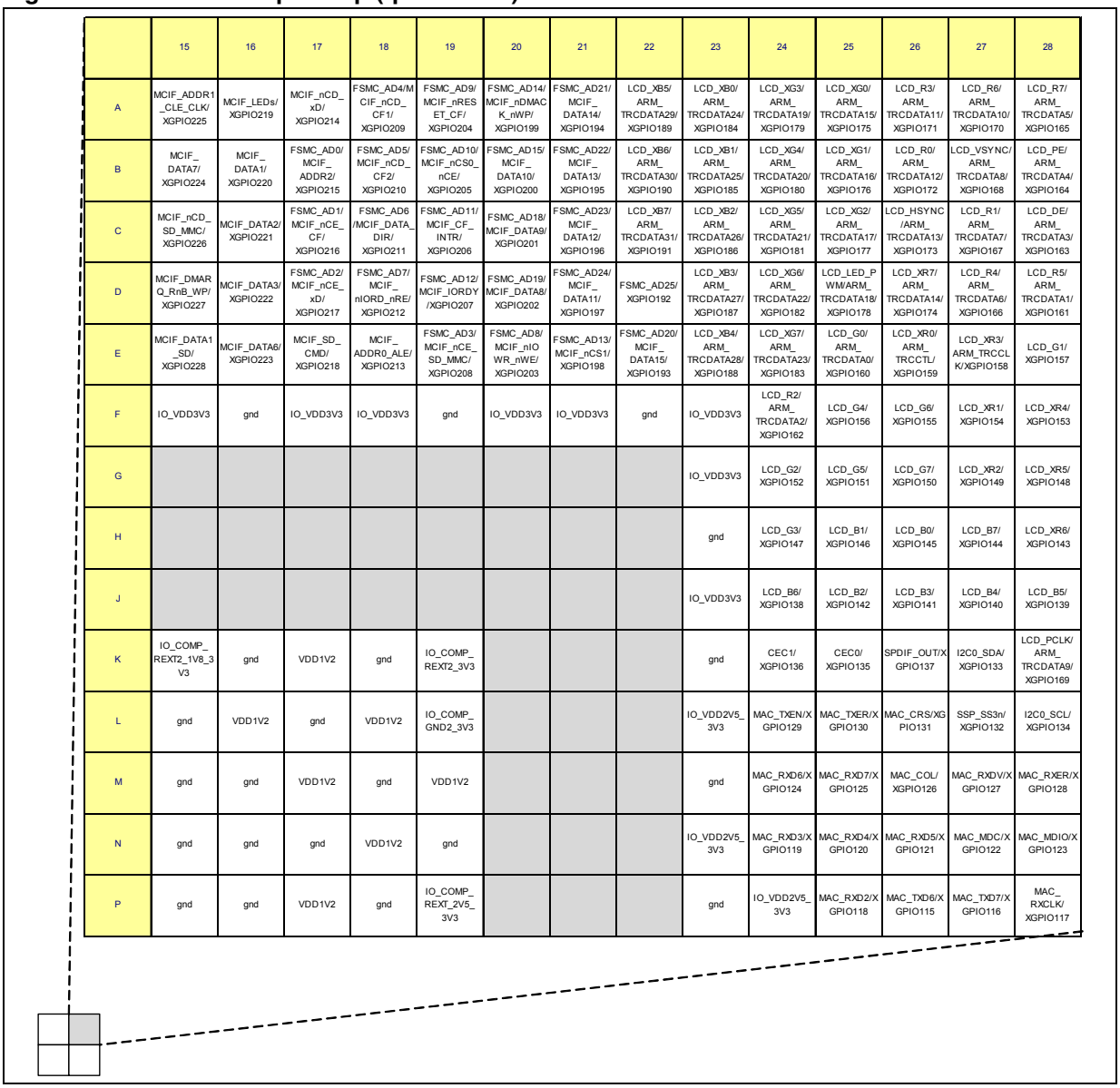
3.1 Pin map

The following figures show the pin map of the device in four quadrants (A, B, C and D).

Figure 2. SPEAr1340 pin map (quadrant A)

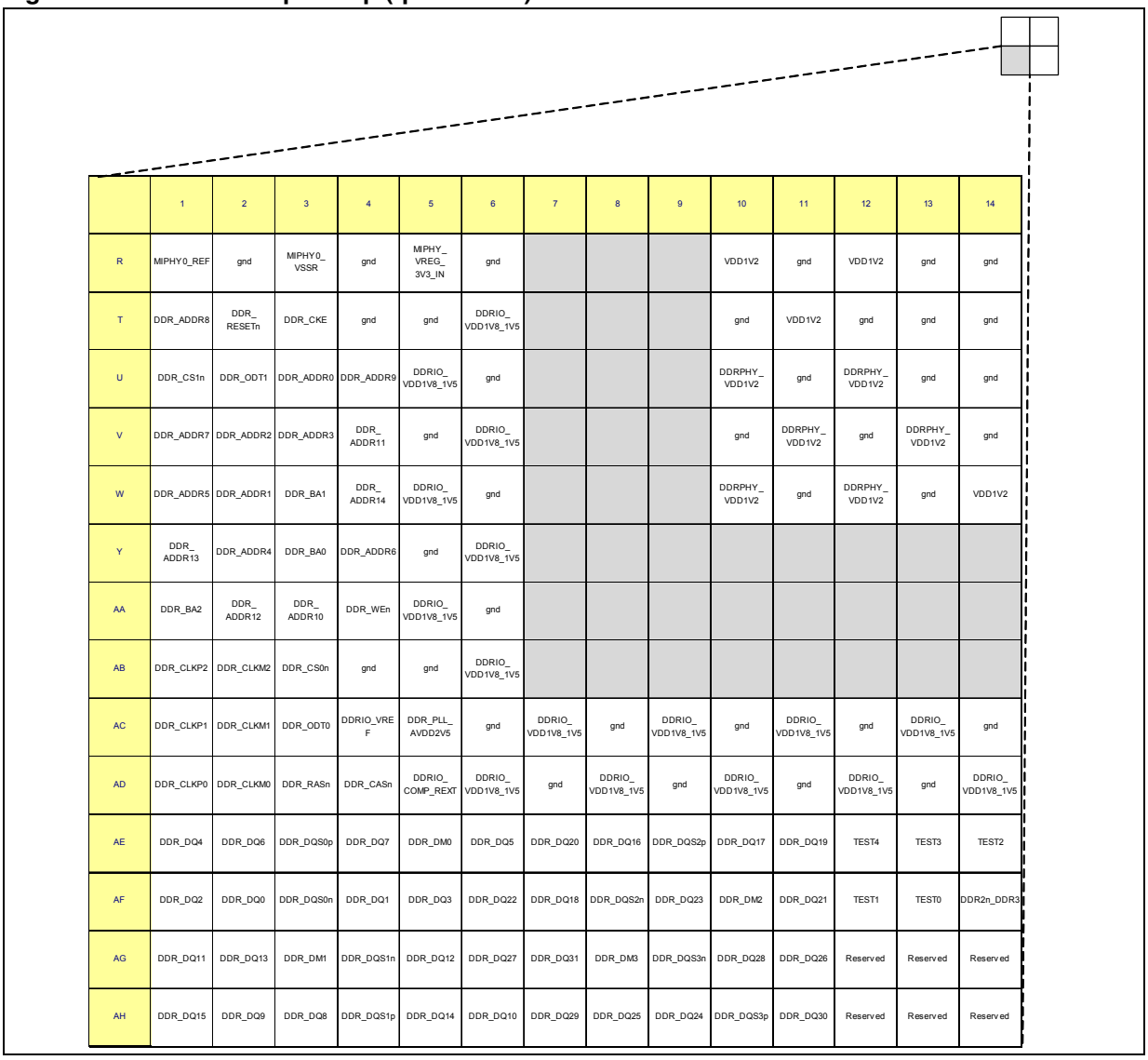
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	RTC_XO	AIN4	AIN3	AIN0	ADC_ VREFP	gnd	MCLK_XI	MCLK_XO	FSMC_IO7/ XGPIO238	FSMC_RSTP WDWN1/ KBD_COL4/ GPIO_A2	FSMC_IO13/K BD_ROW5/X GPIO5	FSMC_IO8/ KBD_ROW0/X GPIO0	USB_UOC_D RVVBUS	MCIF_ DATA2_SD/ XGPIO229
B	RTC_XI	AIN5	AIN6	AIN1	ADC_ VREFN	gnd	MCLK_ AVDD1V2	MCLK_ AVDD3V3	FSMC_IO6/ XGPIO239	FSMC_IO2/ XGPIO233	FSMC_IO14/K BD_COL0/XG PIO6	FSMC_IO9/ KBD_ROW1/X GPIO1	USB_UHC0_ DRVVBUS	MCIF_ DATA3_SD/ XGPIO230
C	RTC_ VDD1V5	AIN7	AIN2	ADC_ AVDD2V5	ADC_AGND	FSMC_CE0n/ XGPIO249	FSMC_RWPR T0n/ XGPIO246	FSMC_ALE_A D17/ XGPIO243	FSMC_IO5/ XGPIO240	FSMC_IO1/ XGPIO234	FSMC_IO15/K BD_COL1/XG PIO7	FSMC_IO10/K BD_ROW2/X GPIO2	USB_UHC1_ DRVVBUS	MCIF_ DATA4/ XGPIO231
D	USB_UHC1_ DP	USB_UHC1_ DM	USB_UHC1_ VDD3V3	PLL2_ VDD1V2	gnd	PLL1_ VDD1V2	FSMC_RB0/X GPIO247	FSMC_REn/X GPIO244	FSMC_IO4/ XGPIO241	FSMC_IO0/ XGPIO235	FSMC_CE1n/ KBD_COL2/G PIO_A0	FSMC_IO11/K BD_ROW3/X GPIO3	USB_UHC0_ OVERCUR	MCIF_ DATA5/ XGPIO232
E	USB_ ANALOG_ TEST	USB_UHC1_ VDD1V2	USB_UHC1_ VDD2V5	PLL2_ AVDD2V5	gnd	PLL1_ AVDD2V5	FSMC_CLE_A D16/ XGPIO248	FSMC_WEn/ XGPIO245	FSMC_IO3/ XGPIO242	FSMC_RST PWDWN0/ XGPIO236	FSMC_ RWPRT1n/ KBD_COL3/ GPIO_A1	FSMC_IO12/K BD_ROW4/ XGPIO4	USB_UHC1_ OVERCUR	MCIF_ DATA0/ XGPIO237
F	USB_UOC_D P	USB_UOC_D M	USB_UOC_V BUS	USB_UOC_ ID	gnd	VREG2_ 2V5_OUT	gnd	IO_ VDD1V8_ 3V3	IO_ VDD1V8 _3V3	gnd	IO_ VDD1V8 _3V3_1	IO_ VDD1V8 _3V3_1	gnd	IO_ VDD3V3
G	USB_ TXRTUNE	USB_UOC_V DD3V3	USB_UOC_V DD2V5	gnd	gnd	gnd								
H	USB_UHC0_ DP	USB_UHC0_ DM	USB_ VSSAC	USB_UOC_ VDD1V2	gnd	VREG2 _3V3_IN								
J	MIPHY0_ VSSR	MIPHY0_ VSSR	USB_UHC0_ VDD3V3	USB_UHC0_ VDD2V5	gnd	gnd								
K	MIPHY0_ RXn	MIPHY0_ RXp	MIPHY0_ VSSR	USB_UHC0_ VDD1V2	gnd	VREG1_ 3V3_IN				gnd	IO_COMP_ GND1_ 1V8_3V3	IO_COMP_ REXT1_ 1V8_3V3	VDD1V2	IO_COMP_ GND2_ 1V8_3V3
L	MIPHY0_ VSSR	MIPHY0_ VSSR	MIPHY0_ VDDR1V2	gnd	gnd	gnd				VDD1V2	gnd	VDD1V2	gnd	VDD1V2
M	MIPHY0_ TXn	MIPHY0_ TXp	MIPHY0_ VSSR	VDD1V2	gnd	VREG1_ 2V5_OUT				gnd	VDD1V2	gnd	gnd	gnd
N	MIPHY0_ VDDT1V2	MIPHY0_ VDD PLL1V2	MIPHY0_ VSST	gnd	PLL3_ AVDD2V5	gnd				VDD1V2	gnd	VDD1V2	gnd	gnd
P	MIPHY0_ XTAL2	MIPHY0_ XTAL1	MIPHY0_ VDD2 PLL2V5	MIPHY0_ VSSPLL	gnd	PLL3_ VDD1V2				gnd	VDD1V2	gnd	gnd	gnd

Figure 3. SPEAr1340 pin map (quadrant B)



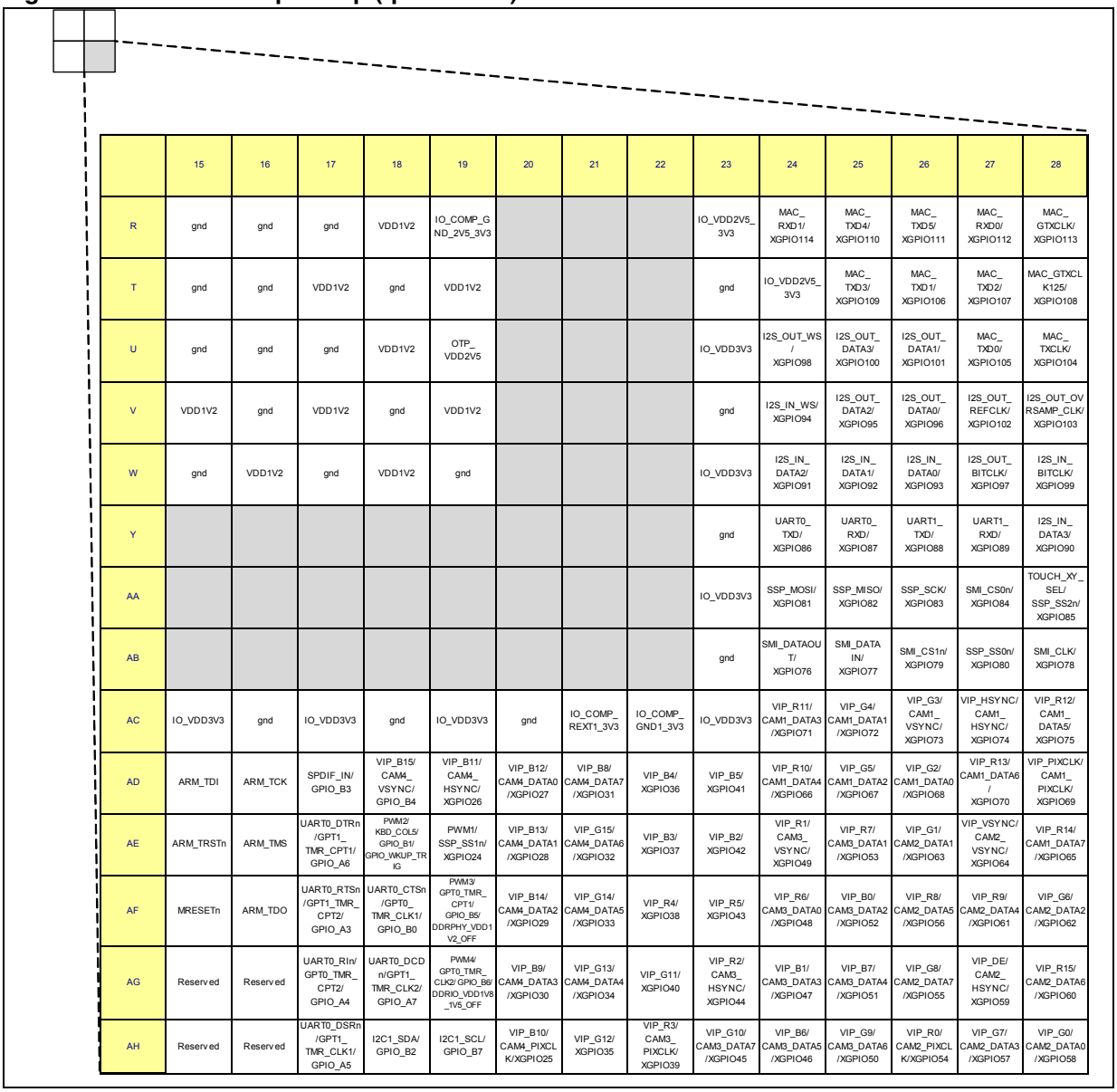
	15	16	17	18	19	20	21	22	23	24	25	26	27	28
A	MCIF_ADDR1_CLE_CLK/ XGPIO225	MCIF_LEDs/ XGPIO219	MCIF_nCD_xD/ XGPIO214	FSMC_AD4/MCIF_nCD_CF1/ XGPIO209	FSMC_AD9/ MCIF_nRESET_CF/ XGPIO204	FSMC_AD14/ MCIF_nDMACK_nWP/ XGPIO199	FSMC_AD21/ MCIF_DATA14/ XGPIO194	LCD_XB5/ ARM_TRCDATA29/ XGPIO189	LCD_XB0/ ARM_TRCDATA24/ XGPIO184	LCD_XG3/ ARM_TRCDATA19/ XGPIO179	LCD_XG0/ ARM_TRCDATA15/ XGPIO175	LCD_R3/ ARM_TRCDATA11/ XGPIO171	LCD_R6/ ARM_TRCDATA10/ XGPIO170	LCD_R7/ ARM_TRCDATA5/ XGPIO165
B	MCIF_DATA7/ XGPIO224	MCIF_DATA1/ XGPIO220	FSMC_AD0/ MCIF_ADDR2/ XGPIO215	FSMC_AD5/ MCIF_nCD_CF2/ XGPIO210	FSMC_AD10/ MCIF_nCS0_nCE/ XGPIO205	FSMC_AD15/ MCIF_DATA10/ XGPIO200	FSMC_AD22/ MCIF_DATA13/ XGPIO195	LCD_XB6/ ARM_TRCDATA30/ XGPIO190	LCD_XB1/ ARM_TRCDATA25/ XGPIO185	LCD_XG4/ ARM_TRCDATA20/ XGPIO180	LCD_XG1/ ARM_TRCDATA16/ XGPIO176	LCD_R0/ ARM_TRCDATA12/ XGPIO172	LCD_VSYNC/ ARM_TRCDATA8/ XGPIO168	LCD_PE/ ARM_TRCDATA4/ XGPIO164
C	MCIF_nCD_SD_MMC/ XGPIO226	MCIF_DATA2/ XGPIO221	FSMC_AD1/ MCIF_nCE_CF/ XGPIO216	FSMC_AD6/MCIF_DATA_DIR/ XGPIO211	FSMC_AD11/ MCIF_CF_INTR/ XGPIO206	FSMC_AD18/ MCIF_DATA9/ XGPIO201	FSMC_AD23/ MCIF_DATA12/ XGPIO196	LCD_XB7/ ARM_TRCDATA31/ XGPIO191	LCD_XB2/ ARM_TRCDATA26/ XGPIO186	LCD_XG5/ ARM_TRCDATA21/ XGPIO181	LCD_XG2/ ARM_TRCDATA17/ XGPIO177	LCD_HSYNC/ARM_TRCDATA13/ XGPIO173	LCD_R1/ ARM_TRCDATA7/ XGPIO167	LCD_DE/ ARM_TRCDATA3/ XGPIO163
D	MCIF_DMARQ_RnB_WP/ XGPIO227	MCIF_DATA3/ XGPIO222	FSMC_AD2/ MCIF_nCE_xD/ XGPIO217	FSMC_AD7/ MCIF_nIORD_nRE/ XGPIO212	FSMC_AD12/ MCIF_IORDY/XGPIO207	FSMC_AD19/ MCIF_DATA8/ XGPIO202	FSMC_AD24/ MCIF_DATA11/ XGPIO197	FSMC_AD25/ XGPIO192	LCD_XB3/ ARM_TRCDATA27/ XGPIO187	LCD_XG6/ ARM_TRCDATA22/ XGPIO182	LCD_LED_PWM/ARM_TRCDATA18/ XGPIO178	LCD_XR7/ ARM_TRCDATA14/ XGPIO174	LCD_R4/ ARM_TRCDATA6/ XGPIO166	LCD_R5/ ARM_TRCDATA1/ XGPIO161
E	MCIF_DATA1_SD/ XGPIO228	MCIF_DATA6/ XGPIO223	MCIF_SD_CMD/ XGPIO218	MCIF_ADDR0_ALE/ XGPIO213	FSMC_AD3/ MCIF_nCE_SD_MMC/ XGPIO208	FSMC_AD8/ MCIF_nIOWR_nWE/ XGPIO203	FSMC_AD13/ MCIF_nCS1/ XGPIO198	FSMC_AD20/ MCIF_DATA15/ XGPIO193	LCD_XB4/ ARM_TRCDATA28/ XGPIO188	LCD_XG7/ ARM_TRCDATA23/ XGPIO183	LCD_G0/ ARM_TRCDATA0/ XGPIO160	LCD_XR0/ ARM_TRCCTL/ XGPIO159	LCD_XR3/ ARM_TRCCLK/XGPIO158	LCD_G1/ XGPIO157
F	IO_VDD3V3	gnd	IO_VDD3V3	IO_VDD3V3	gnd	IO_VDD3V3	IO_VDD3V3	gnd	IO_VDD3V3	LCD_R2/ ARM_TRCDATA2/ XGPIO162	LCD_G4/ XGPIO156	LCD_G6/ XGPIO155	LCD_XR1/ XGPIO154	LCD_XR4/ XGPIO153
G									IO_VDD3V3	LCD_G2/ XGPIO152	LCD_G5/ XGPIO151	LCD_G7/ XGPIO150	LCD_XR2/ XGPIO149	LCD_XR5/ XGPIO148
H									gnd	LCD_G3/ XGPIO147	LCD_B1/ XGPIO146	LCD_B0/ XGPIO145	LCD_B7/ XGPIO144	LCD_XR6/ XGPIO143
J									IO_VDD3V3	LCD_B6/ XGPIO138	LCD_B2/ XGPIO142	LCD_B3/ XGPIO141	LCD_B4/ XGPIO140	LCD_B5/ XGPIO139
K	IO_COMP_REXT2_1V8_3V3	gnd	VDD1V2	gnd	IO_COMP_REXT2_3V3				gnd	CEC1/ XGPIO136	CEC0/ XGPIO135	SPDIF_OUT/XGPIO137	I2C0_SDA/ XGPIO133	LCD_PCLK/ ARM_TRCDATA9/ XGPIO169
L	gnd	VDD1V2	gnd	VDD1V2	IO_COMP_GND2_3V3				IO_VDD2V5_3V3	MAC_TXEN/XGPIO129	MAC_TXER/XGPIO130	MAC_CRS/XGPIO131	SSP_SS3n/ XGPIO132	I2C0_SCL/ XGPIO134
M	gnd	gnd	VDD1V2	gnd	VDD1V2				gnd	MAC_RXD6/XGPIO124	MAC_RXD7/XGPIO125	MAC_COL/ XGPIO126	MAC_RXDV/XGPIO127	MAC_RXER/XGPIO128
N	gnd	gnd	gnd	VDD1V2	gnd				IO_VDD2V5_3V3	MAC_RXD3/XGPIO119	MAC_RXD4/XGPIO120	MAC_RXD5/XGPIO121	MAC_MDC/XGPIO122	MAC_MDIO/XGPIO123
P	gnd	gnd	VDD1V2	gnd	IO_COMP_REXT_2V5_3V3				gnd	IO_VDD2V5_3V3	MAC_RXD2/XGPIO118	MAC_TXD6/XGPIO115	MAC_TXD7/XGPIO116	MAC_RXCLK/ XGPIO117

Figure 4. SPEAr1340 pin map (quadrant C)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	MIPHY0_REF	gnd	MIPHY0_ VSSR	gnd	MIPHY_ VREG_ 3V3_IN	gnd				VDD1V2	gnd	VDD1V2	gnd	gnd
T	DDR_ADDR8	DDR_ RESETn	DDR_CKE	gnd	gnd	DDRIO_ VDD1V8_1V5				gnd	VDD1V2	gnd	gnd	gnd
U	DDR_CS1n	DDR_ODT1	DDR_ADDR0	DDR_ADDR9	DDRIO_ VDD1V8_1V5	gnd				DDRPHY_ VDD1V2	gnd	DDRPHY_ VDD1V2	gnd	gnd
V	DDR_ADDR7	DDR_ADDR2	DDR_ADDR3	DDR_ ADDR11	gnd	DDRIO_ VDD1V8_1V5				gnd	DDRPHY_ VDD1V2	gnd	DDRPHY_ VDD1V2	gnd
W	DDR_ADDR5	DDR_ADDR1	DDR_BA1	DDR_ ADDR14	DDRIO_ VDD1V8_1V5	gnd				DDRPHY_ VDD1V2	gnd	DDRPHY_ VDD1V2	gnd	VDD1V2
Y	DDR_ ADDR13	DDR_ADDR4	DDR_BA0	DDR_ADDR6	gnd	DDRIO_ VDD1V8_1V5								
AA	DDR_BA2	DDR_ ADDR12	DDR_ ADDR10	DDR_WEn	DDRIO_ VDD1V8_1V5	gnd								
AB	DDR_CLKP2	DDR_CLKM2	DDR_CS0n	gnd	gnd	DDRIO_ VDD1V8_1V5								
AC	DDR_CLKP1	DDR_CLKM1	DDR_ODT0	DDRIO_VRE F	DDR_PLL_ AVDD2V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd
AD	DDR_CLKP0	DDR_CLKM0	DDR_RASn	DDR_CASn	DDRIO_ COMP_REXT	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5	gnd	DDRIO_ VDD1V8_1V5
AE	DDR_DQ4	DDR_DQ6	DDR_DQS0p	DDR_DQ7	DDR_DM0	DDR_DQ5	DDR_DQ20	DDR_DQ16	DDR_DQS2p	DDR_DQ17	DDR_DQ19	TEST4	TEST3	TEST2
AF	DDR_DQ2	DDR_DQ0	DDR_DQS0n	DDR_DQ1	DDR_DQ3	DDR_DQ22	DDR_DQ18	DDR_DQS2n	DDR_DQ23	DDR_DM2	DDR_DQ21	TEST1	TEST0	DDR2n_DDR3
AG	DDR_DQ11	DDR_DQ13	DDR_DM1	DDR_DQS1n	DDR_DQ12	DDR_DQ27	DDR_DQ31	DDR_DM3	DDR_DQS3n	DDR_DQ28	DDR_DQ26	Reserved	Reserved	Reserved
AH	DDR_DQ15	DDR_DQ9	DDR_DQ8	DDR_DQS1p	DDR_DQ14	DDR_DQ10	DDR_DQ29	DDR_DQ25	DDR_DQ24	DDR_DQS3p	DDR_DQ30	Reserved	Reserved	Reserved

Figure 5. SPEAr1340 pin map (quadrant D)



	15	16	17	18	19	20	21	22	23	24	25	26	27	28
R	gnd	gnd	gnd	VDD1V2	IO_COMP_GND_2V5_3V3				IO_VDD2V5_3V3	MAC_RXD1/XGPIO114	MAC_TXD4/XGPIO110	MAC_TXD5/XGPIO111	MAC_RXD0/XGPIO112	MAC_GTXCLK/XGPIO113
T	gnd	gnd	VDD1V2	gnd	VDD1V2				gnd	IO_VDD2V5_3V3	MAC_TXD3/XGPIO109	MAC_TXD1/XGPIO106	MAC_TXD2/XGPIO107	MAC_GTXCLK125/XGPIO108
U	gnd	gnd	gnd	VDD1V2	OTP_VDD2V5				IO_VDD3V3	I2S_OUT_WS/XGPIO98	I2S_OUT_DATA3/XGPIO100	I2S_OUT_DATA1/XGPIO101	MAC_TXD0/XGPIO105	MAC_TXCLK/XGPIO104
V	VDD1V2	gnd	VDD1V2	gnd	VDD1V2				gnd	I2S_IN_WS/XGPIO94	I2S_OUT_DATA2/XGPIO95	I2S_OUT_DATA0/XGPIO96	I2S_OUT_REFCLK/XGPIO102	I2S_OUT_OVRSAMP_CLK/XGPIO103
W	gnd	VDD1V2	gnd	VDD1V2	gnd				IO_VDD3V3	I2S_IN_DATA2/XGPIO91	I2S_IN_DATA1/XGPIO92	I2S_IN_DATA0/XGPIO93	I2S_OUT_BITCLK/XGPIO97	I2S_IN_BITCLK/XGPIO99
Y									gnd	UART0_TXD/XGPIO86	UART0_RXD/XGPIO87	UART1_TXD/XGPIO88	UART1_RXD/XGPIO89	I2S_IN_DATA3/XGPIO90
AA									IO_VDD3V3	SSP_MOSI/XGPIO81	SSP_MISO/XGPIO82	SSP_SCK/XGPIO83	SMI_CS0n/XGPIO84	TOUCH_XY_SEL/SSP_SS2n/XGPIO85
AB									gnd	SMI_DATAOUT/XGPIO76	SMI_DATAIN/XGPIO77	SMI_CS1n/XGPIO79	SSP_SS0n/XGPIO80	SMI_CLK/XGPIO78
AC	IO_VDD3V3	gnd	IO_VDD3V3	gnd	IO_VDD3V3	gnd	IO_COMP_REXT1_3V3	IO_COMP_GND1_3V3	IO_VDD3V3	VIP_R11/CAM1_DATA3/XGPIO71	VIP_G4/CAM1_DATA1/XGPIO72	VIP_G3/CAM1_VSYNC/XGPIO73	VIP_HSYNC/CAM1_HSYNC/XGPIO74	VIP_R12/CAM1_DATA5/XGPIO75
AD	ARM_TDI	ARM_TCK	SPDIF_IN/GPIO_B3	VIP_B15/CAM4_VSYNC/GPIO_B4	VIP_B11/CAM4_HSYNC/XGPIO26	VIP_B12/CAM4_DATA0/XGPIO27	VIP_B8/CAM4_DATA7/XGPIO31	VIP_B4/XGPIO36	VIP_B5/XGPIO41	VIP_R10/CAM1_DATA4/XGPIO66	VIP_G5/CAM1_DATA2/XGPIO67	VIP_G2/CAM1_DATA0/XGPIO68	VIP_R13/CAM1_DATA6/XGPIO70	VIP_PIXCLK/CAM1_PIXCLK/XGPIO69
AE	ARM_TRSTn	ARM_TMS	UART0_DTRn/GPT1_TMR_CPT1/GPIO_A6	PWM2/KBD_COL5/GPIO_B1/GPIO_WKUP_TRIG	PWM1/SSP_SS1n/XGPIO24	VIP_B13/CAM4_DATA1/XGPIO28	VIP_G15/CAM4_DATA6/XGPIO32	VIP_B3/XGPIO37	VIP_B2/XGPIO42	VIP_R1/CAM3_VSYNC/XGPIO49	VIP_R7/CAM3_DATA1/XGPIO53	VIP_G1/CAM2_DATA1/XGPIO63	VIP_VSYNC/CAM2_VSYNC/XGPIO64	VIP_R14/CAM1_DATA7/XGPIO65
AF	MRESETn	ARM_TDO	UART0_RTSn/GPT1_TMR_CPT2/GPIO_A3	UART0_CTSn/GPT0_TMR_CLK1/GPIO_B0	PWM3/GPT0_TMR_CPT1/GPIO_B5/DDRPHY_VDD1V2_OFF	VIP_B14/CAM4_DATA2/XGPIO29	VIP_G14/CAM4_DATA5/XGPIO33	VIP_R4/XGPIO38	VIP_R5/XGPIO43	VIP_R6/CAM3_DATA0/XGPIO48	VIP_B0/CAM3_DATA2/XGPIO52	VIP_R8/CAM2_DATA5/XGPIO56	VIP_R9/CAM2_DATA4/XGPIO61	VIP_G6/CAM2_DATA2/XGPIO62
AG	Reserved	Reserved	UART0_RIn/GPT0_TMR_CPT2/GPIO_A4	UART0_DCDn/GPT1_TMR_CLK2/GPIO_A7	PWM4/GPT0_TMR_CLK2/GPIO_B6/DDRIO_VDD1V8_1V5_OFF	VIP_B9/CAM4_DATA3/XGPIO30	VIP_G13/CAM4_DATA4/XGPIO34	VIP_G11/XGPIO40	VIP_R2/CAM3_HSYNC/XGPIO44	VIP_B1/CAM3_DATA3/XGPIO47	VIP_B7/CAM3_DATA4/XGPIO51	VIP_G8/CAM2_DATA7/XGPIO55	VIP_DE/CAM2_HSYNC/XGPIO59	VIP_R15/CAM2_DATA6/XGPIO60
AH	Reserved	Reserved	UART0_DSRn/GPT1_TMR_CLK1/GPIO_A5	I2C1_SDA/GPIO_B2	I2C1_SCL/GPIO_B7	VIP_B10/CAM4_PIXCLK/XGPIO25	VIP_G12/XGPIO35	VIP_R3/CAM3_PIXCLK/XGPIO39	VIP_G10/CAM3_DATA7/XGPIO45	VIP_B6/CAM3_DATA5/XGPIO46	VIP_G9/CAM3_DATA6/XGPIO50	VIP_R0/CAM2_PIXCLK/XGPIO54	VIP_G7/CAM2_DATA3/XGPIO57	VIP_G0/CAM2_DATA0/XGPIO58

3.2 Ball characteristics

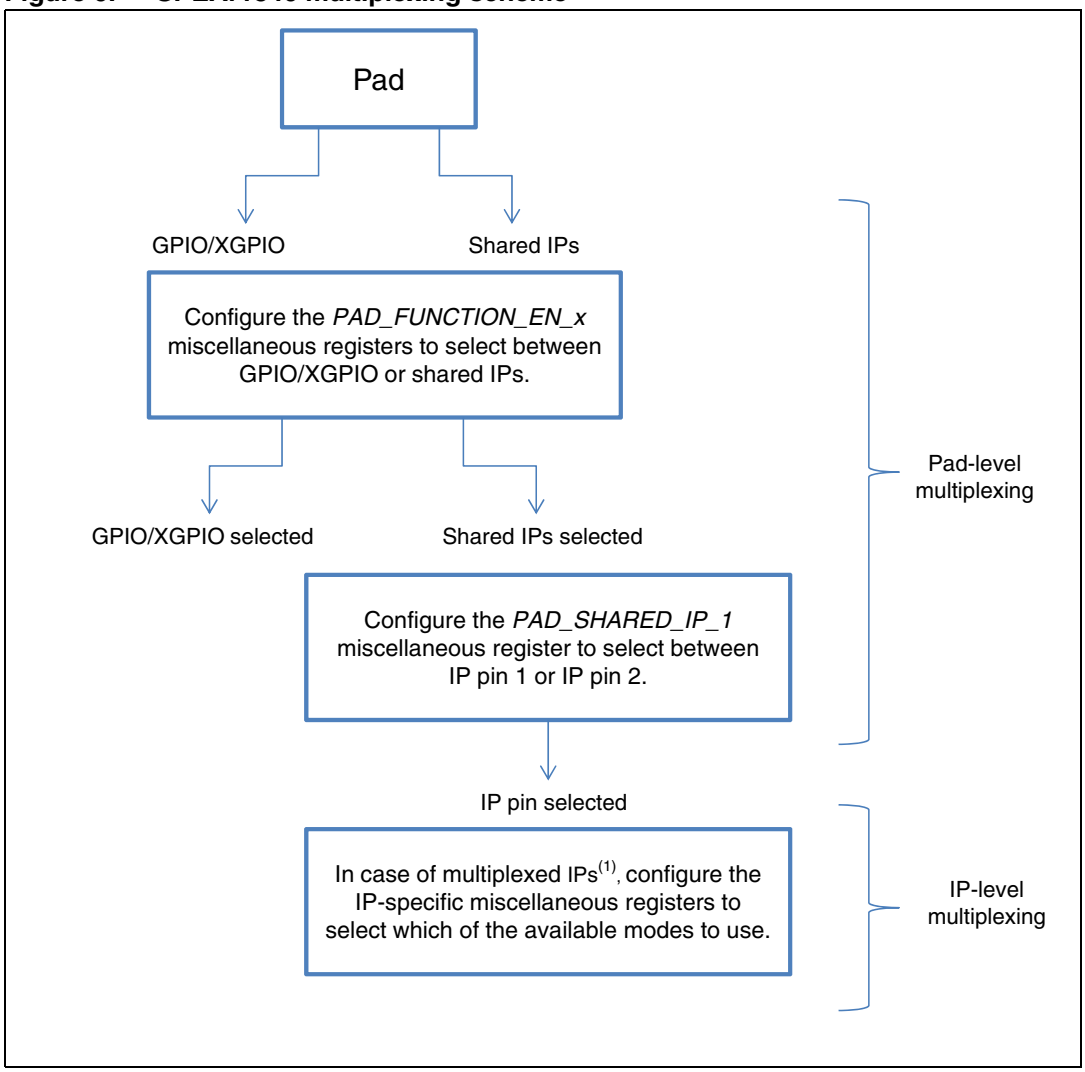
Table 3 provides a detailed description of SPEAr1340 pads and their terminal characteristics.

Two levels of multiplexing are available:

- Pad-level multiplexing
- IP-level multiplexing

Figure 6 shows an overview of SPEAr1340 multiplexing scheme.

Figure 6. SPEAr1340 multiplexing scheme



1. The multiplexed IPs are: GMAC, Keyboard, MCIF and FSMC. See *Section 3.4: Multiplexed signals description* for more details.

Table 3. Ball characteristics

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
U3	DDR_ADDR0	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
W2	DDR_ADDR1	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
V2	DDR_ADDR2	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
V3	DDR_ADDR3	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
Y2	DDR_ADDR4	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
W1	DDR_ADDR5	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
Y4	DDR_ADDR6	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
V1	DDR_ADDR7	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
T1	DDR_ADDR8	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
U4	DDR_ADDR9	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AA3	DDR_ADDR10	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
V4	DDR_ADDR11	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AA2	DDR_ADDR12	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
Y1	DDR_ADDR13	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
W4	DDR_ADDR14	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AD3	DDR_RASn	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AD4	DDR_CASn	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AA4	DDR_WEn	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AB3	DDR_CS0n	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
U1	DDR_CS1n	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
Y3	DDR_BA0	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
W3	DDR_BA1	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AA1	DDR_BA2	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
T3	DDR_CKE	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AC3	DDR_ODT0	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
U2	DDR_ODT1	O	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE5	DDR_DM0	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG3	DDR_DM1	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF10	DDR_DM2	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG8	DDR_DM3	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH16	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	na	na	na	na	na	na	na	na
AE3	DDR_DQS0p	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF3	DDR_DQS0n	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH4	DDR_DQS1p	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG4	DDR_DQS1n	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE9	DDR_DQS2p	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF8	DDR_DQS2n	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH10	DDR_DQS3p	IO	SSTL	na	na	na	DDRIO_VDD1 V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AG9	DDR_DQS3n	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG14	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AH14	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AF2	DDR_DQ0	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF4	DDR_DQ1	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF1	DDR_DQ2	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF5	DDR_DQ3	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE1	DDR_DQ4	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE6	DDR_DQ5	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE2	DDR_DQ6	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE4	DDR_DQ7	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH3	DDR_DQ8	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH2	DDR_DQ9	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AH6	DDR_DQ10	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG1	DDR_DQ11	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG5	DDR_DQ12	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG2	DDR_DQ13	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH5	DDR_DQ14	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH1	DDR_DQ15	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE8	DDR_DQ16	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE10	DDR_DQ17	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF7	DDR_DQ18	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE11	DDR_DQ19	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AE7	DDR_DQ20	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF11	DDR_DQ21	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AF6	DDR_DQ22	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AF9	DDR_DQ23	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH9	DDR_DQ24	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH8	DDR_DQ25	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG11	DDR_DQ26	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG6	DDR_DQ27	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG10	DDR_DQ28	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH7	DDR_DQ29	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AH11	DDR_DQ30	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG7	DDR_DQ31	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	I	na	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AG13	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AH13	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AG16	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AH12	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AG15	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AG12	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
AH15	RESERVED	IO	SSTL	na	na	na	DDRIO_VDD1V8_1V5	na	na	na	na	na	na	na	na
T2	DDR_RESETn	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AD2	DDR_CLKM0	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AD1	DDR_CLKP0	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AC2	DDR_CLKM1	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AC1	DDR_CLKP1	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AB2	DDR_CLKM2	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	1	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
AB1	DDR_CLKP2	O	SSTL	na	na	na	DDRIO_VDD1V8_1V5	O	0	na	na	na	DDR2n_DDR3	DDR2n_DDR3	CC6
A4	AIN0	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
B4	AIN1	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
C3	AIN2	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
A3	AIN3	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
A2	AIN4	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
B2	AIN5	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
B3	AIN6	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
C2	AIN7	I	ANA	na	na	na	ADC_AVDD2V5	I	na	na	na	na	na	na	na
AF15	MRESETn	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
AF14	DDR2n_DDR3	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
A1	RTC_XO	IO	OSC	na	na	na	RTC_VDD1V5	na	na	na	na	na	na	na	na
B1	RTC_XI	I	OSC	na	na	na	RTC_VDD1V5	na	na	na	na	na	na	na	na
D1	USB_UHC1_DP	IO	ANA	na	na	na	USB_UHC1_VDD3V3	na	na	na	na	na	na	na	na
D2	USB_UHC1_DM	IO	ANA	na	na	na	USB_UHC1_VDD3V3	na	na	na	na	na	na	na	na
H1	USB_UHC0_DP	IO	ANA	na	na	na	USB_UHC0_VDD3V3	na	na	na	na	na	na	na	na
H2	USB_UHC0_DM	IO	ANA	na	na	na	USB_UHC0_VDD3V3	na	na	na	na	na	na	na	na
F1	USB_UOC_DP	IO	ANA	na	na	na	USB_UOC_VDD3V3	na	na	na	na	na	na	na	na

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
F2	USB_UOC_DM	IO	ANA	na	na	na	USB_UOC_VDD3V3	na	na	na	na	na	na	na	na
F4	USB_UOC_ID	I	ANA	na	na	na	USB_VDD2V5	na	na	na	na	na	na	na	na
F3	USB_UOC_VBUS	IO	ANA	na	na	na	5V	na	na	na	na	na	na	na	na
E1	USB_ANALOG_TEST	IO	ANA	na	na	na	USB_VDD2V5	na	na	na	na	na	na	na	na
A8	MCLK_XO	IO	OSC	na	na	na	MCLK_AVDD3V3	na	na	na	na	na	na	na	na
A7	MCLK_XI	I	OSC	na	na	na	MCLK_AVDD3V3	na	na	na	na	na	na	na	na
M2	MIPHY0_TXp	O	ANA	na	na	na	MIPHY0_VDDT1V2	na	na	na	na	na	na	na	na
M1	MIPHY0_TXn	O	ANA	na	na	na	MIPHY0_VDDT1V2	na	na	na	na	na	na	na	na
K2	MIPHY0_RXp	I	ANA	na	na	na	MIPHY0_VDDR1V2	na	na	na	na	na	na	na	na
K1	MIPHY0_RXn	I	ANA	na	na	na	MIPHY0_VDDR1V2	na	na	na	na	na	na	na	na
P2	MIPHY0_XTAL1	I	OSC	na	na	na	MIPHY0_VDDPLL1V2	na	na	na	na	na	na	na	na
P1	MIPHY0_XTAL2	IO	OSC	na	na	na	MIPHY0_VDDPLL1V2	na	na	na	na	na	na	na	na
AF13	TEST0	I	IOTYPE1	PD	10ma	FAST	IO_VDD3V3	I	L	PD	10ma	FAST	3V3	3V3	CC1
AF12	TEST1	I	IOTYPE1	PD	10ma	FAST	IO_VDD3V3	I	L	PD	10ma	FAST	3V3	3V3	CC1
AE14	TEST2	I	IOTYPE1	PD	10ma	FAST	IO_VDD3V3	I	L	PD	10ma	FAST	3V3	3V3	CC1
AE13	TEST3	I	IOTYPE1	PD	10ma	FAST	IO_VDD3V3	I	L	PD	10ma	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AE12	TEST4	I	IOTYPE1	PD	10ma	FAST	IO_VDD3V3	I	L	PD	10ma	FAST	3V3	3V3	CC1
AE15	BSD_TRSTn ARM_TRSTn	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
AD16	BSD_TCK ARM_TCK	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
AE16	BSD_TMS ARM_TMS	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
AD15	BSD_TDI ARM_TDI	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC1
AF16	BSD_TDO ARM_TDO	IO	IOTYPE1	Deact	10ma	FAST	IO_VDD3V3	I	na	Deact	10ma	FAST	3V3	3V3	CC1
A13	USB_UOC_DRVVBUS	O	IOTYPE1	Deact	10ma	FAST	IO_VDD3V3	I	na	Deact	10ma	FAST	3V3	3V3	CC2
B13	USB_UHC0_DRVVBUS	O	IOTYPE1	Deact	10ma	FAST	IO_VDD3V3	O	0	Deact	10ma	FAST	3V3	3V3	CC2
C13	USB_UHC1_DRVVBUS	O	IOTYPE1	Deact	10ma	FAST	IO_VDD3V3	O	0	Deact	10ma	FAST	3V3	3V3	CC2
D13	USB_UHC0_OVERCUR	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC2
E13	USB_UHC1_OVERCUR	I	IOTYPE1	PU	10ma	FAST	IO_VDD3V3	I	na	PU	10ma	FAST	3V3	3V3	CC2
A12	FSMC_IO8 KBD_ROW0 XGPIO0	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
B12	FSMC_IO9 KBD_ROW1 XGPIO1	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
C12	FSMC_IO10 KBD_ROW2 XGPIO2	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
D12	FSMC_IO11 KBD_ROW3 XGPIO3	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
E12	FSMC_IO12 KBD_ROW4 XGPIO4	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
A11	FSMC_IO13 KBD_ROW5 XGPIO5	IO IOD IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
B11	FSMC_IO14 KBD_COL0 XGPIO6	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
C11	FSMC_IO15 KBD_COL1 XGPIO7	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
D11	FSMC_CE1n KBD_COL2 GPIO_A0	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
E11	FSMC_RWPRT1n KBD_COL3 GPIO_A1	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4
A10	FSMC_RSTPWDWN1 KBD_COL4 GPIO_A2	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3V3	I	na	PU	6ma	FAST	1V8	STRAP5	CC4

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AF17	UART0_RTSn GPT1_TMR_CPT2 GPIO_A3	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG17	UART0_RIn GPT0_TMR_CPT2 GPIO_A4	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH17	UART0_DSRn GPT1_TMR_CLK1 GPIO_A5	I O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE17	UART0_DTRn GPT1_TMR_CPT1 GPIO_A6	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG18	UART0_DCDn GPT1_TMR_CLK2 GPIO_A7	I O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF18	UART0_CTSn GPT0_TMR_CLK1 GPIO_B0	I O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE18	PWM2 KBD_COL5 GPIO_B1 GPIO_WKUP_TRIG	O IO IO I	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH18	I2C1_SDA GPIO_B2	IOD IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD17	SPDIF_IN GPIO_B3	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AD18	VIP_B15 CAM4_VSYNC GPIO_B4	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF19	PWM3 GPT0_TMR_CPT1 GPIO_B5 DDRPHY_VDD1V2_OFF	O I IO O	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG19	PWM4 GPT0_TMR_CLK2 GPIO_B6 DDRIO_VDD1V8_1V5_OFF	O O IO O	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH19	I2C1_SCL GPIO_B7	IOD IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE19	PWM1 SSP_SS1n XGPIO24 STRAP0	O O IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH20	VIP_B10 CAM4_PIXCLK XGPIO25 STRAP1	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD19	VIP_B11 CAM4_HSYNC XGPIO26 STRAP2	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AD20	VIP_B12 CAM4_DATA0 XGPIO27 STRAP3	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE20	VIP_B13 CAM4_DATA1 XGPIO28 STRAP4	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF20	VIP_B14 CAM4_DATA2 XGPIO29 STRAP5	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG20	VIP_B9 CAM4_DATA3 XGPIO30 STRAP6	I I IO S	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD21	VIP_B8 CAM4_DATA7 XGPIO31	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE21	VIP_G15 CAM4_DATA6 XGPIO32	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF21	VIP_G14 CAM4_DATA5 XGPIO33	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AG21	VIP_G13 CAM4_DATA4 XGPIO34	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH21	VIP_G12 XGPIO35	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD22	VIP_B4 XGPIO36	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE22	VIP_B3 XGPIO37	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF22	VIP_R4 XGPIO38	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH22	VIP_R3 CAM3_PIXCLK XGPIO39	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG22	VIP_G11 XGPIO40	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD23	VIP_B5 XGPIO41	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE23	VIP_B2 XGPIO42	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF23	VIP_R5 XGPIO43	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG23	VIP_R2 CAM3_HSYNC XGPIO44	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AH23	VIP_G10 CAM3_DATA7 XGPIO45	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH24	VIP_B6 CAM3_DATA5 XGPIO46	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG24	VIP_B1 CAM3_DATA3 XGPIO47	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF24	VIP_R6 CAM3_DATA0 XGPIO48	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE24	VIP_R1 CAM3_VSYNC XGPIO49	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH25	VIP_G9 CAM3_DATA6 XGPIO50	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG25	VIP_B7 CAM3_DATA4 XGPIO51	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF25	XGPIO52 VIP_B0 CAM3_DATA2	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE25	VIP_R7 CAM3_DATA1 XGPIO53	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AH26	VIP_R0 CAM2_PIXCLK XGPIO54	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG26	VIP_G8 CAM2_DATA7 XGPIO55	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF26	VIP_R8 CAM2_DATA5 XGPIO56	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH27	XGPIO57 VIP_G7 CAM2_DATA3	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AH28	VIP_G0 CAM2_DATA0 XGPIO58	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG27	VIP_DE CAM2_HSYNC XGPIO59	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AG28	VIP_R15 CAM2_DATA6 XGPIO60	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF27	VIP_R9 CAM2_DATA4 XGPIO61	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AF28	VIP_G6 CAM2_DATA2 XGPIO62	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AE26	VIP_G1 CAM2_DATA1 XGPIO63	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE27	VIP_VSYNC CAM2_VSYNC XGPIO64	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AE28	VIP_R14 CAM1_DATA7 XGPIO65	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD24	VIP_R10 CAM1_DATA4 XGPIO66	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD25	VIP_G5 CAM1_DATA2 XGPIO67	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD26	VIP_G2 CAM1_DATA0 XGPIO68	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD28	VIP_PIXCLK CAM1_PIXCLK XGPIO69	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AD27	VIP_R13 CAM1_DATA6 XGPIO70	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AC24	VIP_R11 CAM1_DATA3 XGPIO71	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AC25	VIP_G4 CAM1_DATA1 XGPIO72	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AC26	VIP_G3 CAM1_VSYNC XGPIO73	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AC27	VIP_HSYNC CAM1_HSYNC XGPIO74	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AC28	VIP_R12 CAM1_DATA5 XGPIO75	I I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AB24	SMI_DATAOUT XGPIO76	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AB25	SMI_DATAIN XGPIO77	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AB28	SMI_CLK XGPIO78	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AB26	SMI_CS1n XGPIO79	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AB27	SSP_SS0n XGPIO80	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AA24	SSP_MOSI XGPIO81	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AA25	SSP_MISO XGPIO82	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AA26	SSP_SCK XGPIO83	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AA27	SMI_CS0n XGPIO84	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
AA28	TOUCH_XY_SEL SSP_SS2n XGPIO85	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
Y24	UART0_TXD XGPIO86	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
Y25	UART0_RXD XGPIO87	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
Y26	UART1_TXD XGPIO88	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
Y27	UART1_RXD XGPIO89	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
Y28	I2S_IN_DATA3 XGPIO90	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
W24	I2S_IN_DATA2 XGPIO91	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
W25	I2S_IN_DATA1 XGPIO92	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
W26	I2S_IN_DATA0 XGPIO93	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
V24	I2S_IN_WS XGPIO94	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
V25	I2S_OUT_DATA2 XGPIO95	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
V26	I2S_OUT_DATA0 XGPIO96	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
W27	I2S_OUT_BITCLK XGPIO97	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
U24	I2S_OUT_WS XGPIO98	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
W28	I2S_IN_BITCLK XGPIO99	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
U25	I2S_OUT_DATA3 XGPIO100	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
U26	I2S_OUT_DATA1 XGPIO101	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
V27	I2S_OUT_REFCLK(1) XGPIO102	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
V28	I2S_OUT_OVRSAMP_CLK XGPIO103	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC1
U28	MAC_TXCLK XGPIO104	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
U27	MAC_TXD0 XGPIO105	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
T26	MAC_TXD1 XGPIO106	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
T27	MAC_TXD2 XGPIO107	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
T28	MAC_GTXCLK125 XGPIO108	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
T25	MAC_TXD3 XGPIO109	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
R25	MAC_TXD4 XGPIO110	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
R26	MAC_TXD5 XGPIO111	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
R27	MAC_RXD0 XGPIO112	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
R28	MAC_GTXCLK XGPIO113	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
R24	MAC_RXD1 XGPIO114	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
P26	MAC_TXD6 XGPIO115	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
P27	MAC_TXD7 XGPIO116	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
P28	MAC_RXCLK XGPIO117	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
P25	MAC_RXD2 XGPIO118	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
N24	MAC_RXD3 XGPIO119	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
N25	MAC_RXD4 XGPIO120	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
N26	MAC_RXD5 XGPIO121	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
N27	MAC_MDC XGPIO122	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
N28	MAC_MDIO XGPIO123	IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
M24	MAC_RXD6 XGPIO124	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
M25	MAC_RXD7 XGPIO125	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
M26	MAC_COL XGPIO126	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
M27	MAC_RXDV XGPIO127	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
M28	MAC_RXER XGPIO128	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
L24	MAC_TXEN XGPIO129	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
L25	MAC_TXER XGPIO130	O IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
L26	MAC_CRS XGPIO131	I IO	IOTYPE3	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD2V5_3 V3	I	na	PU	6ma	FAST	2V5	STRAP6	CC5
L27	SSP_SS3n XGPIO132	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
K27	I2C0_SDA XGPIO133	IOD IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
L28	I2C0_SCL XGPIO134	IOD IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
K25	CEC0 XGPIO135	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
K24	CEC1 XGPIO136	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
K26	SPDIF_OUT XGPIO137	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
J24	LCD_B6 XGPIO138	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
J28	LCD_B5 XGPIO139	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
J27	LCD_B4 XGPIO140	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
J26	LCD_B3 XGPIO141	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
J25	LCD_B2 XGPIO142	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
H28	LCD_XR6 XGPIO143	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
H27	LCD_B7 XGPIO144	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
H26	LCD_B0 XGPIO145	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
H25	LCD_B1 XGPIO146	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
H24	LCD_G3 XGPIO147	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
G28	LCD_XR5 XGPIO148	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
G27	LCD_XR2 XGPIO149	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
G26	LCD_G7 XGPIO150	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
G25	LCD_G5 XGPIO151	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
G24	LCD_G2 XGPIO152	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
F28	LCD_XR4 XGPIO153	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
F27	LCD_XR1 XGPIO154	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
F26	LCD_G6 XGPIO155	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
F25	LCD_G4 XGPIO156	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E28	LCD_G1 XGPIO157	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E27	LCD_XR3 ARM_TRCCLK XGPIO158	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E26	LCD_XR0 ARM_TRCCTL XGPIO159	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E25	LCD_G0 ARM_TRCDATA0 XGPIO160	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D28	LCD_R5 ARM_TRCDATA1 XGPIO161	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
F24	LCD_R2 ARM_TRCDATA2 XGPIO162	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C28	LCD_DE ARM_TRCDATA3 XGPIO163	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B28	LCD_PE ARM_TRCDATA4 XGPIO164	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
A28	LCD_R7 ARM_TRCDATA5 XGPIO165	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D27	LCD_R4 ARM_TRCDATA6 XGPIO166	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C27	LCD_R1 ARM_TRCDATA7 XGPIO167	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B27	LCD_VSYNC ARM_TRCDATA8 XGPIO168	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
K28	LCD_PCLK ARM_TRCDATA9 XGPIO169(2)	O	IOTYPE4	PU/ PD	8 mA	na	IO_VDD3V3	I	na	PU	8mA	na	3V3	3V3	CC2
A27	LCD_R6 ARM_TRCDATA10 XGPIO170	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A26	LCD_R3 ARM_TRCDATA11 XGPIO171	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B26	LCD_R0 ARM_TRCDATA12 XGPIO172	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C26	LCD_HSYNC ARM_TRCDATA13 XGPIO173	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
D26	LCD_XR7 ARM_TRCDATA14 XGPIO174	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A25	LCD_XG0 ARM_TRCDATA15 XGPIO175	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B25	LCD_XG1 ARM_TRCDATA16 XGPIO176	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C25	LCD_XG2 ARM_TRCDATA17 XGPIO177	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D25	LCD_LED_PWM ARM_TRCDATA18 XGPIO178	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A24	LCD_XG3 ARM_TRCDATA19 XGPIO179	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B24	LCD_XG4 ARM_TRCDATA20 XGPIO180	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C24	LCD_XG5 ARM_TRCDATA21 XGPIO181	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D24	LCD_XG6 ARM_TRCDATA22 XGPIO182	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
E24	LCD_XG7 ARM_TRCDATA23 XGPIO183	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A23	LCD_XB0 ARM_TRCDATA24 XGPIO184	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B23	LCD_XB1 ARM_TRCDATA25 XGPIO185	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C23	LCD_XB2 ARM_TRCDATA26 XGPIO186	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D23	LCD_XB3 ARM_TRCDATA27 XGPIO187	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E23	LCD_XB4 ARM_TRCDATA28 XGPIO188	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A22	LCD_XB5 ARM_TRCDATA29 XGPIO189	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B22	LCD_XB6 ARM_TRCDATA30 XGPIO190	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C22	LCD_XB7 ARM_TRCDATA31 XGPIO191	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
D22	FSMC_AD25 XGPIO192	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E22	FSMC_AD20 MCIF_DATA15 XGPIO193	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A21	FSMC_AD21 MCIF_DATA14 XGPIO194	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B21	FSMC_AD22 MCIF_DATA13 XGPIO195	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C21	FSMC_AD23 MCIF_DATA12 XGPIO196	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D21	FSMC_AD24 MCIF_DATA11 XGPIO197	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E21	FSMC_AD13 MCIF_nCS1 XGPIO198	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A20	FSMC_AD14 MCIF_nDMACK_nWP XGPIO199	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B20	FSMC_AD15 MCIF_DATA10 XGPIO200	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
C20	FSMC_AD18 MCIF_DATA9 XGPIO201	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D20	FSMC_AD19 MCIF_DATA8 XGPIO202	O IO IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E20	FSMC_AD8 MCIF_nIOWR_nWE XGPIO203	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A19	FSMC_AD9 MCIF_nRESET_CF XGPIO204	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B19	FSMC_AD10 MCIF_nCS0_nCE XGPIO205	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C19	FSMC_AD11 MCIF_CF_INTR XGPIO206	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D19	FSMC_AD12 MCIF_IORDY XGPIO207	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E19	FSMC_AD3 MCIF_nCE_SD_MMC XGPIO208	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A18	FSMC_AD4 MCIF_nCD_CF1 XGPIO209	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
B18	FSMC_AD5 MCIF_nCD_CF2 XGPIO210	O I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C18	FSMC_AD6 MCIF_DATA_DIR XGPIO211	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D18	FSMC_AD7 MCIF_nIORD_nRE XGPIO212	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E18	MCIF_ADDR0_ALE XGPIO213	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A17	MCIF_nCD_xD XGPIO214	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B17	FSMC_AD0 MCIF_ADDR2 XGPIO215	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C17	FSMC_AD1 MCIF_nCE_CF XGPIO216	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D17	FSMC_AD2 MCIF_nCE_xD XGPIO217	O O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E17	MCIF_SD_CMD XGPIO218	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A16	MCIF_LEDS XGPIO219	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
B16	MCIF_DATA1 XGPIO220	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C16	MCIF_DATA2 XGPIO221	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D16	MCIF_DATA3 XGPIO222	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E16	MCIF_DATA6 XGPIO223	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B15	MCIF_DATA7 XGPIO224	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A15	MCIF_ADDR1_CLE_CLK XGPIO225	O IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C15	MCIF_nCD_SD_MMC XGPIO226	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
D15	MCIF_DMARQ_RnB_WP XGPIO227	I IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
E15	MCIF_DATA1_SD XGPIO228	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A14	MCIF_DATA2_SD XGPIO229	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B14	MCIF_DATA3_SD XGPIO230	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
C14	MCIF_DATA4 XGPIO231	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
D14	MCIF_DATA5 XGPIO232	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
B10	FSMC_IO2 XGPIO233	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C10	FSMC_IO1 XGPIO234	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
D10	FSMC_IO0 XGPIO235	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
E10	FSMC_RSTPWDWN0 XGPIO236	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
E14	MCIF_DATA0 XGPIO237	IO	IOTYPE1	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD3V3	I	na	PU	6mA	FAST	3V3	3V3	CC2
A9	FSMC_IO7 XGPIO238	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
B9	FSMC_IO6 XGPIO239	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C9	FSMC_IO5 XGPIO240	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
D9	FSMC_IO4 XGPIO241	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
E9	FSMC_IO3 XGPIO242	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C8	FSMC_ALE_AD17 XGPIO243	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
D8	FSMC_REn XGPIO244	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
E8	FSMC_WEn XGPIO245	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C7	FSMC_RWPRT0n XGPIO246	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
D7	FSMC_RB0 XGPIO247	IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
E7	FSMC_CLE_AD16 XGPIO248	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C6	FSMC_CE0n XGPIO249	O IO	IOTYPE2	PU/ PD	4/6/8/ 10mA	SLOW /FAST	IO_VDD1V8_3 V3	I	na	PU	6ma	FAST	1V8	STRAP4	CC3
C1	RTC_VDD1V5	PWR													
K13 K17 L10 L12 L14 L16 L18 M11 M17 M19 N10 N12 N18 P11 P17	VDD1V2	PWR													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
R10 R12 R18 T11 T17 T19 U18 V15 V17 V19 W14 W16 W18 M4	VDD1V2	PWR													
U10 U12 V11 V13 W10 W12	DDRPHY_VDD1V2	PWR													
T6 U5 V6 W5 Y6 AA5 AB6 AC7 AC9 AC11 AC13 AD6 AD8 AD10	DDRIO_VDD1V8_1V5	PWR													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AD12 AD14	DDRIO_VDD1V8_1V5	PWR													
C4	ADC_AVDD2V5	PWR													
F14 F15 F17 F18 F20 F21 F23 G23 J23 W23 AA23 AC23 AC19 AC17 AC15 U23	IO_VDD3V3	PWR													
F8 F9	IO_VDD1V8_3V3	PWR													
F11 F12	IO_VDD1V8_3V3_1	PWR													
L23 N23 R23 T24 P24	IO_VDD2V5_3V3	PWR													
N2	MIPHY0_VDDPLL1V2	PWR													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
P3	MIPHY0_VDD2PLL2V5	PWR													
L3	MIPHY0_VDDR1V2	PWR													
N1	MIPHY0_VDDT1V2	PWR													
E6	PLL1_AVDD2V5	PWR													
D6	PLL1_VDD1V2	PWR													
E4	PLL2_AVDD2V5	PWR													
D4	PLL2_VDD1V2	PWR													
N5	PLL3_AVDD2V5	PWR													
P6	PLL3_VDD1V2	PWR													
AC5	DDR_PLL_AVDD2V5	PWR													
U19	OTP_VDD2V5	PWR													
B7	MCLK_AVDD1V2	PWR													
B8	MCLK_AVDD3V3	PWR													
K4	USB_UHC0_VDD1V2	PWR													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
J4	USB_UHC0_VDD2V5	PWR													
J3	USB_UHC0_VDD3V3	PWR													
E2	USB_UHC1_VDD1V2	PWR													
E3	USB_UHC1_VDD2V5	PWR													
D3	USB_UHC1_VDD3V3	PWR													
H4	USB_UOC_VDD1V2	PWR													
G3	USB_UOC_VDD2V5	PWR													
G2	USB_UOC_VDD3V3	PWR													
M6	VREG1_2V5_OUT	O	REG OUT												
K6	VREG1_3V3_IN	PWR													
F6	VREG2_2V5_OUT	O	REG OUT												
H6	VREG2_3V3_IN	PWR													
R5	MIPHY0_VREG_3V3_IN	PWR													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
A6 B6 D5 E5 F5 F7 F10 F13 F16 F19 F22 G4 G5 G6 H5 H23 J5 J6 K5 K10 K16 K18 K23 L4 L5 L6 L11 L13 L15 L17 M5 M10 M12 M13 M14 M15 M16 M18 M23 N4 N6 N11	gnd	GND													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
N13 N14 N15 N16 N17 N19 R2 P5 P10 P12 P13 P14 P15 P16 P18 P23 R4 R6 R11 R13 R14 R15 R16 R17 T4 T5 T10 T12 T13 T14 T15 T16 T18 U6 U11 U13	gnd	GND													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
U14 U15 U16 U17 T23 V5 V10 V12 V14 V16 V18 V23 W6 W11 W13 W15 W17 W19 Y5 Y23 AA6 AB4 AB5 AB23 AC6 AC8 AC10 AC12 AC14 AC16 AC18 AC20 AD7	gnd	GND													

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
AD9 AD11 AD13	gnd	GND													
P4	MIPHY0_VSSPLL	GND													
J1 J2 K3 L1 L2 M3 R3	MIPHY0_VSSR	GND													
N3	MIPHY0_VSST	GND													
H3	USB_VSSAC	GND													
C5	ADC_AGND	GND													
A5	ADC_VREFP	I	ANA REF												
B5	ADC_VREFN	I	ANA REF												
AC4	DDRIO_VREF	I	ANA REF												
AD5	DDRIO_COMP_REXT	IO	ANA REF												
AC21	IO_COMP_REXT1_3V3	IO	ANA REF												
AC22	IO_COMP_GND1_3V3	GND	DED GND												

Table 3. Ball characteristics (continued)

Ball	Pin name	Pad type and pad options						Reset/Reset rel. state					Reset mode	Reset rel. mode	Compensation cell
		Signal type	Pin type	PU/ PD	Drive	Slew	Supply name	Direction	Out value	PU/ PD	Drive	Slew			
K19	IO_COMP_REXT2_3V3	IO	ANA REF												
L19	IO_COMP_GND2_3V3	GND	DED GND												
K12	IO_COMP_REXT1_1V8_3V3	IO	ANA REF												
K11	IO_COMP_GND1_1V8_3V3	GND	DED GND												
K15	IO_COMP_REXT2_1V8_3V3	IO	ANA REF												
K14	IO_COMP_GND2_1V8_3V3	GND	DED GND												
P19	IO_COMP_REXT_2V5_3V3	IO	ANA REF												
R19	IO_COMP_GND_2V5_3V3	GND	DED GND												
R1	MIPHY0_REF	IO	ANA REF												
G1	USB_TXRTUNE	IO	ANA REF												

1. This is the input reference clock for I2S output functional block.
2. The XGPIO169 is the only XGPIO pin which is always an output. All the other XGPIO pins are IO.

3.3 Power supply signals description

Table 4. Power supply signals description

Pin name	Description	Ball	Signal type	Pin type
ADC_AGND	ADC ground	C5	GND	
ADC_AVDD2V5	ADC power supply	C4	PWR	
ADC_VREFN	ADC negative voltage reference	B5	I	ANA REF
ADC_VREFP	ADC positive voltage reference	A5	I	ANA REF
DDR_PLL_AVDD2V5	DDR PLL power supply	AC5	PWR	
DDRIO_COMP_REXT	DDR IO compensation cell analog reference	AD5	IO	ANA REF
DDRIO_VDD1V8_1V5	DDR IO power supply	T6 U5 V6 W5 Y6 AA5 AB6 AC7 AC9 AC11 AC13 AD6 AD8 AD10 AD12 AD14	PWR	
DDRIO_VREF	DDR IO voltage reference	AC4	I	ANA REF
DDRPHY_VDD1V2	DDR PHY power supply	U10 U12 V11 V13 W10 W12	PWR	
IO_COMP_GND_2V5_3V3	IOTYPE3 IO compensation cell ground	P19	GND	DED GND
IO_COMP_GND1_1V8_3V3	IOTYPE2 IO compensation cell ground	K11	GND	DED GND
IO_COMP_GND1_3V3	IOTYPE1 & IOTYPE4 IO compensation cell ground	AC22	GND	DED GND
IO_COMP_GND2_1V8_3V3	IOTYPE2 IO compensation cell ground	K14	GND	DED GND
IO_COMP_GND2_3V3	IOTYPE1 & IOTYPE4 IO compensation cell ground	L19	GND	DED GND
IO_COMP_REXT_2V5_3V3	IOTYPE3 IO compensation cell analog reference	R19	IO	ANA REF
IO_COMP_REXT1_1V8_3V3	IOTYPE2 IO compensation cell analog reference	K12	IO	ANA REF
IO_COMP_REXT1_3V3	IOTYPE1 & IOTYPE4 IO compensation cell analog reference	AC21	IO	ANA REF
IO_COMP_REXT2_1V8_3V3	IOTYPE2 IO compensation cell analog reference	K15	IO	ANA REF
IO_COMP_REXT2_3V3	IOTYPE1 & IOTYPE4 IO compensation cell analog reference	K19	IO	ANA REF

Table 4. Power supply signals description (continued)

Pin name	Description	Ball	Signal type	Pin type
IO_VDD1V8_3V3	IOTYPE2 IO power supply	F8 F9	PWR	
IO_VDD1V8_3V3_1	IOTYPE2 IO power supply	F11 F12	PWR	
IO_VDD2V5_3V3	IOTYPE3 IO power supply	L23 N23 R23 T24 P24	PWR	
IO_VDD3V3	IOTYPE1 & IOTYPE4 IO power supply	F14 F15 F17 F18 F20 F21 F23 G23 J23 W23 AA23 AC23 AC19 AC17 AC15 U23	PWR	
MCLK_AVDD1V2	Master clock oscillator power supply	B7	PWR	
MCLK_AVDD3V3	Master clock oscillator power supply	B8	PWR	
MIPHY0_REF	MIPHY analog reference	R1	IO	ANA REF
MIPHY0_VDD2PLL2V5	MIPHY PLL power supply	P3	PWR	
MIPHY0_VDDPLL1V2	MIPHY PLL power supply	N2	PWR	
MIPHY0_VDDR1V2	MIPHY receiver power supply	L3	PWR	
MIPHY0_VDDT1V2	MIPHY transmitter power supply	N1	PWR	
MIPHY0_VREG_3V3_IN	MIPHY voltage regulator power supply	R5	PWR	
MIPHY0_VSSPLL	MIPHY PLL ground	P4	GND	
MIPHY0_VSSR	MIPHY receiver ground	J1 J2 K3 L1 L2 M3 R3	GND	
MIPHY0_VSST	MIPHY transmitter ground	N3	GND	
OTP_VDD2V5	OTP antifuses power supply	U19	PWR	
PLL1_AVDD2V5	PLL1 power supply	E6	PWR	
PLL1_VDD1V2	PLL1 power supply	D6	PWR	
PLL2_AVDD2V5	PLL2 power supply	E4	PWR	
PLL2_VDD1V2	PLL2 power supply	D4	PWR	
PLL3_AVDD2V5	PLL3 power supply	N5	PWR	
PLL3_VDD1V2	PLL3 power supply	P6	PWR	
RTC_VDD1V5	Real time clock power supply	C1	PWR	

Table 4. Power supply signals description (continued)

Pin name	Description	Ball	Signal type	Pin type
USB_TXRTUNE	USB PHY analog reference	G1	IO	ANA REF
USB_UHC0_VDD1V2	USB PHY Host 0 power supply	K4	PWR	
USB_UHC0_VDD2V5	USB PHY Host 0 power supply	J4	PWR	
USB_UHC0_VDD3V3	USB PHY Host 0 power supply	J3	PWR	
USB_UHC1_VDD1V2	USB PHY Host 1 power supply	E2	PWR	
USB_UHC1_VDD2V5	USB PHY Host 1 power supply	E3	PWR	
USB_UHC1_VDD3V3	USB PHY Host 1 power supply	D3	PWR	
USB_UOC_VDD1V2	USB PHY OTG power supply	H4	PWR	
USB_UOC_VDD2V5	USB PHY OTG power supply	G3	PWR	
USB_UOC_VDD3V3	USB PHY OTG power supply	G2	PWR	
USB_VSSAC	USB PHY ground	H3	GND	
VDD1V2	Core power supply	K13 K17 L10 L12 L14 L16 L18 M11 M17 M19 N10 N12 N18 P11 P17 R10 R12 R18 T11 T17 T19 U18 V15 V17 V19 W14 W16 W18 M4	PWR	
VREG1_2V5_OUT	Voltage regulator 1 output	M6	O	REG OUT
VREG1_3V3_IN	Voltage regulator 1 power supply	K6	PWR	
VREG2_2V5_OUT	Voltage regulator 2 output	F6	O	REG OUT

Table 4. Power supply signals description (continued)

Pin name	Description	Ball	Signal type	Pin type
VREG2_3V3_IN	Voltage regulator 2 power supply	H6	PWR	
gnd	Ground	A6 B6 D5 E5 F5 F7 F10 F13 F16 F19 F22 G4 G5 G6 H5 H23 J5 J6 K5 K10 K16 K18 K23 L4 L5 L6 L11 L13 L15 L17 M5 M10 M12 M13 M14 M15 M16 M18 M23 N4 N6 N11 N13 N14 N15 N16 N17 N19 R2 P5 P10 P12 P13 P14 P15 P16 P18 P23 R4 R6 R11 R13 R14 R15 R16 R17 T4 T5 T10 T12 T13 T14 T15 T16 T18 U6 U11 U13 U14 U15 U16 U17 T23 V5 V10 V12 V14 V16 V18 V23 W6 W11 W13 W15 W17 W19 Y5 Y23 AA6 AB4 AB5 AB23 AC6 AC8 AC10 AC12 AC14 AC16 AC18 AC20 AD7 AD9 AD11 AD13	GND	

3.4 Multiplexed signals description

3.4.1 MAC Ethernet port multiplexing scheme

Table 5. MAC Ethernet port multiplexing scheme

Ball	MAC							
	GMII		MII		RGMII		RMII	
T28	MAC_GTXCLK125	I	-	-	MAC_GTXCLK125	I	MAC_GTXCLK125	I
R28	MAC_GTXCLK	O	-	-	MAC_GTXCLK	O	MAC_GTXCLK	O
U28	-	-	MAC_TXCLK	I	-	-	-	-
U27	MAC_TXD0	O	MAC_TXD0	O	MAC_TXD0	O	MAC_TXD0	O
T26	MAC_TXD1	O	MAC_TXD1	O	MAC_TXD1	O	MAC_TXD1	O
T27	MAC_TXD2	O	MAC_TXD2	O	MAC_TXD2	O	-	-
T25	MAC_TXD3	O	MAC_TXD3	O	MAC_TXD3	O	-	-
R25	MAC_TXD4	O	-	-	-	-	-	-
R26	MAC_TXD5	O	-	-	-	-	-	-
P26	MAC_TXD6	O	-	-	-	-	-	-
P27	MAC_TXD7	O	-	-	-	-	-	-
L24	MAC_TXEN	O	MAC_TXEN	O	MAC_TXEN	O	MAC_TXEN	O
L25	MAC_TXER	O	MAC_TXER	O	-	-	-	-
P28	MAC_RXCLK	I	MAC_RXCLK	I	MAC_RXCLK	I	-	-
M27	MAC_RXDV	I	MAC_RXDV	I	MAC_RXDV	I	MAC_RXDV	I
M28	MAC_RXER	I	MAC_RXER	I	-	-	-	-
R27	MAC_RXD0	I	MAC_RXD0	I	MAC_RXD0	I	MAC_RXD0	I
R24	MAC_RXD1	I	MAC_RXD1	I	MAC_RXD1	I	MAC_RXD1	I
P25	MAC_RXD2	I	MAC_RXD2	I	MAC_RXD2	I	-	-
N24	MAC_RXD3	I	MAC_RXD3	I	MAC_RXD3	I	-	-
N25	MAC_RXD4	I	-	-	-	-	-	-
N26	MAC_RXD5	I	-	-	-	-	-	-
M24	MAC_RXD6	I	-	-	-	-	-	-
M25	MAC_RXD7	I	-	-	-	-	-	-
M26	MAC_COL	I	MAC_COL	I	-	-	-	-
L26	MAC_CRS	I	MAC_CRS	I	-	-	-	-
N27	MAC_MDC	O	MAC_MDC	O	MAC_MDC	O	MAC_MDC	O
N28	MAC_MDIO	IO	MAC_MDIO	IO	MAC_MDIO	IO	MAC_MDIO	IO

3.4.2 KBD multiplexing scheme

Table 6. KBD multiplexing scheme

Ball	Signal name	GPIO	Keyboard 6x6	Keyboard 2x2
A11	KBD_ROW5	KBD_ROW5	Keyboard Output (ROW5)	
E12	KBD_ROW4	KBD_ROW4	Keyboard Output (ROW4)	
D12	KBD_ROW3	KBD_ROW3	Keyboard Output (ROW3)	
C12	KBD_ROW2	KBD_ROW2	Keyboard Output (ROW2)	
B12	KBD_ROW1	KBD_ROW1	Keyboard Output (ROW1)	Keyboard Output (ROW1)
A12	KBD_ROW0	KBD_ROW0	Keyboard Output (ROW0)	Keyboard Output (ROW0)
AE18	KBD_COL5	KBD_COL5	Keyboard Input (COL5)	
A10	KBD_COL4	KBD_COL4	Keyboard Input (COL4)	
E11	KBD_COL3	KBD_COL3	Keyboard Input (COL3)	
D11	KBD_COL2	KBD_COL2	Keyboard Input (COL2)	
C11	KBD_COL1	KBD_COL1	Keyboard Input (COL1)	Keyboard Input (COL1)
B11	KBD_COL0	KBD_COL0	Keyboard Input (COL0)	Keyboard Input (COL0)

3.4.3 MCIF multiplexing scheme

Table 7. MCIF multiplexing scheme

Ball	Signal name	Asynchronous card				Synchronous card	
		Compact Flash		xD card		SD/SDIO/MMC	
E14	MCIF_DATA0	MCIF_DATA0	IO	MCIF_DATA0	IO	MCIF_DATA0	IO
B16	MCIF_DATA1	MCIF_DATA1	IO	MCIF_DATA1	IO	-	-
C16	MCIF_DATA2	MCIF_DATA2	IO	MCIF_DATA2	IO	-	-
D16	MCIF_DATA3	MCIF_DATA3	IO	MCIF_DATA3	IO	-	-
C14	MCIF_DATA4	MCIF_DATA4	IO	MCIF_DATA4	IO	MCIF_DATA4	IO
D14	MCIF_DATA5	MCIF_DATA5	IO	MCIF_DATA5	IO	MCIF_DATA5	IO
E16	MCIF_DATA6	MCIF_DATA6	IO	MCIF_DATA6	IO	MCIF_DATA6	IO
B15	MCIF_DATA7	MCIF_DATA7	IO	MCIF_DATA7	IO	MCIF_DATA7	IO
E15	MCIF_DATA1_SD	-	-	-	-	MCIF_DATA1_SD	IO
A14	MCIF_DATA2_SD	-	-	-	-	MCIF_DATA2_SD	IO
B14	MCIF_DATA3_SD	-	-	-	-	MCIF_DATA3_SD	IO

Table 7. MCIF multiplexing scheme (continued)

Ball	Signal name	Asynchronous card				Synchronous card	
		Compact Flash		xD card		SD/SDIO/MMC	
D21	MCIF_DATA8	MCIF_DATA8	IO	-	-	-	-
C21	MCIF_DATA9	MCIF_DATA9	IO	-	-	-	-
B21	MCIF_DATA10	MCIF_DATA10	IO	-	-	-	-
A21	MCIF_DATA11	MCIF_DATA11	IO	-	-	-	-
E22	MCIF_DATA12	MCIF_DATA12	IO	-	-	-	-
E15	MCIF_DATA13	MCIF_DATA13	IO	-	-	-	-
A14	MCIF_DATA14	MCIF_DATA14	IO	-	-	-	-
B14	MCIF_DATA15	MCIF_DATA15	IO	-	-	-	-
E18	MCIF_ADDR0_ALE	MCIF_ADDR0_ALE	O	MCIF_ADDR0_ALE	O	-	-
A15	MCIF_ADDR1_CLE_CLK	MCIF_ADDR1_CLE_CLK	O	MCIF_ADDR1_CLE_CLK	O	MCIF_ADDR1_CLE_CLK	O
B17	MCIF_ADDR2	MCIF_ADDR2	O	-	-	-	-
C17	MCIF_nCE_CF	MCIF_nCE_CF	O	-	-	-	-
D17	MCIF_nCE_xD	-	-	MCIF_nCE_xD	O		-
E19	MCIF_nCE_SD_MMC	-	-	-	-	MCIF_nCE_SD_MMC	O
A18	MCIF_nCD_CF1	MCIF_nCD_CF1	I	-	-	-	-
B18	MCIF_nCD_CF2	MCIF_nCD_CF2	I	-	-	-	-
A17	MCIF_nCD_xD			MCIF_nCD_xD	I	-	-
C15	MCIF_nCD_SD_MMC	-	-	-	-	MCIF_nCD_SD_MMC	I
C18	MCIF_DATA_DIR	MCIF_DATA_DIR	O	MCIF_DATA_DIR	O	MCIF_DATA_DIR	O
D15	MCIF_DMARQ_RnB_WP	MCIF_DMARQ_RnB_WP	I	MCIF_DMARQ_RnB_WP	I	MCIF_DMARQ_RnB_WP	I
D18	MCIF_nIORD_nRE	MCIF_nIORD_nRE	O	MCIF_nIORD_nRE	O	-	-
E20	MCIF_nIOWR_nWE	MCIF_nIOWR_nWE	O	MCIF_nIOWR_nWE	O	-	-
A19	MCIF_nRESET_CF	MCIF_nRESET_CF	O	-		-	-
B19	MCIF_nCS0_nCE	MCIF_nCS0_nCE	O	MCIF_nCS0_nCE	O	-	-
C19	MCIF_CF_INTR	MCIF_CF_INTR	I	-		-	-
D19	MCIF_IORDY	MCIF_IORDY	I	-		-	-
E21	MCIF_nCS1	MCIF_nCS1	O	-	-	-	-
A20	MCIF_nDMACK_nWP	MCIF_nDMACK_nWP	O	MCIF_nDMACK_nWP	O	-	-
E17	MCIF_SD_CMD	-	-	-	-	MCIF_SD_CMD	IO
A16	MCIF_LEDS	MCIF_LEDS	O	MCIF_LEDS	O	MCIF_LEDS	O

3.4.4 FSMC multiplexing scheme

Table 8. FSMC multiplexing scheme

Ball	Signal name	NAND		NOR		Asynchronous SRAM	
D10	FSMC_IO0	FSMC_IO0	IO	FSMC_IO0	IO	FSMC_IO0	IO
C10	FSMC_IO1	FSMC_IO1	IO	FSMC_IO1	IO	FSMC_IO1	IO
B10	FSMC_IO2	FSMC_IO2	IO	FSMC_IO2	IO	FSMC_IO2	IO
E9	FSMC_IO3	FSMC_IO3	IO	FSMC_IO3	IO	FSMC_IO3	IO
D9	FSMC_IO4	FSMC_IO4	IO	FSMC_IO4	IO	FSMC_IO4	IO
C9	FSMC_IO5	FSMC_IO5	IO	FSMC_IO5	IO	FSMC_IO5	IO
B9	FSMC_IO6	FSMC_IO6	IO	FSMC_IO6	IO	FSMC_IO6	IO
A9	FSMC_IO7	FSMC_IO7	IO	FSMC_IO7	IO	FSMC_IO7	IO
A12	FSMC_IO8	FSMC_IO8	IO	FSMC_IO8	IO	FSMC_IO8	IO
B12	FSMC_IO9	FSMC_IO9	IO	FSMC_IO9	IO	FSMC_IO9	IO
C12	FSMC_IO10	FSMC_IO10	IO	FSMC_IO10	IO	FSMC_IO10	IO
D12	FSMC_IO11	FSMC_IO11	IO	FSMC_IO11	IO	FSMC_IO11	IO
E12	FSMC_IO12	FSMC_IO12	IO	FSMC_IO12	IO	FSMC_IO12	IO
A11	FSMC_IO13	FSMC_IO13	IO	FSMC_IO13	IO	FSMC_IO13	IO
B11	FSMC_IO14	FSMC_IO14	IO	FSMC_IO14	IO	FSMC_IO14	IO
C11	FSMC_IO15	FSMC_IO15	IO	FSMC_IO15	IO	FSMC_IO15	IO
C6	FSMC_CE0n	FSMC_CE0n	O	FSMC_CE0n	O	FSMC_CE0n	O
E8	FSMC_WEn	FSMC_WEn	O	FSMC_WEn	O	FSMC_WEn	O
D8	FSMC_REn	FSMC_REn	O	FSMC_REn	O	FSMC_REn	O
C8	FSMC_ALE_AD17	FSMC_ALE_AD17	O	FSMC_ALE_AD17	O	FSMC_ALE_AD17	O
E7	FSMC_CLE_AD16	FSMC_CLE_AD16	O	FSMC_CLE_AD16	O	FSMC_CLE_AD16	O
D7	FSMC_RB0	FSMC_RB0	I	FSMC_AV	O	FSMC_BL0n	O
C7	FSMC_RWPRT0n	FSMC_RWPRT0n	O	FSMC_RWPRT0n	O	FSMC_BL1n	O
B17	FSMC_AD0			FSMC_AD0	O	FSMC_AD0	O
C17	FSMC_AD1			FSMC_AD1	O	FSMC_AD1	O
D17	FSMC_AD2			FSMC_AD2	O	FSMC_AD2	O
E19	FSMC_AD3			FSMC_AD3	O	FSMC_AD3	O
A18	FSMC_AD4			FSMC_AD4	O	FSMC_AD4	O
B18	FSMC_AD5			FSMC_AD5	O	FSMC_AD5	O
C18	FSMC_AD6			FSMC_AD6	O	FSMC_AD6	O
D18	FSMC_AD7			FSMC_AD7	O	FSMC_AD7	O
E20	FSMC_AD8			FSMC_AD8	O	FSMC_AD8	O
A19	FSMC_AD9			FSMC_AD9	O	FSMC_AD9	O

Table 8. FSMC multiplexing scheme (continued)

Ball	Signal name	NAND		NOR		Asynchronous SRAM	
B19	FSMC_AD10			FSMC_AD10	O	FSMC_AD10	O
C19	FSMC_AD11			FSMC_AD11	O	FSMC_AD11	O
D19	FSMC_AD12			FSMC_AD12	O	FSMC_AD12	O
E21	FSMC_AD13			FSMC_AD13	O	FSMC_AD13	O
A20	FSMC_AD14			FSMC_AD14	O	FSMC_AD14	O
B20	FSMC_AD15			FSMC_AD15	O	FSMC_AD15	O
C20	FSMC_AD18			FSMC_AD18	O	FSMC_AD18	O
D20	FSMC_AD19			FSMC_AD19	O	FSMC_AD19	O
E22	FSMC_AD20			FSMC_AD20	O	FSMC_AD20	O
A21	FSMC_AD21			FSMC_AD21	O	FSMC_AD21	O
B21	FSMC_AD22			FSMC_AD22	O	FSMC_AD22	O
C21	FSMC_AD23			FSMC_AD23	O	FSMC_AD23	O
D21	FSMC_AD24			FSMC_AD24	O	FSMC_AD24	O
D22	FSMC_AD25			FSMC_AD25	O	FSMC_AD25	O
D11	FSMC_CE1n	FSMC_CE1n	O	FSMC_CE1n	O	FSMC_CE1n	O
E11	FSMC_RWPRT1n	FSMC_RWPRT1n	O	FSMC_RWPRT1n	O		
E10	FSMC_RSTPWDN0			FSMC_RSTPWDN0	O		
A10	FSMC_RSTPWDN1	FSMC_RB1	I	FSMC_RSTPWDN1	O		

3.5 Signals description

3.5.1 CPU subsystem

Table 9. CPU subsystem - A9SM signals description

Signal name	Description	Type	Ball
ARM_TRSTn	JTAG reset	I	AE15
ARM_TCK	JTAG clock	I	AD16
ARM_TMS	JTAG mode select	I	AE16
ARM_TDI	JTAG data input	I	AD15
ARM_TDO	JTAG data output	IO	AF16
ARM_TRCCLK	Trace clock	O	E27
ARM_TRCCTL	Trace control	O	E26
ARM_TRCDATA0	Trace data	O	E25
ARM_TRCDATA1			D28
ARM_TRCDATA2			F24
ARM_TRCDATA3			C28
ARM_TRCDATA4			B28
ARM_TRCDATA5			A28
ARM_TRCDATA6			D27
ARM_TRCDATA7			C27
ARM_TRCDATA8			B27
ARM_TRCDATA9			K28
ARM_TRCDATA10			A27
ARM_TRCDATA11			A26
ARM_TRCDATA12			B26
ARM_TRCDATA13			C26
ARM_TRCDATA14			D26
ARM_TRCDATA15			A25
ARM_TRCDATA16			B25
ARM_TRCDATA17			C25
ARM_TRCDATA18			D25
ARM_TRCDATA19			A24
ARM_TRCDATA20			B24
ARM_TRCDATA21			C24
ARM_TRCDATA22			D24
ARM_TRCDATA23			E24

Table 9. CPU subsystem - A9SM signals description (continued)

Signal name	Description	Type	Ball
ARM_TRCDATA24	Trace data	O	A23
ARM_TRCDATA25			B23
ARM_TRCDATA26			C23
ARM_TRCDATA27			D23
ARM_TRCDATA28			E23
ARM_TRCDATA29			A22
ARM_TRCDATA30			B22
ARM_TRCDATA31			C22

3.5.2 Memories

Table 10. Memories - MPMC signals description

Signal name	Description	Type	Ball
DDR2n_DDR3	This pin is used to select the DDR2 or DDR3 operation mode for DDR2/3 buffers. 0 DDR2 selection 1 DDR3 selection	I	AF14
DDR_ADDR0	Memory address bus	O	U3
DDR_ADDR1			W2
DDR_ADDR2			V2
DDR_ADDR3			V3
DDR_ADDR4			Y2
DDR_ADDR5			W1
DDR_ADDR6			Y4
DDR_ADDR7			V1
DDR_ADDR8			T1
DDR_ADDR9			U4
DDR_ADDR10			AA3
DDR_ADDR11			V4
DDR_ADDR12			AA2
DDR_ADDR13			Y1
DDR_ADDR14			W4
DDR_RASn	Memory row address select (active low)	O	AD3
DDR_CASn	Memory columns address select (active low)	O	AD4
DDR_WEn	Memory write transfer cycle (active low)	O	AA4
DDR_CS0n	Memory chip select 0 (active low)	O	AB3

Table 10. Memories - MPMC signals description (continued)

Signal name	Description	Type	Ball
DDR_CS1n	Memory chip select 1 (active low)	O	U1
DDR_BA0	Memory bank address	O	Y3
DDR_BA1			W3
DDR_BA2			AA1
DDR_CKE	Memory clock enable (active high)	O	T3
DDR_ODT0	Memory ODT signal	O	AC3
DDR_ODT1			U2
DDR_DM0	Memory data mask (active high)	O	AE5
DDR_DM1			AG3
DDR_DM2			AF10
DDR_DM3			AG8
DDR_DQS0p	Differential memory data strobe active high; drove during write transaction and received from memory device during read during transfer	IO	AE3
DDR_DQS1p			AH4
DDR_DQS2p			AE9
DDR_DQS3p			AH10
DDR_DQS0n	Differential memory data strobe active low; drove during write transaction and received from memory device during read during transfer	IO	AF3
DDR_DQS1n			AG4
DDR_DQS2n			AF8
DDR_DQS3n			AG9
DDR_DQ0	Memory data bus	IO	AF2
DDR_DQ1			AF4
DDR_DQ2			AF1
DDR_DQ3			AF5
DDR_DQ4			AE1
DDR_DQ5			AE6
DDR_DQ6			AE2
DDR_DQ7			AE4
DDR_DQ8			AH3
DDR_DQ9			AH2
DDR_DQ10			AH6
DDR_DQ11			AG1
DDR_DQ12			AG5
DDR_DQ13			AG2

Table 10. Memories - MPMC signals description (continued)

Signal name	Description	Type	Ball
DDR_DQ14	Memory data bus	IO	AH5
DDR_DQ15			AH1
DDR_DQ16			AE8
DDR_DQ17			AE10
DDR_DQ18			AF7
DDR_DQ19			AE11
DDR_DQ20			AE7
DDR_DQ21			AF11
DDR_DQ22			AF6
DDR_DQ23			AF9
DDR_DQ24			AH9
DDR_DQ25			AH8
DDR_DQ26			AG11
DDR_DQ27			AG6
DDR_DQ28			AG10
DDR_DQ29			AH7
DDR_DQ30			AH11
DDR_DQ31			AG7
DDR_RESETn	Memory reset (active low)	O	T2
DDR_CLKM0	Differential memory clock (active low)	O	AD2
DDR_CLKM1			AC2
DDR_CLKM2			AB2
DDR_CLKP0	Differential memory clock (active high)	O	AD
DDR_CLKP1			AC1
DDR_CLKP2			AB1

Table 11. Memories - FSMC signals description

Signal name	Description	Type	Ball
FSMC_IO0	Data bus	IO	D10
FSMC_IO1			C10
FSMC_IO2			B10
FSMC_IO3			E9
FSMC_IO4			D9
FSMC_IO5			C9
FSMC_IO6			B9
FSMC_IO7			A9
FSMC_IO8			A12
FSMC_IO9			B12
FSMC_IO10			C12
FSMC_IO11			D12
FSMC_IO12			E12
FSMC_IO13			A11
FSMC_IO14			B11
FSMC_IO15			C11
FSMC_AD0	Address bus	O	B17
FSMC_AD1			C17
FSMC_AD2			D17
FSMC_AD3			E19
FSMC_AD4			A18
FSMC_AD5			B18
FSMC_AD6			C18
FSMC_AD7			D18
FSMC_AD8			E20
FSMC_AD9			A19
FSMC_AD10			B19
FSMC_AD11			C19
FSMC_AD12			D19
FSMC_AD13			E21
FSMC_AD14			A20
FSMC_AD15			B20
FSMC_AD18			C20
FSMC_AD19			D20
FSMC_AD20			E22

Table 11. Memories - FSMC signals description (continued)

Signal name	Description	Type	Ball
FSMC_AD21	Address bus	O	A21
FSMC_AD22			B21
FSMC_AD23			C21
FSMC_AD24			D21
FSMC_AD25			D22
FSMC_CE0n[1]	NAND/NOR/SRAM chip select (default NAND)	O	C6
FSMC_CE1n			D11
FSMC_WEn	Write enable	O	E8
FSMC_REn	Read enable	O	D8
FSMC_ALE_AD17	Address latch enable /address pin #17	O	C8
FSMC_CLE_AD16	Command latch enable / address pin #16	O	E7
FSMC_RB0	NAND ready/busy[0] or NOR address valid or SRAM byte lane[0] (valid only for 16-bit configuration)	IO	D7
FSMC_RSTPWDWN1	NAND ready/busy[1] or NOR reset power down[1]	IO	A10
FSMC_RWPRT0n	NAND/NOR write protect [0] or SRAM byte lane[1] (valid only for 16-bit configuration)	O	C7
FSMC_RWPRT1n	NAND/NOR write protect [1]		E11
FSMC_RSTPWDWN0	NOR reset / Power down [0]	O	E10

1. FSMC_CE0n is used for booting from Parallel NOR or NAND Flash.

Table 12. Memories - SMI signals description

Signal name	Description	Type	Ball
SMI_DATAIN	Data in from external serial Flash	I	AB25
SMI_DATAOUT	Data out to external serial Flash	O	AB24
SMI_CLK	Data out clock to external Flash	O	AB28
SMI_CS0n[1]	Chip selects (active low)	O	AA27
SMI_CS1n			AB26

1. SMI_CS0n is used for booting from Serial NOR.

3.5.3 Clocks and resets

Table 13. Main clock and reset pins descriptions

Signal name	Description	Type	Ball
MCLK_XI	Master clock (MCLK) 24 MHz (typical) crystal in	OSC	A7
MCLK_XO	Master clock (MCLK) 24 MHz (typical) crystal out		A8
RTC_XI	Real-time clock (RTC) 32 kHz crystal in	OSC	B1
RTC_XO	Real-time clock (RTC) 32 kHz crystal out		A1
MRESETn	Main reset	IOTYPE1	AF15

3.5.4 Debug interface

Table 14. Debug pins description

Signal name	Description	Type	Ball
ARM_TRSTn	Test reset input	I	AE15
ARM_TCK	Test trace clock	I	AD16
ARM_TDI	Test trace data input	I	AD15
ARM_TMS	Test trace mode select	I	AE16
ARM_TDO	Test trace data output	IO	AF16

Note: 1 The ARM Trace ports are enabled via the miscellaneous registers.

2 For ARM JTAG mode, the TEST[4:0] pins should be set to “00001” at power-up. For functional mode, the same pins should be set to “00000”.

3 When the 2V5 power supply is not present on the OTP supply ball, the JTAG debug features are not available on the device.

3.5.5 Connectivity

Table 15. Connectivity - MAC PHY interface signals description

Signal name	Description	Type	Ball
MAC_GTXCLK125	Auxiliary source of clock	I	T28
MAC_GTXCLK	Transmission clock This is the transmission clock provided by the external PHY/oscillator/internal PLL for the RGMII,GMII, RMII. All the RGMII,GMII, RMII transmission signals generated by the MAC are synchronous to this clock. RMII: this clock is used also as receive clock, so all the receive signals are synchronous to this clock.	O	R28
MAC_TXCLK	Transmission clock This is the transmission clock (25/2.5 MHz in 100M/10Mbps) provided by the external PHY for the MII. All the MII transmission signals generated by the MAC are synchronous to this clock.	I	U28
MAC_TXD0	PHY transmit data This is a bundle of eight transmit data signals driven by the MAC. It has multiple functions depending on which PHY interface is selected, as given below. Unused bits in the RGMII,RMII,MII interface configurations are tied to low. – GMII: All 8 bits provide the GMII transmit data byte. The validity of the data is qualified with MAC_TXEN and MAC_TXER. *Note: Using 10/100 Mbps-only operation, MAC_TXD bus is only 4 bits wide (MAC_TXD[3:0]).* – MII: Bits [3:0] provide the MII transmit data nibble. The validity of the data is qualified with MAC_TXEN and MAC_TXER. – RGMII: Bits [3:0] provide the RGMII transmit data. The data bus changes with both rising and falling edges of the transmit clock. The validity of the data is qualified with MAC_TXEN. – RMII: Bits [1:0] provide the RMII transmit data. The validity of the data is qualified with MAC_TXEN.	O	U27
MAC_TXD1			T26
MAC_TXD2			T27
MAC_TXD3			T25
MAC_TXD4			R25
MAC_TXD5			R26
MAC_TXD6			P26
MAC_TXD7			P27
MAC_TXEN	PHY transmit data enable This signal is driven by the MAC and has multiple functions depending on which PHY interface is selected, as given below. – GMII/MII/RMII: When high, indicates that valid data is being transmitted on the MAC_TXD bus. – RGMII: This signal is the control signal for the transmit data, and is driven on both edges of the clock.	O	L24
MAC_TXER	PHY transmit error This signal is driven by the MAC and has multiple functions depending on which PHY interface is selected, as given below. – GMII/MII: When high, indicates a transmit error or carrier extension (in GMII) on the MAC_TXD bus. – RMII, RGMII: Not used. Tied low in some configurations; driven low in others.	O	L25

Table 15. Connectivity - MAC PHY interface signals description (continued)

Signal name	Description	Type	Ball
MAC_RXCLK	Reception clock (rmii_clk) This is the reception clock (125/25/2.5 MHz in 1G/100M/10Mbps) provided by the external PHY for RGMII,GMII,MII. All the RGMII,GMII,MII receive signals received by the MAC are synchronous to this clock.	I	P28
MAC_RXDV	PHY receive data valid This signal is driven by PHY and has multiple functions depending on which PHY interface is selected as given below. – GMII/MII: When high, indicates that data on the MAC_RXD bus is valid. It remains asserted continuously from the first recovered byte/nibble of the frame through the final recovered byte/nibble. – RGMII: This is the receive control signal used to qualify the data received on MAC_RXD bus. This signal is sampled on both edges of the clock. – RMII: Contains the crs and data valid information of the receive interface.	I	M27
MAC_RXER	PHY receive error This signal is driven by the PHY and has multiple functions depending on which PHY interface is selected as given below. – GMII/MII: When high, indicates an error or carrier extension (in GMII) in the received frame on the MAC_RXD bus. – RGMII/RMII: Not used.	I	M28
MAC_RXD0	PHY receive data This is a bundle of eight data signals received from the PHY. It has multiple functions depending on which PHY interface is selected, as given below. – GMII: All 8 bits provide the GMII receive data byte. The validity of the data is qualified with MAC_RXDV and MAC_RXER. Note: Using 10/100 Mbps-only operation, MAC_RXD bus is only 4 bits wide (MAC_RXD[3:0]). – MII: Bits [3:0] provide the MII receive data nibble. The validity of the data is qualified with MAC_RXDV and MAC_RXER. – RGMII: Bits [3:0] provide the RGMII receive data. The data bus is sampled with both rising and falling edges of the receive clock (MAC_RXCLK). The validity of the data is qualified with MAC_RXDV. – RMII: Bits [1:0] provide the RMII receive data. The validity of the data is qualified with MAC_RXDV.	I	R27
MAC_RXD1			R24
MAC_RXD2			P25
MAC_RXD3			N24
MAC_RXD4			N25
MAC_RXD5			N26
MAC_RXD6			M24
MAC_RXD7			M25
MAC_COL	PHY collision This signal, valid only in GMII/MII mode, is asserted by the PHY when a collision is detected on the medium. This signal is not synchronous to any clock.(Active high)	I	M26
MAC_CRS	PHY CRS This signal, valid only in GMII/MII mode, is asserted by the PHY when either the transmit or receive medium is not idle. The PHY deasserts this signal when both transmit and receive medium are idle. This signal is not synchronous to any clock. (active high)	I	L26

Table 15. Connectivity - MAC PHY interface signals description (continued)

Signal name	Description	Type	Ball
MAC_MDC	Management data clock The MAC provides timing reference for the MAC_MDIO signal through this aperiodic clock. The maximum frequency of this clock is 2.5 MHz.This clock is generated from the application clock (HCLK) via a clock divider.	O	N27
MAC_MDIO	Management data input/output.	IO	N28

Table 16. Connectivity - PCIe/SATA physical interface (MIPHY) signals description (1)

Signal name	Description	Type	Ball
MIPHY single lane			
MIPHY0_TXp	Positive TX output	O	M2
MIPHY0_TXn	Negative TX output	O	M1
MIPHY0_RXp	Positive RX input	I	K2
MIPHY0_RXn	Negative RX input	I	K1
MIPHY0_XTAL1	Input of the crystal oscillator	I	P2
MIPHY0_XTAL2		IO	P1

1. PCIe and SATA cannot be used simultaneously; one port in alternative to the other one. To select between PCIe or SATA you have to configure the register PCIE_SATA_CFG[0], pcie_sata_sel.

Table 17. Connectivity - USB 2.0 Host signals description

Signal name	Description	Type	Ball
USB_UHC0_DRVVBUS	USB Host 0 VBUS, port power switch	O	B13
USB_UHC1_DRVVBUS	USB Host 1 VBUS, port power switch	O	C13
USB_UHC0_OVERCUR	Port overcurrent indication from application	I	D13
USB_UHC1_OVERCUR		I	E13

Table 18. Connectivity - USB 2.0 OTG signals description

Signal name	Description	Type	Ball
USB_UOC_DRVVBUS	Power switch to 5 V charge pump	O	A13

Table 19. Connectivity - USB 2.0 PHY signals description

Signal name	Description	Type	Ball
USB_UHC0_DP	USB Host 0 D+	IO	H1
USB_UHC0_DM	USB Host 0 D-	IO	H2
USB_UHC1_DP	USB Host 1 D+	IO	D1
USB_UHC1_DM	USB Host 1 D-	IO	D2
USB_UOC_DP	USB OTG D+	IO	F1
USB_UOC_DM	USB OTG D-	IO	F2
USB_UOC_ID	USB OTG mini-receptacle identifier	I	F4
USB_UOC_VBUS	USB OTG power supply pin: – When SPEAr is configured as USB Device, this is a VBUS detect signal. – When SPEAr is configured as USB Host, this is a power supply pin. A charge pump external to the USB PHY must provide power to this pin (and to pin1 of the Micro-USB connector). The nominal voltage for this pin is 5 V. The voltage range is 0-5.25 V.	IO	F3

Table 20. Connectivity - UART signals description

Signal name	Description	Type	Ball
UART0			
UART0_RXD	UART0 receive serial data input IrDA input (SIRIN)	I	Y25
UART0_TXD	UART0 transmitted serial data output IrDA output (SIROUT)	O	Y24
UART0_RTSn	UART0 request to send modem status output (active low)	O	AF17
UART0_CTSn	UART0 clear to send modem status input (active low)	I	AF18
UART0_DCDn	UART0 data carrier detect modem status input (active low)	I	AG18
UART0_DTRn	UART0 data terminal ready modem status output (active low)	O	AE17
UART0_DSRn	UART0 data set ready modem status input (active low)	I	AH17
UART0_RIn	UART0 Ring Indicator modem status input (active low)	I	AG17
UART1			
UART1_RXD	UART1 receive serial data input IrDA input (SIRIN)	I	Y27
UART1_TXD	UART1 transmitted serial data output IrDA output (SIROUT)	O	Y26

Table 21. Connectivity - SSP signals description

Signal name	Description	Type	Ball
SSP_SCK	SSP clock. It is used as output in master mode as input in slave mode	IO	AA26
SSP_MISO	Master input slave output	IO	AA25
SSP_MOSI	Master output slave input	IO	AA24
SSP_SS0n	SSP frame output (master mode), input (slave mode)	IO	AB27
SSP_SS1n	Slave select 1 (used only in master mode)	O	AE19
SSP_SS2n	Slave select 2 (used only in master mode)	O	AA28
SSP_SS3n	Slave select 3 (used only in master mode)	O	L27

Table 22. Connectivity - I2C signals description

Signal name	Description	Type	Ball
I2C0			
I2C0_SDA	I2C0 input/output data	IOD	K27
I2C0_SCL	I2C0 input/output clock	IOD	L28
I2C1			
I2C1_SDA	I2C1 input/output data	IOD	AH18
I2C1_SCL	I2C1 input/output clock	IOD	AH19

Table 23. Connectivity- MCIF signals description

Signal name	Description(1)	Type	Ball
MCIF_DATA0	All modes Data0 line	IO	E14
MCIF_DATA1	Compact Flash (CF)/xD card: Data lines (3 to 1)	IO	B16
MCIF_DATA2		IO	C16
MCIF_DATA3		IO	D16
MCIF_DATA4	MMC8/CF/xD card: Data lines (7 to 4)	IO	C14
MCIF_DATA5		IO	D14
MCIF_DATA6		IO	E16
MCIF_DATA7		IO	B15

Table 23. Connectivity- MCIF signals description (continued)

Signal name	Description[1]	Type	Ball
MCIF_DATA8	Compact Flash (CF): Data lines (15 to 8)	IO	D20
MCIF_DATA9		IO	C20
MCIF_DATA10		IO	B20
MCIF_DATA11		IO	D21
MCIF_DATA12		IO	C21
MCIF_DATA13		IO	B21
MCIF_DATA14		IO	A21
MCIF_DATA15		IO	E22
MCIF_DATA1_SD	SD/SDIO/MMC: Data lines (3 to 1)	IO	E15
MCIF_DATA2_SD		IO	A14
MCIF_DATA3_SD		IO	B14
MCIF_ADDR0_ALE	CF: A0 Address bit 0, used to select one of the eight registers in the task file xD: Address latch enable	O	E18
MCIF_ADDR1_CLE_CLK	CF: A1 Address bit 1, used to select one of the eight registers in the task file xD: Command latch enable SD: SD/SDIO/MMC clock	O	A15
MCIF_ADDR2	CF: A2 Address bit 2, used to select one of the eight registers in the task file	O	B17
MCIF_nCE_CF	CF: Chip enable (active low)	O	C17
MCIF_nCE_xD	xD: Chip enable (active low)	O	D17
MCIF_nCE_SD_MMC	SD: Chip enable (active low)	O	E19
MCIF_nCD_CF1	CF: -CD1, -CD2 These card detect pins are connected to ground on the CF Storage Card or CF+ Card. They are used by the host to determine that the CF Storage Card or CF+ Card is fully inserted into its socket	I	A18
MCIF_nCD_CF2		I	B18
MCIF_nCD_xD	xD: Card insert/remove pin: 0 - Card inserted 1 - Card removed	I	A17
MCIF_nCD_SD_MMC	SD: Card detection for single slot, active low	I	C15
MCIF_DATA_DIR	All modes Data direction on board	O	C18

Table 23. Connectivity- MCIF signals description (continued)

Signal name	Description[1]	Type	Ball
MCIF_DMARQ_RnB_WP	CF: DMARQ A DMA request, asserted by the device when it is ready to transfer data to or from the host. For multiword DMA transfers, the direction of data transfer is controlled by -IORD and -IOWR. The device waits until the host asserts -DMACK before negating DMARQ, and then reasserts DMARQ if there is more data to transfer. DMARQ is not driven when the device is not selected. While a DMA operation is in progress, -CS0 and –CS1 are held negated. xD: Ready/Busy Output from xD Card. SD: Active high. SD card write protect	I	D15
MCIF_nIORD_nRE	CF: -IORD, -HDMARDY, HSTROBE. An IO read strobe (-IORD) generated by the host. This signal gates IO data onto the bus from the CF storage card or CF+ card when the card is configured to use the interface. When in ultra DMA mode, DMA *Read* is active; this signal (-HDMARDY) is asserted by the host to indicate that the host is read to receive Ultra DMA data-in bursts. The host may negate -HDMARDY to pause an ultra DMA transfer. When ub ultra DMA mode, DMA *Write* is active; this signal is the data out strobe (HSTROBE) generated by the host. Both the rising and falling edge of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA dataout burst. xD: Read enable	O	D18
MCIF_nIOWR_nWE	CF: -IOWR, STOP The IO Write strobe (-IOWR) pulse is used to clock IO data on the card data bus into the CF+ card controller registers when the CF+ card is configured to use the IO interface. The clocking occurs on the negative to positive (trailing) edge of the signal. While Ultra DMA mode protocol is active, the assertion of this signal (STOP) causes the termination of the Ultra DMA Burst. This signal must be negated before entering ultra DMA mode protocol. xD Write enable	O	E20
MCIF_nRESET_CF	CF: -RESET Active low hardware reset from the Host	O	A19
MCIF_nCS0_nCE	CF: -CS0 -CS0 is the chip select for the task file registers. While -DMACK is asserted, this signal is held negated. xD: Chip enable	O	B19
MCIF_CF_INTR	CF: INTRQ Active high interrupt request from the device to the Host	I	C19

Table 23. Connectivity- MCIF signals description (continued)

Signal name	Description(1)	Type	Ball
MCIF_IORDY	CF: IORDY, -DDMARDY, DSTROBE Except in Ultra DMA mode, this input signal may be used as IORDY. When in ultra DMA mode, DMA write is active; this signal (-DDMARDY) is asserted by the device to indicate that the device is read to receive Ultra DMA data-in bursts. The device may negate -DDMARDY to pause an ultra DMA transfer. When ultra DMA mode DMA read is active, this signal is the data out strobe (DSTROBE) generated by the device. Both the rising and falling edge of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an ultra DMA data-out burst	I	D19
MCIF_nCS1	CF: -CS1 -CS1 is used to select the alternate status register and the device control register. While -DMACK is asserted, this signal is held negated	O	E21
MCIF_nDMACK_nWP	CF: -DMACK A DMA acknowledge signal that is asserted by the host in response to DMARQ to initiate DMA transfers. When DMA operations are not active, the card ignores the -DMACK signal, including a floating condition. xD: Write protect	O	A20
MCIF_SD_CMD	SD: Command /response line	IO	E17
MCIF_LEDS	All modes Monitors bus activity when data transfer occurs. ***Caution**: do not remove the card while it is being accessed*	O	A16

1. For more details on the use of each signal, please refer to *Table 7: MCIF multiplexing scheme*.

Table 24. Connectivity - KBD signals description

Signal name	Signal type		Description		Ball
	Keyboard	GPIO	Keyboard	GPIO	
KBD_ROW5	OD	IO	Strobe 5, active low	GPIO. Input/Output	A11
KBD_ROW4	OD	IO	Strobe 4, active low		E12
KBD_ROW3	OD	IO	Strobe 3, active low		D12
KBD_ROW2	OD	IO	Strobe 2, active low		C12
KBD_ROW1	OD	IO	Strobe 1, active low		B12
KBD_ROW0	OD	IO	Strobe 0, active low		A12
KBD_COL5	I	IO	Pressed key5, active low		AE18
KBD_COL4	I	IO	Pressed key4, active low		A10

Table 24. Connectivity - KBD signals description (continued)

Signal name	Signal type		Description		Ball
	Keyboard	GPIO	Keyboard	GPIO	
KBD_COL3	I	IO	Pressed key3, active low	GPIO. Input/Output	E11
KBD_COL2	I	IO	Pressed key2, active low		D11
KBD_COL1	I	IO	Pressed key1, active low		C11
KBD_COL0	I	IO	Pressed key0, active low		B11

Table 25. Connectivity - CEC signals description

Signal name	Description	Type	Ball
CEC0			
CEC0	CEC0 RX/TX data	IO	K25
CEC1			
CEC1	CEC1 RX/TX data	IO	K24

3.5.6 Audio

Table 26. Audio - I2S signals description

Signal name	Description	Type	Ball
I2SIN			
I2S_IN_DATA3	Data input for receive mode	I	Y28
I2S_IN_DATA2		I	W24
I2S_IN_DATA1		I	W25
I2S_IN_DATA0		I	W26
I2S_IN_WS	Word select line for receive mode	I	V24
I2S_IN_BITCLK	Serial interface clock	I	W28
I2SOUT			
I2S_OUT_DATA3	Data output for transmit mode	O	U25
I2S_OUT_DATA2		O	V25
I2S_OUT_DATA1		O	U26
I2S_OUT_DATA0		O	V26
I2S_OUT_WS	Word select line for transmit mode - (active high)	O	U24
I2S_OUT_BITCLK	Serial interface clock	O	W27
I2S_OUT_REFCLK	Input reference clock for I2S output functional block (audio crystal)	I	V27
I2S_OUT_OVRSAMP_CLK	Oversampling/reference clock for external audio devices	O	V28

Table 27. Audio - S/PDIF signals description

Signal name	Description	Type	Ball
SPDIF_IN	S/PDIF input	I	AD17
SPDIF_OUT	S/PDIF output	O	K26

3.5.7 Video

Table 28. Video - LCD controller signals description

Signal name	Description	Type	Ball
LCD_R0	Port 1 red data	O	B26
LCD_R1			C27
LCD_R2			F24
LCD_R3			A26
LCD_R4			D27
LCD_R5			D28
LCD_R6			A27
LCD_R7			A28
LCD_G0	Port 1 green data	O	E25
LCD_G1			E28
LCD_G2			G24
LCD_G3			H24
LCD_G4			F25
LCD_G5			G25
LCD_G6			F26
LCD_G7			G26
LCD_B0	Port 1 blue data	O	H26
LCD_B1			H25
LCD_B2			J25
LCD_B3			J26
LCD_B4			J27
LCD_B5			J28
LCD_B6			J24
LCD_B7			H27

Table 28. Video - LCD controller signals description (continued)

Signal name	Description	Type	Ball
LCD_XR0	Port 2 red data	O	E26
LCD_XR1			F27
LCD_XR2			G27
LCD_XR3			E27
LCD_XR4			F28
LCD_XR5			G28
LCD_XR6			H28
LCD_XR7			D26
LCD_XG0	Port 2 green data	O	A25
LCD_XG1			B25
LCD_XG2			C25
LCD_XG3			A24
LCD_XG4			B24
LCD_XG5			C24
LCD_XG6			D24
LCD_XG7			E24
LCD_XB0	Port 2 blue data	O	A23
LCD_XB1			B23
LCD_XB2			C23
LCD_XB3			D23
LCD_XB4			E23
LCD_XB5			A22
LCD_XB6			B22
LCD_XB7			C22
LCD_PCLK	Pixel clock to LCD panel	O	K28
LCD_HSYNC	Horizontal sync pulse	O	C26
LCD_VSYNC	Vertical sync pulse	O	B27
LCD_DE	Data enable	O	C28
LCD_LED_PWM	LCD LED pulse width modulation	O	D25
LCD_PE	Power enable	O	B28

Table 29. Video - VIP signals description

Signal name	Description	Type	Ball
VIP_R0	Red data	I	AH26
VIP_R1			AE24
VIP_R2			AG23
VIP_R3			AH22
VIP_R4			AF22
VIP_R5			AF23
VIP_R6			AF24
VIP_R7			AE25
VIP_R8			AF26
VIP_R9			AF27
VIP_R10	Red data	I	AD24
VIP_R11			AC24
VIP_R12			AC28
VIP_R13			AD27
VIP_R14			AE28
VIP_R15			AG28
VIP_G0	Green data	I	AH28
VIP_G1			AE26
VIP_G2			AD26
VIP_G3			AC26
VIP_G4			AC25
VIP_G5			AD25
VIP_G6			AF28
VIP_G7			AH27
VIP_G8			AG26
VIP_G9			AH25
VIP_G10			AH23
VIP_G11			AG22
VIP_G12			AH21
VIP_G13			AG21
VIP_G14			AF21
VIP_G15			AE21

Table 29. Video - VIP signals description (continued)

Signal name	Description	Type	Ball
VIP_B0	Blue data	I	AF25
VIP_B1			AG24
VIP_B2			AE23
VIP_B3			AE22
VIP_B4			AD22
VIP_B5			AD23
VIP_B6			AH24
VIP_B7			AG25
VIP_B8			AD21
VIP_B9			AG20
VIP_B10			AH20
VIP_B11			AD19
VIP_B12			AD20
VIP_B13	Blue data	I	AE20
VIP_B14			AF20
VIP_B15			AD18
VIP_PIXCLK	Pixel clock from VIP panel	I	AD28
VIP_HSYNC	Horizontal sync pulse	I	AC27
VIP_VSYNC	Vertical sync pulse	I	AE27
VIP_DE	Data enable	I	AG27

Table 30. Video - CAM signals description

Signal name	Description	Type	Ball
CAM1			
CAM1_DATA0	CAM1 data	I	AD26
CAM1_DATA1			AC25
CAM1_DATA2			AD25
CAM1_DATA3			AC24
CAM1_DATA4			AD24
CAM1_DATA5			AC28
CAM1_DATA6			AD27
CAM1_DATA7			AE28
CAM1_PIXCLK	Pixel clock from CAM1 panel	I	AD28
CAM1_VSYNC	CAM1 vertical sync pulse	I	AC26

Table 30. Video - CAM signals description (continued)

Signal name	Description	Type	Ball
CAM1_HSYNC	CAM1 horizontal sync pulse	I	AC27
CAM2			
CAM2_DATA0	CAM2 data	I	AH28
CAM2_DATA1			AE26
CAM2_DATA2			AF28
CAM2_DATA3			AH27
CAM2_DATA4			AF27
CAM2_DATA5			AF26
CAM2_DATA6			AG28
CAM2_DATA7			AG26
CAM2_PIXCLK	Pixel clock from CAM2 panel	I	AH26
CAM2_VSYNC	CAM2 vertical sync pulse	I	AE27
CAM2_HSYNC	CAM2 horizontal sync pulse	I	AG27
CAM3			
CAM3_DATA0	CAM3 data	I	AF24
CAM3_DATA1			AE25
CAM3_DATA2			AF25
CAM3_DATA3	CAM3 data		AG24
CAM3_DATA4			AG25
CAM3_DATA5			AH24
CAM3_DATA6			AH25
CAM3_DATA7			AH23
CAM3_PIXCLK	Pixel clock from CAM3 panel	I	AH22
CAM3_VSYNC	CAM3 vertical sync pulse	I	AE24
CAM3_HSYNC	CAM3 horizontal sync pulse	I	AG23
CAM4			
CAM4_DATA0	CAM4 data	I	AD20
CAM4_DATA1			AE20
CAM4_DATA2			AF20
CAM4_DATA3			AG20
CAM4_DATA4			AG21
CAM4_DATA5			AF21
CAM4_DATA6			AE21
CAM4_DATA7			AD21

Table 30. Video - CAM signals description (continued)

Signal name	Description	Type	Ball
CAM4_PIXCLK	Pixel clock from CAM4 panel	I	AH20
CAM4_VSYNC	CAM4 vertical sync pulse	I	AD18
CAM4_HSYNC	CAM4 horizontal sync pulse	I	AD19

3.5.8 Timers

Table 31. GPT signals description

Signal name	Description	Type	Ball
GPT0			
GPT0_TMR_CPT1	Asynchronous signal provided for the measurement of timing signals in Timer 1	I	AF19
GPT0_TMR_CLK1	This clock toggles each time the Timer 1 interrupt goes active.	O	AF18
GPT0_TMR_CPT2	Asynchronous signal provided for the measurement of timing signals in Timer 2	I	AG17
GPT0_TMR_CLK2	This clock toggles each time the Timer 2 interrupt goes active.	O	AG19
GPT1			
GPT1_TMR_CPT1	Asynchronous signal provided for the measurement of timing signals in Timer 1	I	AE17
GPT1_TMR_CLK1	This clock toggles each time the Timer 1 interrupt goes active.	O	AH17
GPT1_TMR_CPT2	Asynchronous signal provided for the measurement of timing signals in Timer 2	I	AF17
GPT1_TMR_CLK2	This clock toggles each time the Timer 2 interrupt goes active.	O	AG18

3.5.9 Miscellaneous

Table 32. Miscellaneous - ADC signals description

Signal name	Description	Type	Ball
AIN0	Analog inputs #(0..7)	I	A4
AIN1		I	B4
AIN2		I	C3
AIN3		I	A3
AIN4		I	A2
AIN5		I	B2
AIN6		I	B3
AIN7		I	C2
TOUCH_XY_SEL	Touchscreen select	O	AA28

Table 33. Miscellaneous - PWM signals description

Signal name	Description	Type	Ball
PWM1	Channel 1	O	AE19
PWM2	Channel 2	O	AE18
PWM3	Channel 3	O	AF19
PWM4	Channel 4	O	AG19

Table 34. Miscellaneous - GPIO signals description

Signal name	Description	Type	Ball
GPIO_A0	IO data	IO	D11
GPIO_A1		IO	E11
GPIO_A2		IO	A10
GPIO_A3		IO	AF17
GPIO_A4		IO	AG17
GPIO_A5		IO	AH17
GPIO_A6		IO	AE17
GPIO_A7		IO	AG18
GPIO_B0		IO	AF18
GPIO_B1		IO	AE18
GPIO_B2		IO	AH18
GPIO_B3		IO	AD17
GPIO_B4		IO	AD18
GPIO_B5		IO	AF19
GPIO_B6		IO	AG19
GPIO_B7		IO	AH19

Table 35. PCM signals description

Signal name	Description	Type	Ball
GPIO_WKUP_TRIG	Wake-up trigger from GPIO	I	AE18
DDRPHY_VDD1V2_OFF	Controls the (optional) external (i.e. board) power switch on the DDRPHY 1V2 supply line.	O	AF19
DDRIO_VDD1V8_1V5_OFF	Controls the (optional) external (i.e. board) power switch on the DDRPHY 1V5/1V8 supply line.	O	AG19

Table 36. XGPIO signals description

Signal name	Description	Type	Ball
XGPIO0	General purpose IO	IO	A12
XGPIO1		IO	B12
XGPIO2		IO	C12
XGPIO3		IO	D12
XGPIO4		IO	E12
XGPIO5		IO	A11
XGPIO6		IO	B11
XGPIO7		IO	C11

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO24	General purpose IO	IO	AE19
XGPIO25		IO	AH20
XGPIO26		IO	AD19
XGPIO27		IO	AD20
XGPIO28		IO	AE20
XGPIO29		IO	AF20
XGPIO30		IO	AG20
XGPIO31		IO	AD21
XGPIO32		IO	AE21
XGPIO33		IO	AF21
XGPIO34		IO	AG21
XGPIO35		IO	AH21
XGPIO36		IO	AD22
XGPIO37		IO	AE22
XGPIO38		IO	AF22
XGPIO39		IO	AH22
XGPIO40		IO	AG22
XGPIO41		IO	AD23
XGPIO42		IO	AE23
XGPIO43		IO	AF23
XGPIO44		IO	AG23
XGPIO45		IO	AH23
XGPIO46		IO	AH24
XGPIO47		IO	AG24
XGPIO48		IO	AF24
XGPIO49		IO	AE24
XGPIO50		IO	AH25
XGPIO51		IO	AG25
XGPIO52		IO	AF25
XGPIO53		IO	AE25
XGPIO54		IO	AH26
XGPIO55		IO	AG26
XGPIO56		IO	AF26
XGPIO57		IO	AH27
XGPIO58		IO	AH28

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO59	General purpose IO	IO	AG27
XGPIO60		IO	AG28
XGPIO61		IO	AF27
XGPIO62		IO	AF28
XGPIO63		IO	AE26
XGPIO64		IO	AE27
XGPIO65		IO	AE28
XGPIO66		IO	AD24
XGPIO67		IO	AD25
XGPIO68		IO	AD26
XGPIO69		IO	AD28
XGPIO70		IO	AD27
XGPIO71		IO	AC24
XGPIO72		IO	AC25
XGPIO73		IO	AC26
XGPIO74		IO	AC27
XGPIO75		IO	AC28
XGPIO76		IO	AB24
XGPIO77		IO	AB25
XGPIO78		IO	AB28
XGPIO79		IO	AB26
XGPIO80		IO	AB27
XGPIO81		IO	AA24
XGPIO82		IO	AA25
XGPIO83		IO	AA26
XGPIO84		IO	AA27
XGPIO85		IO	AA28
XGPIO86		IO	Y24
XGPIO87		IO	Y25
XGPIO88		IO	Y26
XGPIO89		IO	Y27
XGPIO90		IO	Y28
XGPIO91		IO	W24
XGPIO92		IO	W25
XGPIO93		IO	W26

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO94	General purpose IO	IO	V24
XGPIO95		IO	V25
XGPIO96		IO	V26
XGPIO97		IO	W27
XGPIO98		IO	U24
XGPIO99		IO	W28
XGPIO100		IO	U25
XGPIO101		IO	U26
XGPIO102		IO	V27
XGPIO103		IO	V28
XGPIO104		IO	U28
XGPIO105		IO	U27
XGPIO106		IO	T26
XGPIO107		IO	T27
XGPIO108		IO	T28
XGPIO109		IO	T25
XGPIO110		IO	R25
XGPIO111		IO	R26
XGPIO112		IO	R27
XGPIO113		IO	R28
XGPIO114		IO	R24
XGPIO115		IO	P26
XGPIO116		IO	P27
XGPIO117		IO	P28
XGPIO118		IO	P25
XGPIO119		IO	N24
XGPIO120		IO	N25
XGPIO121		IO	N26
XGPIO122		IO	N27
XGPIO123		IO	N28
XGPIO124		IO	M24
XGPIO125		IO	M25
XGPIO126		IO	M26
XGPIO127		IO	M27
XGPIO128		IO	M28

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO129	General purpose IO	IO	L24
XGPIO130		IO	L25
XGPIO131		IO	L26
XGPIO132		IO	L27
XGPIO133		IO	K27
XGPIO134		IO	L28
XGPIO135		IO	K25
XGPIO136		IO	K24
XGPIO137		IO	K26
XGPIO138		IO	J24
XGPIO139		IO	J28
XGPIO140		IO	J27
XGPIO141		IO	J26
XGPIO142		IO	J25
XGPIO143		IO	H28
XGPIO144		IO	H27
XGPIO145		IO	H26
XGPIO146		IO	H25
XGPIO147		IO	H24
XGPIO148		IO	G28
XGPIO149		IO	G27
XGPIO150		IO	G26
XGPIO151		IO	G25
XGPIO152		IO	G24
XGPIO153		IO	F28
XGPIO154		IO	F27
XGPIO155		IO	F26
XGPIO156		IO	F25
XGPIO157		IO	E28
XGPIO158		IO	E27
XGPIO159		IO	E26
XGPIO160		IO	E25
XGPIO161		IO	D28
XGPIO162		IO	F24
XGPIO163		IO	C28

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO164	General purpose IO	IO	B28
XGPIO165		IO	A28
XGPIO166		IO	D27
XGPIO167		IO	C27
XGPIO168		IO	B27
XGPIO169		O	K28
XGPIO170		IO	A27
XGPIO171		IO	A26
XGPIO172		IO	B26
XGPIO173		IO	C26
XGPIO174		IO	D26
XGPIO175		IO	A25
XGPIO176		IO	B25
XGPIO177		IO	C25
XGPIO178		IO	D25
XGPIO179		IO	A24
XGPIO180		IO	B24
XGPIO181		IO	C24
XGPIO182		IO	D24
XGPIO183		IO	E24
XGPIO184		IO	A23
XGPIO185		IO	B23
XGPIO186		IO	C23
XGPIO187		IO	D23
XGPIO188		IO	E23
XGPIO189		IO	A22
XGPIO190		IO	B22
XGPIO191		IO	C22
XGPIO192		IO	D22
XGPIO193		IO	E22
XGPIO194		IO	A21
XGPIO195		IO	B21
XGPIO196		IO	C21
XGPIO197		IO	D21
XGPIO198		IO	E21

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO199	General purpose IO	IO	A20
XGPIO200		IO	B20
XGPIO201		IO	C20
XGPIO202		IO	D20
XGPIO203		IO	E20
XGPIO204		IO	A19
XGPIO205		IO	B19
XGPIO206		IO	C19
XGPIO207		IO	D19
XGPIO208		IO	E19
XGPIO209		IO	A18
XGPIO210		IO	B18
XGPIO211		IO	C18
XGPIO212		IO	D18
XGPIO213		IO	E18
XGPIO214		IO	A17
XGPIO215		IO	B17
XGPIO216		IO	C17
XGPIO217		IO	D17
XGPIO218		IO	E17
XGPIO219		IO	A16
XGPIO220		IO	B16
XGPIO221		IO	C16
XGPIO222		IO	D16
XGPIO223		IO	E16
XGPIO224		IO	B15
XGPIO225		IO	A15
XGPIO226		IO	C15
XGPIO227		IO	D15
XGPIO228		IO	E15
XGPIO229		IO	A14
XGPIO230		IO	B14
XGPIO231		IO	C14
XGPIO232		IO	D14
XGPIO233		IO	B10

Table 36. XGPIO signals description (continued)

Signal name	Description	Type	Ball
XGPIO234	General purpose IO	IO	C10
XGPIO235		IO	D10
XGPIO236		IO	E10
XGPIO237		IO	E14
XGPIO238		IO	A9
XGPIO239		IO	B9
XGPIO240		IO	C9
XGPIO241		IO	D9
XGPIO242		IO	E9
XGPIO243		IO	C8
XGPIO244		IO	D8
XGPIO245		IO	E8
XGPIO246		IO	C7
XGPIO247		IO	D7
XGPIO248		IO	E7
XGPIO249		IO	C6

3.6 Strapping options

The following two tables show the strapping options available (STRAP[6:0]) on SPEAr1340.

STRAP[6:0] pins are sampled at reset release and they are reusable after the internal latching for different purposes. When used as output pins, these pins require no special conditions, but when used as input pins, the application must keep them in a non-driving (tri-state) mode for at least 2 µs after MRESETn is released.

STRAP[6:0] pins are sampled by internal hardware logic during the power-on reset sequence and latched on the BOOTSTRAP_CFG register in the MISC.

Table 37. Strapping options

Signal name	Description	Type	Ball
STRAP0	The BootROM firmware selects the booting device after reset release by reading the status of the STRAP[3:0] pins.	S	AE19
STRAP1		S	AH20
STRAP2		S	AD19
STRAP3		S	AD20
STRAP4	Used to select the usage of NAND Flash 8-bit interface working as 3V3 or 1V8, along with CE0n: STRAP4= 1 --> 3V3 STRAP4= 0 --> 1V8	S	AE20
STRAP5	Used to select the usage of NAND Flash extension to 16-bit interface and/or second chip select CE1n working as 3V3 or 1V8: STRAP5= 1 --> 3V3 STRAP5= 0 --> 1V8	S	AF20
STRAP6	Used to select the GMII/RGMII interface working at 3V3 or 2V5: STRAP6= 1 --> 2V5 STRAP6= 0 --> 3V3	S	AG20

Table 38. Hardware boot selection (STRAP[0..3])

Primary source	Backup source(1)	STRAP3	STRAP2	STRAP1	STRAP0
Bypass	na	0	0	0	0
Serial NOR Flash(2)	USB OTG (Device)	0	0	0	1
NAND Flash(3)	USB OTG (Device)	0	0	1	0
Parallel NOR Flash (8-bit)(3)	USB OTG (Device)	0	0	1	1
Parallel NOR Flash (16-bit)(3)	USB OTG (Device)	0	1	0	0
UART	na	0	1	0	1
rfu(4)	na	0	1	1	0
rfu	na	0	1	1	1
USB OTG (Device)	na	1	0	0	0
Serial NOR Flash(2)	UART	1	0	0	1
NAND Flash(3)	UART	1	0	1	0

Table 38. Hardware boot selection (STRAP[0..3]) (continued)

Primary source	Backup source(1)	STRAP3	STRAP2	STRAP1	STRAP0
Parallel NOR Flash (8-bit)(3)	UART	1	0	1	1
Parallel NOR Flash (16-bit)(3)	UART	1	1	0	0
MMC/SD memory card	na	1	1	0	1
rfu	na	1	1	1	0
rfu	na	1	1	1	1

1. The backup source will be used in case that the primary source is not available.
2. To boot from serial NOR Flash use SMI_CS0n.
3. To boot from NAND Flash or Parallel NOR Flash use FSMC_CE0n.
4. Reserved for future use.

4 Electrical characteristics

This chapter provides the electrical characteristics for SPEAr1340.

Please refer to *AN3317, Application notes, PCB guidelines for SPEAr1340* for additional details.

4.1 Absolute maximum ratings

SPEAr1340 contains devices to protect the inputs against damage due to high/low static voltages. However, it is advisable to take normal precaution to avoid application of any voltage higher/lower than the specified maximum/minimum rated voltages.

Caution: Stresses above those listed in *Table 39* and *Table 40* may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 39. Voltage absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD} 1V2	1V2 power supply	-0.3	1.44	V
V_{DD} 2V5	2V5 power supply	-0.3	3	
V_{DD} 3V3	3V3 power supply	-0.3	3.9	
V_{DD} RTC	RTC 1V5 power supply	-0.3	2.16	
V_{DD} DDR	DDR2 1V8 power supply	-0.3	2.16	
	DDR3 1V5 power supply	-0.3	2.16	
V_{DD} 1V8/3V3	Programmable 1V8 power supply	-0.3	3.9	
	Programmable 3V3 power supply	-0.3	3.9	
V_{DD} 2V5/3V3	Programmable 2V5 power supply	-0.3	3.9	
	Programmable 3V3 power supply	-0.3	3.9	

Table 40. Thermal absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{STG}	Storage temperature range	-55	150	°C
T_J	Junction temperature	-40	125	

4.2 Recommended operating conditions

To ensure proper operation of the device, it is highly recommended to follow the conditions shown in *Table 41*.

Table 41. Recommended operating conditions

Symbol	Parameter	Ball	Min	Typ	Max	Unit
V_{DD} 1V2	1V2 power supply	K13 K17 L10 L12 L14 L16 L18 M11 M17 M19 N10 N12 N18 P11 P17 R10 R12 R18 T11 T17 T19 U18 V15 V17 V19 W14 W16 W18 M4 U10 U12 V11 V13 W10 W12 N2 L3 N1 D6 D4 P6 K4 E2 H4	1.14	1.2	1.3	V
V_{DD} 2V5	2V5 power supply	C4, P3, E6, E4, N5, AC5, U19, J4, E3, G3	2.25	2.5	2.75	V
V_{DD} 3V3	3V3 power supply	F14 F15 F17 F18 F20 F21 F23 G23 J23 W23 AA23 AC23 AC19 AC17 AC15 U23 B8 J3 D3 G2 K6 H6 R5	3.0	3.3	3.6	V
V_{DD} RTC	RTC 1V5 power supply	C1	1.3	1.5	1.8	V
V_{DD} DDR	DDR2 1V8 power supply	T6 U5 V6 W5 Y6 AA5 AB6 AC7 AC9 AC11 AC13 AD6 AD8 AD10 AD12 AD14	1.7	1.8	1.9	V
	DDR3 1V5 power supply		1.4	1.5	1.6	V
V_{DD} 1V8/3V3	Programmable 1V8 power supply	F8 F9 F11 F12	1.65	1.8	1.95	V
	Programmable 3V3 power supply		3.0	3.3	3.6	V
V_{DD} 2V5/3V3	Programmable 2V5 power supply	L23 N23 R23 T24 P24	2.25	2.5	2.75	V
	Programmable 3V3 power supply		3.0	3.3	3.6	V
T_C	Case temperature	–	-40		85	°C

4.3 Clocking parameters

4.3.1 Master clock (MCLK)

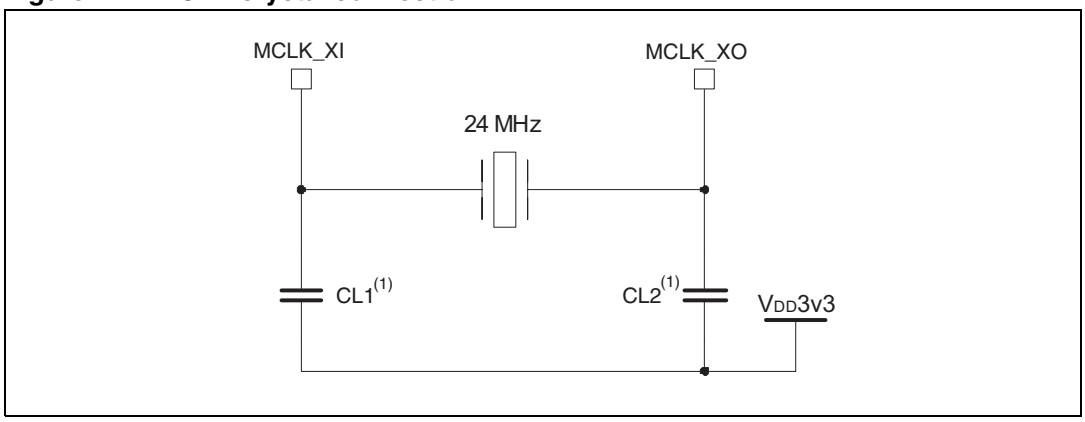
External clock generated from a crystal oscillator

Table 42. MCLK oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc_in}	Oscillator frequency			24(1)	33 (2)	MHz
ESR	Equivalent series resisistance				50	Ω
gm	Oscillator transconductance	Startup	19.8	28.5		mA/V
t_{SU}	Startup time	Stabilized power on MCLK_AVDD3V3 pin			2 (3)	ms

1. A frequency of 24 MHz is mandatory to obtain the required frequencies for all clocks generated by the PLL of the USB PHY.
2. At Max freq = 33 MHz the ESR value has to be less than 20 Ω.
3. Startup time simulated with a 30 MHz crystal.

Figure 7. MCLK crystal connection



1. CL1 and CL2 are the load capacitors.

The value of the capacitors depends on the type of the selected crystal. To calculate the value of the load capacitance, use the formula given below.

For this example, Aker C2E-24.000-12-3030-X 24 MHz oscillator has been used.

Formula

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Where CL1 and CL2 are the load capacitors and CS is the circuit stray capacitance.

In our application:

$$CL1 = CL2 = Cext$$

This implies:

$$Cext = (CL-CS)*2$$

Example:

For the Aker C2E-24.000-12-3030-X crystal, CL = 12 PF

With CS = 3 PF, we have: Cext = CL1 = CL2 = 18 PF

MCLK generated from an external clock source

Table 43. MCLK external user clock source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCLK_XI}	External clock source frequency		No limitation	24(1)	33	MHz
V_{MCLK_XIH}	MCLK_XI input pin high level voltage		MCLK_AVDD3V3 - 0.3		MCLK_AVDD3V3	V
V_{MCLK_XIL}	MCLK_XI input pin low level voltage		MCLK_GNDSUB		0.3	V
$DuCy_{(MCLK\_XI)}$	Duty cycle(2)		40		60	%
$t_{r(MCLK\_XI)}$ $t_{f(MCLK\_XI)}$	MCLK_XI input rise and fall time		-5% of the clock period		+5% of the clock period	%
$C_{IN(MCLK\_XI)}$	MCLK_XI input capacitance			7		pF
$I_{L(MCLK\_XI)}$	MCLK_XI input leakage current	MCLK_GNDSUB $\leq V_{IN} \leq$ MCLK_AVDD3V3			±1	µA

1. A frequency of 24 MHz is mandatory to obtain the required operating frequency for all clocks generated by the PLL from the USB PHY.
2. An initial delay of 1 µs + 2048 f_{MCLK_XI} cycles occurs for duty cycle detection and internal clock availability.

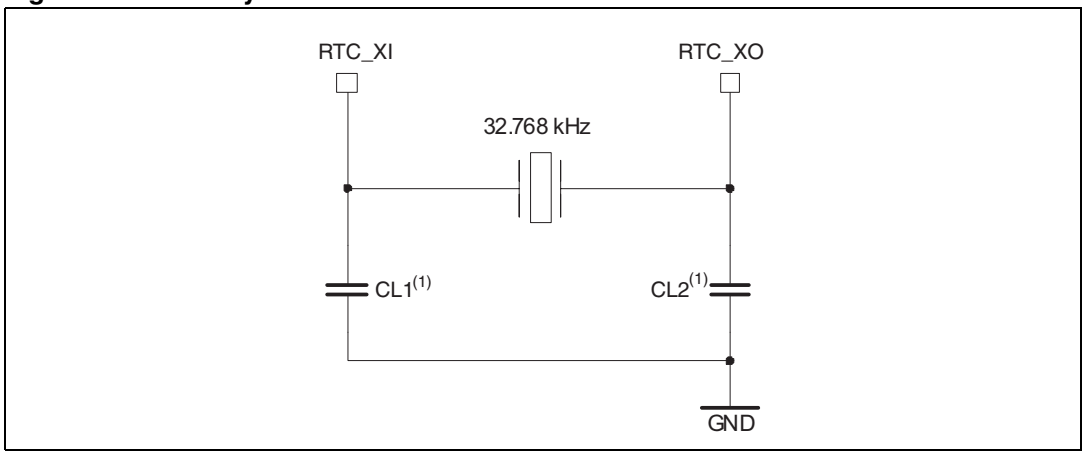
4.3.2 Real-time clock (RTC)

External clock generated from a crystal oscillator

Table 44. RTC oscillator characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency			32.768		kHz
ESR	Equivalent series resistance				6000	Ω
gm	Oscillator transconductance	Startup	12		25	µA/V
t_{SU}	Startup time	Stabilized power on RTC_VDD1V5 pin			1.5	f_{OSC_IN} cycles

Figure 8. RTC crystal connection



1. CL1 and CL2 are the load capacitors.

The value of the capacitors depends on the type of the selected crystal. To calculate the value of the load capacitance, use the formula given below.

Formula

$$C_L = \frac{C_{L1} \times C_{L2}}{C_{L1} + C_{L2}} + C_s$$

Where C_{L1} and C_{L2} are the load capacitors and C_S is the circuit stray capacitance.

In our application:

$$C_{L1} = C_{L2} = C_{ext}$$

This implies:

$$C_{ext} = (C_L\text{-}C_S)*2$$

Example:

For this example, a Fox Electronics, NC26LF-327 32.768 kHz oscillator has been used.

For the Fox Electronics, NC26LF-327 crystal, C_L = 12.5 pF

With C_S = ~0.1 pF, we have: Cext = C_{L1} = CL2 = 24.8 pF=22 pF

RTC clock generated from an external clock source

Table 45. RTC external user clock source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{RTC_XI}	External clock source frequency			32.768		kHz
V_{RTC_XIH}	RTC_XI input pin high level voltage		RTC_VDD1V5 - 0.2		RTC_VDD1V5	V
V_{RTC_XIL}	RTC_XI input pin low level voltage		RTC_GND		0.2	V
$DuCy_{(RTC\_XI)}$	Duty cycle		40		60	%
$t_{r(RTC\_XI)}$ $tf_{(RTC\_XI)}$	RTC_XI input rise and fall time				50	ns
$C_{IN(RTC\_XI)}$	RTC_XI input capacitance			5		pF
$I_{L(RTC\_XI)}$	RTC_XI input leakage	RTC_GND ≤ V_{IN} ≤ RTC_VDD1V5			±1	µA

4.4 I/O AC/DC characteristics

The following sections show the electrical AC/DC characteristics of the I/Os present in SPEAr1340.

4.4.1 3V3/2V5/1V8 I/O buffers (IOTYPE1/IOTYPE2/IOTYPE3)

The 3V3/2V5/1V8 buffers are designed to operate at 3.3 V, 2.5 V, and 1.8 V supply level. Even if they support switchable supplies, each I/O type has limited supply flexibility by design:

IOTYPE1: only 3V3

IOTYPE2: 3V3/1V8

IOTYPE3: 3V3/2V5

Features

- Switchable 1.8 V, 2.5 V, or 3.3 V supply
- Input with hysteresis
- Programmable drive and slew
- Programmable pull-up/down functionality

DC characteristics

Table 46 shows the DC characteristics for 3V3/2V5/1V8 I/O buffers.

Table 46. 3V3/2V5/1V8 I/O DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDx	1V8 supply voltage	–	1.65	–	1.95	V
	2V5 supply voltage	–	2.25	–	2.75	V
	3V3 supply voltage	–	3.0	–	3.6	V
Receiver characteristics(1)						
1V8 I/O operation						
V_{IH}	High level input voltage	–	0.65*VDDx	–	VDDx+0.3	V
V_{IL}	Low level input voltage	–	-0.3	–	0.35*VDDx	V
V_{hyst}	Schmitt trigger hysteresis	–	50	–	-	mV
2V5 I/O operation						
V_{IH}	High level input voltage	–	1.7	–	VDDx+0.3	V
V_{IL}	Low level input voltage	–	-0.3	–	0.7	V
V_{hyst}	Schmitt trigger hysteresis	–	50	–		mV
3V3 I/O operation						
V_{IH}	High level input voltage	–	2.0	–	VDDx+0.3	V

Table 46. 3V3/2V5/1V8 I/O DC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	–	-0.3	–	0.8	V
V_{hyst}	Schmitt trigger hysteresis	-	50	-		mV
Pull-up and pull-down characteristics						
1V8 I/O operation						
R_{PU} (50 KΩ)	Equivalent pull-up resistance	Vi= 0V	50	-		KΩ
R_{PD}	Equivalent pull-down resistance	Vi= VDDx	50	-	-	KΩ
2V5 I/O operation						
R_{PU} (50 KΩ)	Equivalent pull-up resistance	Vi= 0V	50	-		KΩ
R_{PD}	Equivalent pull-down resistance	Vi= VDDx	50	-	-	KΩ
3V3 I/O operation						
R_{PU} (50KΩ)	Equivalent pull-up resistance	Vi= 0V	50	-		KΩ
R_{PD}	Equivalent pull-down resistance	Vi= VDDx	50	-	-	KΩ
Output characteristics						
1V8 I/O operation						
V_{OL}	Low level output voltage	I_{OL}[(2)]=4 /6 /8 /10 mA	-	-	0.4	V
V_{OH}	High level output voltage	I_{OH}= 4 /6 /8 /10 mA	VDDx-0.4	-	-	V
2V5 I/O operation						
V_{OL}	Low level output voltage	I_{OL}= 4 /6 /8 /10 mA	-	-	0.4	V
V_{OH}	High level output voltage	I_{OH}= 4 /6 /8 /10 mA	VDDx-0.4	-	-	V
3V3 I/O operation						
V_{OL}	Low level output voltage	I_{OL}= 4 /6 /8 /10 mA	-	-	0.4	V
V_{OH}	High level output voltage	I_{OH}= 4 /6 /8 /10 mA	VDDx-0.4	-	-	V

1. External drivers must be powered at the same voltage as the relative SPEAr input pad.
2. At V_{OL}/V_{OH} level, I_{OL}/I_{OH} is the minimum source/sink current drive, when the buffer is programmed at corresponding drive level by core drive select pins.

AC characteristics

Table 47 and *Table 48* show the AC input and output characteristics for 3V3/2V5/1V8 I/O buffers.

Table 47. 3V3/2V5/1V8 I/O AC input characteristics

Max frequency	Max load	Comment
1V8 I/O operation		
200 MHz	1 pF	This load is placed at ZI. (see *Figure 9* below)
2V5/3V3 I/O operation		
200 MHz	1 pF	This load is placed at ZI.

Table 48. 3V3/2V5/1V8 I/O AC output characteristics

Drive	Fast slew		Nominal slew	
	Frequency (MHz)	Load (pF)	Frequency (MHz)	Load (pF)
1V8 I/O operation				
4 mA	20	20	8	20
	40	6	16	6
6 mA	30	20	12	20
	60	6	24	6
8 mA	40	20	16	20
	80	6	32	6
10 mA	50	20	20	20
	100	6	40	6
2V5/3V3 I/O operation				
4 mA	30	20	12	20
	60	6	24	6
6 mA	45	20	18	20
	90	6	36	6
8 mA	60	20	24	20
	120	6	48	6
10 mA	70	20	28	20
	140	6	56	6

Figure 9. 3V3/2V5/1V8 I/O input test setup

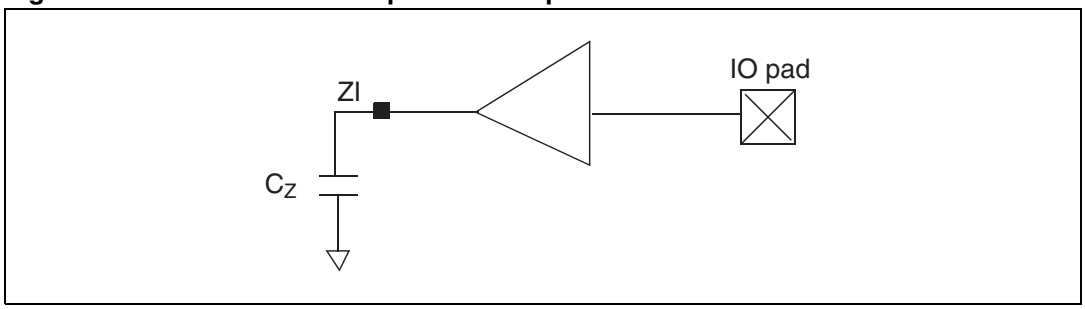
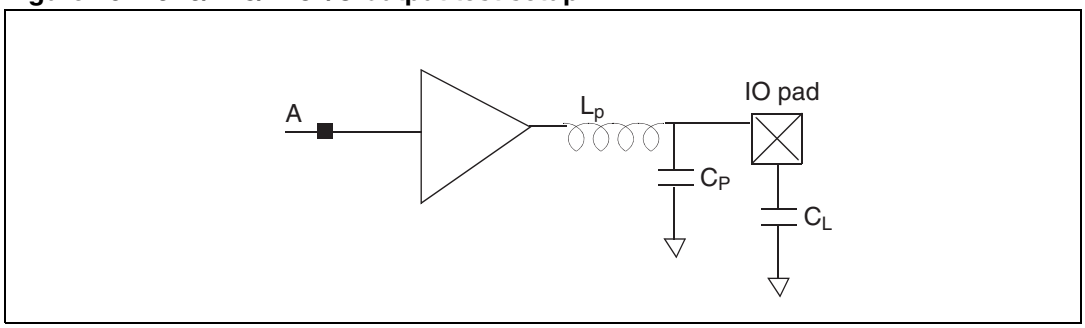


Figure 10. 3V3/2V5/1V8 I/O output test setup



4.4.2 IOTYPE4 I/O buffers

There is only one I/O pin of this type: XGPIO169 (ball K28).

Features

- 3.3 V signaling
- Programmable pull-up/down functionality

DC characteristics

Table 49 shows the DC characteristics of IOTYPE4 buffers.

Table 49. IOTYPE4 DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD} 3V3	Supply voltage	-	3.0	-	3.6	V
Receiver characteristics(1)						
V_{IH}	High level input voltage	-	2.0	-	V_{DD} 3V3+0.5	V
V_{IL}	Low level input voltage	-	-0.5	-	0.8	V
Driver characteristics						
I_{OH}	Source current	V_{OH}= V_{DD} 3V3-0.2	8	-	-	mA
I_{OL}	Sink current	V_{OL}= 0.2	8	-	-	mA
Pull-up and pull-down characteristics						
R_{PU}	Equivalent pull-up resistance	V_{pad} = 0	-	50	-	KΩ
R_{PD}	Equivalent pull-down resistance	V_{pad} = V_{DD} 3V3	-	50	-	KΩ

1. External drivers must be powered at the same voltage as the relative SPEAr input pad.

AC characteristics

Table 50 shows the AC characteristics of IOTYPE4 buffers.

Table 50. Input (I/O) pin capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver characteristics						
C_z	Capacitive load at ZI	–	–	–	1	pF
Duty cycle	Duty cycle at ZI	(1)	45	–	55	%
Driver characteristics						
C_L	Capacitive load at I/O	–	–	–	40	pF
Frequency	Operating frequency	(2)	–	–	100	MHz
Duty cycle	Duty cycle at I/O	(3)	45	–	55	%

1. With input duty cycle of 50% at I/O.
2. Output swing from 2.4V to 0.4 V is guaranteed for this operating frequency range.
3. With input duty cycle of 50% at A.

Figure 11. IOTYPE4 input test setup

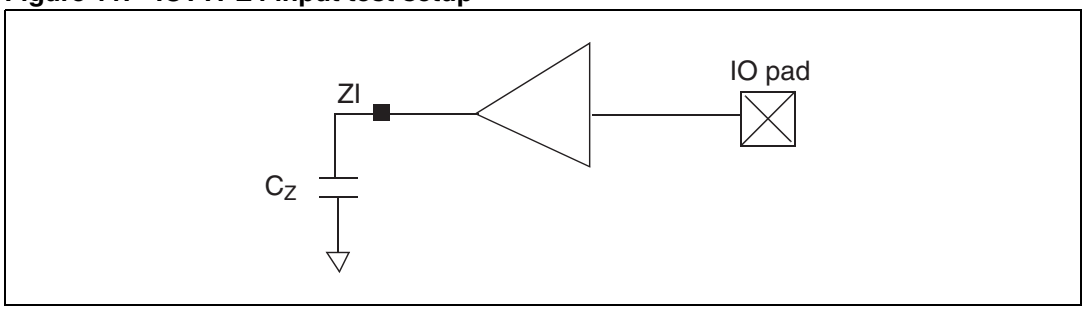
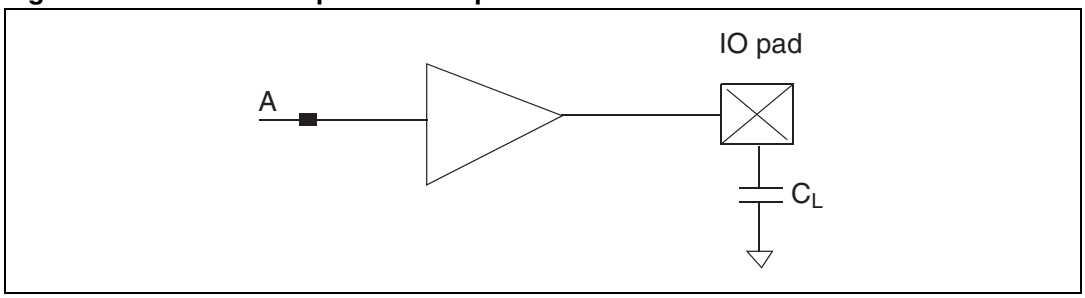


Figure 12. IOTYPE4 output test setup



1. Parasitic capacitance and inductance are not shown here, but taken into account with measurement setup. For values of L and C, please refer to *Table 49: IOTYPE4 DC characteristics*.

4.4.3 DDR2 and DDR3 mode I/O buffers

This section is applicable to I/O pins of type SSTL (SSTL 1V5/1V8).

The DDR2/DDR3 buffers can work either with 1.8 V supply in DDR2 applications or 1.5 V in DDR3 applications.

Features

- 1.5 V and 1.8 V signaling
- Pseudo-differential input for data and fully-differential input for strobe.
- On-die termination (ODT) functionality, in order to integrate the parallel resistor inside the die and improve signal integrity.

AC/DC characteristics

Table 51 shows the AC/DC characteristics of DDR2 and DDR3 buffers.

Table 51. DDR2/DDR3 AC/DC driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD} DDR	DDR2 1V8 supply voltage	-	1.7	1.8	1.9	V
	DDR3 1V5 supply voltage	-	1.4	1.5	1.6	V
Z_{OUT}	Output impedance	Vpad= V_{DD} DDR/2 R_{EXT}= 332 Mandatory	34.3-10% = 30.9	34.3	34.3 + 10% = 37.7	Ω
V_{OH} (AC)	High level output voltage	-	DDR2: V_{DD} DDR/2 + 0.2	-	-	V
			DDR3: V_{DD} DDR/2 + 0.175			
V_{OL} (AC)	Low level output voltage	-	-	-	DDR2: V_{DD} DDR/2-02	V
				-	DDR3: V_{DD} DDR/2- 0.175	
V_{OH} (DC)	High level output voltage	-	DDR2: V_{DD} DDR/2 + 0.125	-	-	V
			DDR3: V_{DD} DDR/2 + 0.1			
V_{OL} (DC)	Low level output voltage	-	-	-	DDR2: V_{DD} DDR/2 - 0.125	V
				-	DDR3: V_{DD} DDR/2 - 0.1	

Table 52. DDR2/DDR3 pseudo-differential receiver AC and DC characteristics

Symbol	Parameter	DDR2			DDR3			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{DD} DDR	DDR2/DDR3 supply voltage	1.7	1.8	1.9	1.4	1.5	1.6	V
V_{REF}	Voltage reference	0.49 * V_{DD} DDR	0.5 * V_{DD} DDR	0.51 * V_{DD} DDR	0.49 * V_{DD} DDR	0.5 * V_{DD} DDR	0.51 * V_{DD} DDR	V
V_{IH}(AC)	High level input voltage	(1)	-	(1)	V_{REF} + 0.1	-	(1)	V
V_{IL}(AC)	Low level input voltage		-		(1)	-	V_{REF} - 0.1	V
V_{IH}(DC)	High level input voltage		-		0.8 * V_{DD} DDR	-	(1)	V
V_{IL}(DC)	Low level input voltage		-		(1)	-	0.2 * V_{DD} DDR	V

1. No data available in JEDEC update.

Table 53. DDR2/DDR3 on-die termination (ODT) DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{T1} (DDR2)	Lower effective impedance value for DDR2	60	75	90	Ω
R_{T2} (DDR2)	Higher effective impedance value for DDR2	120	150	180	Ω
R_{T1} (DDR3)	Lower effective impedance value for DDR3	53 (60-12%)	60	69 (60+15%)	Ω
R_{T2} (DDR3)	Higher effective impedance value for DDR3	106 (120-12%)	120	138 (120+15%)	Ω
DeltaVM	Deviation of V_M with respect to V_{DD} DDR/2	-5	-	1	%

To measure RT1 or RT2:

1. Apply V_{IH}(DC) and V_{IL}(DC) to the IOPAD pin separately while the I/O is in input mode with the ODT enabled.
2. Measure the current I(V_{IH}(DC)) and I(V_{IL}(DC)) according to the following equation:

$$R_{TX} = \frac{V_{IH}(DC) - V_{IL}(DC)}{I(V_{IH}(DC)) - I(V_{IL}(DC))}$$

To measure DeltaVM:

1. Measure voltage at the IOPAD pin while the I/O is in input mode with the ODT enabled.
2. Calculate DeltaV_M according to the following equation:

$$DeltaV_M = \left(\frac{2 \times V_M - V_{DD}DDR}{V_{DD}DDR}\right) \times 100$$

4.5 Voltage regulator characteristics

SPEAr1340 has three internal voltage regulators:

- MIPHY single-lane regulator: the voltage controlled by this regulator is internally connected to the MIPHY supply, but it is also externally visible on MIPHY0_VDD2PLL2V5. The regulator is always active; it is not possible to bypass it.
- VREG1 regulator: used only for USB
- VREG2 regulator: used for all PLLs (PLL1, PLL2, PLL3, DDR PLL), ADC and OTP.

Each regulator receives a 3V3 voltage supply as input and generates a 2V5 voltage supply as output.

The following table shows the main requirements for the voltage regulators.

Table 54. Voltage regulators requirements

Voltage regulator input	Voltage regulator output	Balls connected	Input voltage	Output voltage	Max current	External capacitor
MIPHY0_VREG_3V3_IN	MIPHY0_VDD2PLL2V5	P3	3.3 V	2.5 V	100 mA	10 µF
VREG1_3V3_IN	VREG1_2V5_OUT (ball M6)	J4 E3 G3	3.3 V	2.5 V	150 mA	2.2 µF
VREG2_3V3_IN	VREG2_2V5_OUT (ball F6)	E6 E4 N5 AC5 U19 C4	3.3 V	2.5 V	150 mA	2.2 µF

4.6 MiPHY characteristics

For SATA operation, the MIPHY0_XTAL1/MIPHY0_XTAL2 clock input can be implemented by a 25 MHz crystal oscillator. For PCIe operation, a suitable clock driver such as ON Semiconductor NB3N5573 or Silicon labs Si5330C_A000207 can be used.

Table 55. MiPHY characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{OSC}	MIPHY0_XTAL1/MIPHY0_XTAL2 clock input frequency for SATA configuration		25		MHz
	MIPHY0_XTAL1/MIPHY0_XTAL2 clock input frequency for PCIe configuration		100		
V_{IH}	MIPHY0_RXp/MIPHY0_RXn differential input HIGH voltage	+150			mV
V_{IL}	MIPHY0_RXp/MIPHY0_RXn differential input LOW voltage			-150	mV
$V_{IN(OSC)}$	MIPHY0_XTAL1/MIPHY0_XTAL2 clock input voltage	-0.3		1.15	V
$Z_{IN(OSC)}$	MIPHY0_XTAL1/MIPHY0_XTAL2 clock input impedance		50		Ω

4.7 Required external components

Some pads require the use of an external resistor. *Table 56* lists these pads and the value of the resistors to be used.

Table 56. List of required resistors

Pad name	Value	Ball
MIPHY0_REF	487 Ω (± 1%)	R1
USB_TXRTUNE	43.2 Ω (± 1%)	G1
DDRIO_COMP_REXT	332 Ω (± 1%)	AD5
IO_COMP_REXT1_3V3	121 KΩ (± 1%)	AC21
IO_COMP_REXT2_3V3	121 KΩ (± 1%)	K19
IO_COMP_REXT1_1V8_3V3	121 KΩ (± 1%)	K12
IO_COMP_REXT2_1V8_3V3	121 KΩ (± 1%)	K15
IO_COMP_REXT_2V5_3V3	121 KΩ (± 1%)	R19

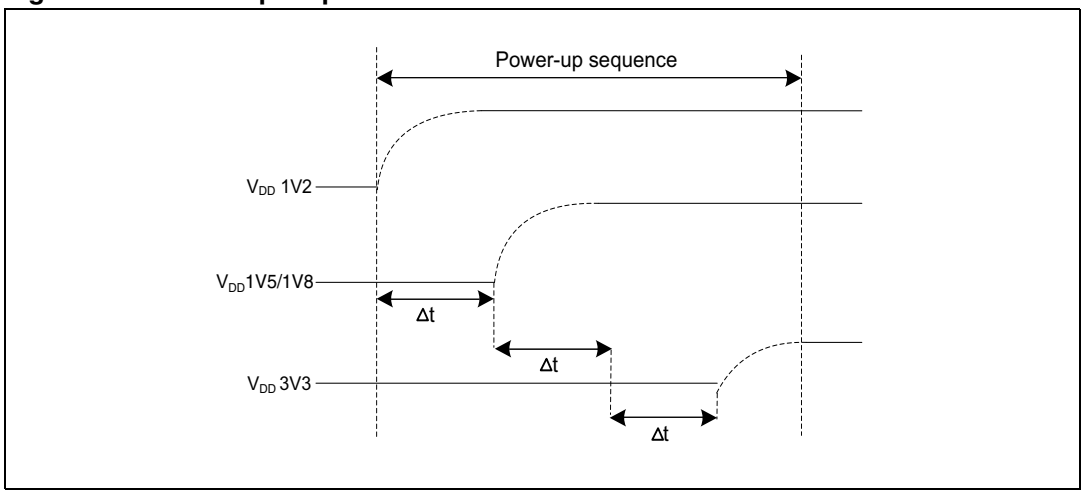
4.8 Power-up sequence

It is recommended to power up the power supplies in the order shown in *Figure 13*.

V_{DD} 1V2 is brought up first, followed by V_{DD} 1V5/1V8, and then V_{DD} 3V3. The minimum time (Δt) between each power up is >0 µs.

Note: The 2V5 power supply is generated by internal voltage regulators, just after the 3V3. Make sure that different 2V5 input power rails are driven by SPEAr internal regulators.

Figure 13. Power-up sequence



4.9 Power-down sequence

All power supplies can be shut down at the same time.

4.10 Reset release

The master reset (MRESETn) must be released after all the power supplies are stable and for a time interval of 2 ms, which is the start-up time of the main oscillator, and must be asserted low for at least 1 µs for warm reset.

Figure 14. Cold reset release

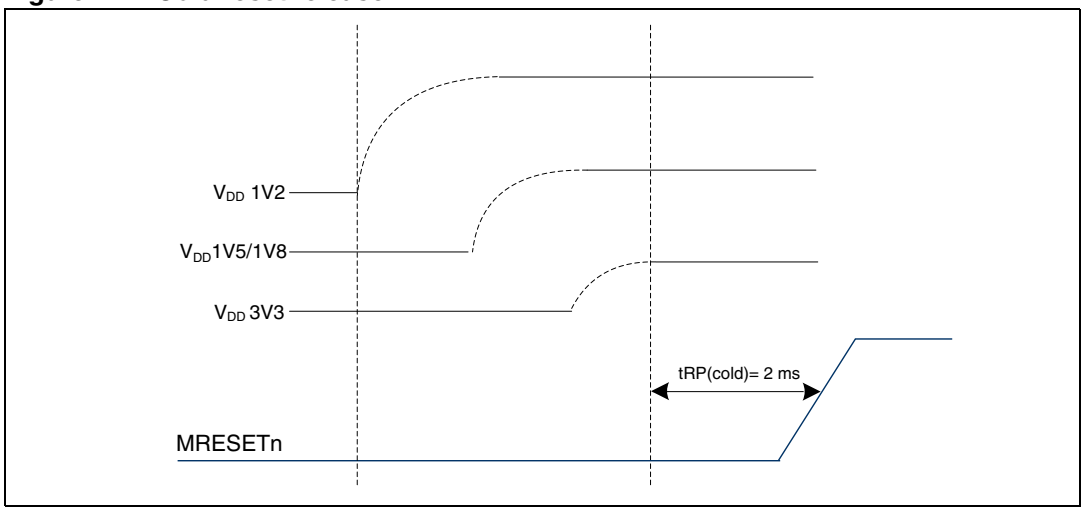
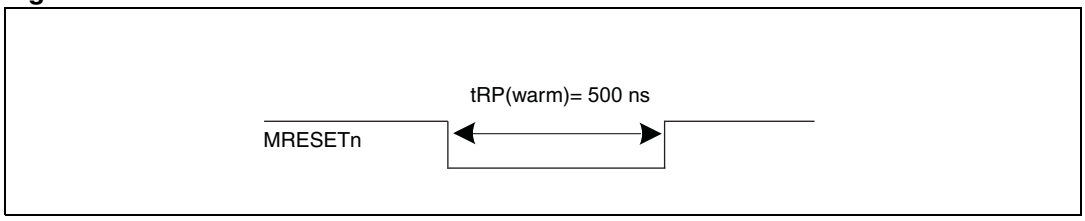


Figure 15. Warm reset release



Note: See also: Section 5.1: Reset timing characteristics on page 151.

4.11 ADC electrical characteristics

Table 57. ADC characteristics

Symbol	Parameters	Min	Typ	Max	Unit
f_{ADC_CLK}	ADC_CLK frequency	2.5	14	20	MHz
AV_{DD}	ADC supply voltage	2.25	2.5	2.75	V
V_{REFP}	Positive reference voltage	1	2.5	2.75	V
V_{REFN}	Negative reference voltage	0	0	0.7	V
V_{IREF}	Internal reference voltage	1.95	2	2.05	V
$t_{STARTUP}$	Startup time		50		µs
V_{AIN}	Input range (absolute)	AGND - 0.3		AVDD - 0.3	V
	Conversion range	V_{REFN}		V_{REFP}	V
C_{AIN}	Input capacitance	5	6.4	8	pF

Table 57. ADC characteristics (continued)

Symbol	Parameters	Min	Typ	Max	Unit
R_{AIN}	Input mux resistance (total equivalent sampling resistance)	1.5	2	2.5	KΩ
t_{CONV}	Conversion time (f_{ADC_CLK}=14 MHz)		1		µs
	Conversion time	14			ADC_CLK cycles
INL	Integral linearity error			±1	LSB
DNL	Differential linearity error			±0.8	LSB

5 Timing characteristics

This chapter provides the timing characteristics for the synchronous and asynchronous IPs present in SPEAr1340.

The timings have been calculated under the following operating conditions:

- In worst case: V= 0.90 V, T = 125 °C
- In best case: V= 1.10 V, T = 40 °C

In *Table 58* you will find an explanation of the symbols used in this chapter to describe timing parameters.

Table 58. Symbol definition

Symbol	Definition
T_{CLK}	Clock period: the time for a complete clock cycle.
$T_{CLKhigh}$	High-pulse width: the minimum amount of time for the high pulse of the clock.
T_{CLKlow}	Low-pulse width: the minimum amount of time for the low pulse of the clock.
T_{setup} (T_s)	Setup time: the minimum amount of time the data signal should be held steady *before* the clock event so that the data is reliably sampled.
T_{hold} (T_h)	Hold time: the minimum amount of time the data signal should be held steady *after* the clock event so that the data is reliably sampled.
T_D	Clock-to-output delay: the maximum time required to obtain a valid output after the clock edge.

5.1 Reset timing characteristics

Table 59. Reset timing characteristics

Symbol	Description	Min	Unit
tRP(cold)	MRESETn pin active low state duration for cold reset (startup time from all supplies up and stable). See *Figure 14: Cold reset release on page 149*)	2	ms
tRP(warm)	MRESETn pin active low state duration for warm reset (minimum pulse width able to reset the device). See *Figure 15: Warm reset release on page 149*)	500	µs

Note: Warm reset can be triggered by software by writing any value to the miscellaneous register SYS_SW_RES.

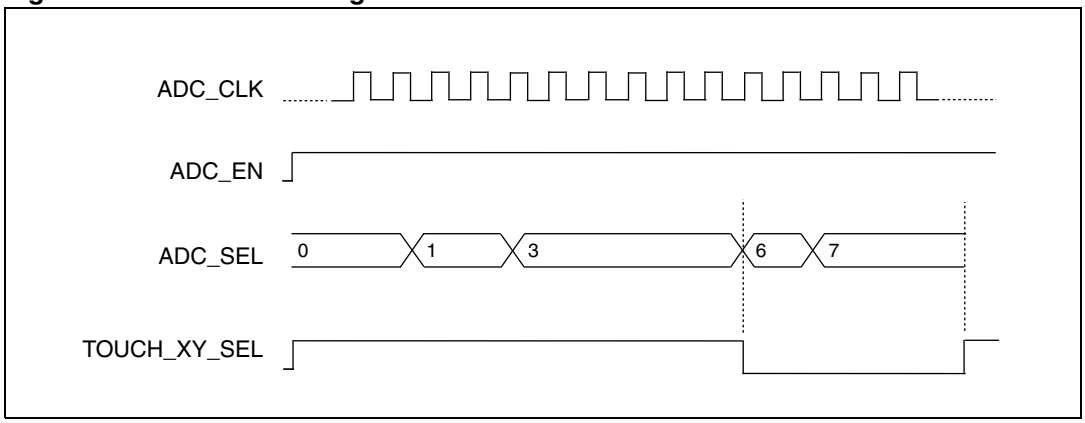
5.2 ADC timing characteristics

This section describes the timing characteristics of the TOUCH_XY_SEL signal of the A/C converter.

The TOUCH_XY_SEL signal allows the switching of the X and Y axes. It is generated in both cases of 2 and 4 channels (depending on single or dual touchscreen configuration). This signal is high when converting the X values, while low when converting the Y ones.

Figure 16 shows the TOUCH_XY_SEL behavior during the ADC conversion phase. In this example, the dual touchscreen configuration is used: channels 1 and 3 convert the X values, while channels 6 and 7 convert the Y values.

Figure 16. Touchscreen signal waveform



5.3 Cortex-A9 JTAG/trace timing characteristics

This section describes the timing characteristics of Cortex-A9 JTAG and Cortex-A9 trace.

5.3.1 Cortex-A9 JTAG timing characteristics

This section describes the timing characteristics for the Cortex-A9 JTAG.

The timing characterization is performed assuming an output load capacitance of 20 pF on ARM_TDO output and an input transition of 2 ns on all the inputs.

Figure 17. JTAG timing waveforms

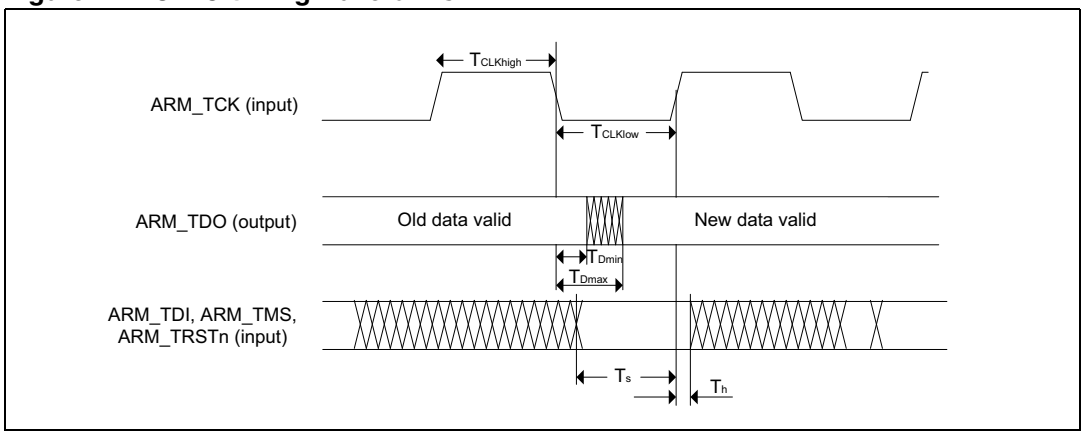


Table 60. JTAG timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	ARM_TCK clock period	33.3		ns
$T_{CLKhigh}$	ARM_TCK pulse high	10	–	ns
T_{CLKlow}	ARM_TCK pulse low	10	–	ns
T_{D}	ARM_TCK to ARM_TDO output delay	4	17	ns
T_{sdata}	Setup time for ARM_TDI and ARM_TMS data	6		ns
T_{hdata}	Hold time for ARM_TDI and ARM_TMS data	1		ns
T_{sreset}	Setup time for ARM_TRSTn reset	15		ns
T_{hreset}	Hold time for ARM_TRSTn reset	1		ns

5.3.2 Cortex-A9 trace timing characteristics

This section describes the timing characteristics for the ARM trace which works on both rising edge and falling edge of the ARM_TRCCLK clock.

The timing characterization is performed assuming an output load capacitance of 20 pF on the outputs and using PLL1 as the clock source for the timing extractions.

Figure 18. ARM trace timing waveform

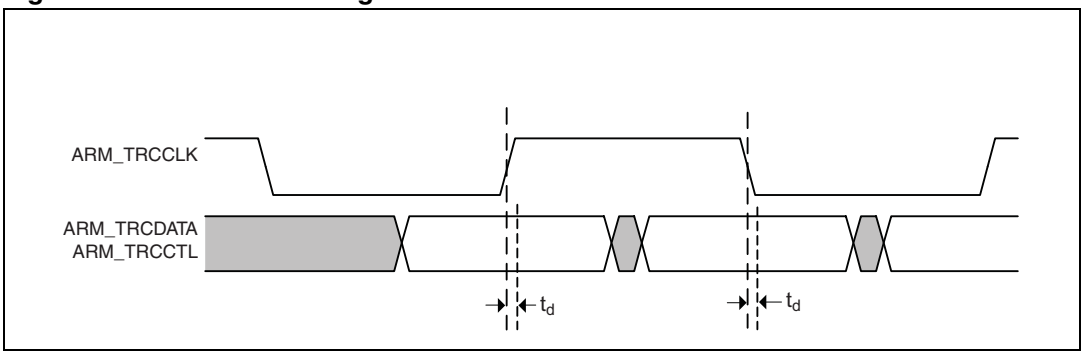


Table 61. ARM trace timing characteristics

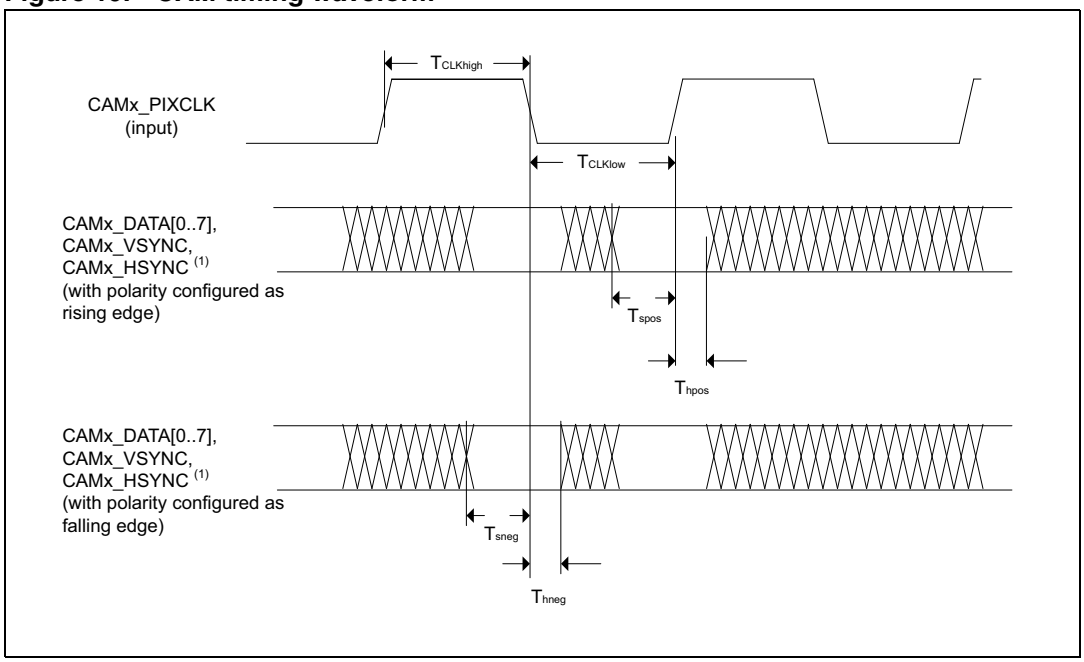
Symbol	Description	Min	Max	Unit
T_{CLK}	ARM_TRCCLK clock period	8		ns
$T_{CLKhigh}$	ARM_TRCCLK pulse high	2.9	–	ns
T_{CLKlow}	ARM_TRCCLK pulse low	2.9	–	ns
T_{Drise}	ARM_TRCCLK to ARM_TRCDATA0..ARM_TRCDATA31, ARM_TRCCTL output delay	-3.7	4	ns
T_{Dfall}	ARM_TRCCLK to ARM_TRCDATA0..ARM_TRCDATA31, ARM_TRCCTL output delay	-4	3.7	ns

5.4 CAM timing characteristics

This section describes the timing characteristics of the four camera input interfaces which can work on the clock rising edge or on the clock falling edge.

The timing characterization is performed assuming an input transition of 2 ns on all the inputs and CAMx_PIXCLK and using PLL1 as the clock source for the timing extractions.

Figure 19. CAM timing waveform



1. x = 1..4.

Table 62. CAMx timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	CAMx_PIXCLK clock period	6.5	–	ns
$T_{CLKhigh}$	CAMx_PIXCLK pulse high	2.9	–	ns
T_{CLKlow}	CAMx_PIXCLK pulse low	2.9	–	ns
CAM1				
T_{spos}	Setup time for CAM1 data respect to clock rising edge	5.4	–	ns
T_{hpos}	Hold time for CAM1 data respect to clock rising edge	-0.7	–	ns
T_{sneg}	Setup time for CAM1 data respect to clock falling edge	5.6	–	ns
T_{hneg}	Hold time for CAM1 data respect to clock falling edge	-0.8	–	ns
CAM2				
T_{spos}	Setup time for CAM2 data respect to clock rising edge	5.7	–	ns
T_{hpos}	Hold time for CAM2 data respect to clock rising edge	-0.3	–	ns
T_{sneg}	Setup time for CAM2 data respect to clock falling edge	5.9	–	ns
T_{hneg}	Hold time for CAM2 data respect to clock falling edge	-0.4	–	ns

Table 62. CAMx timing characteristics (continued)

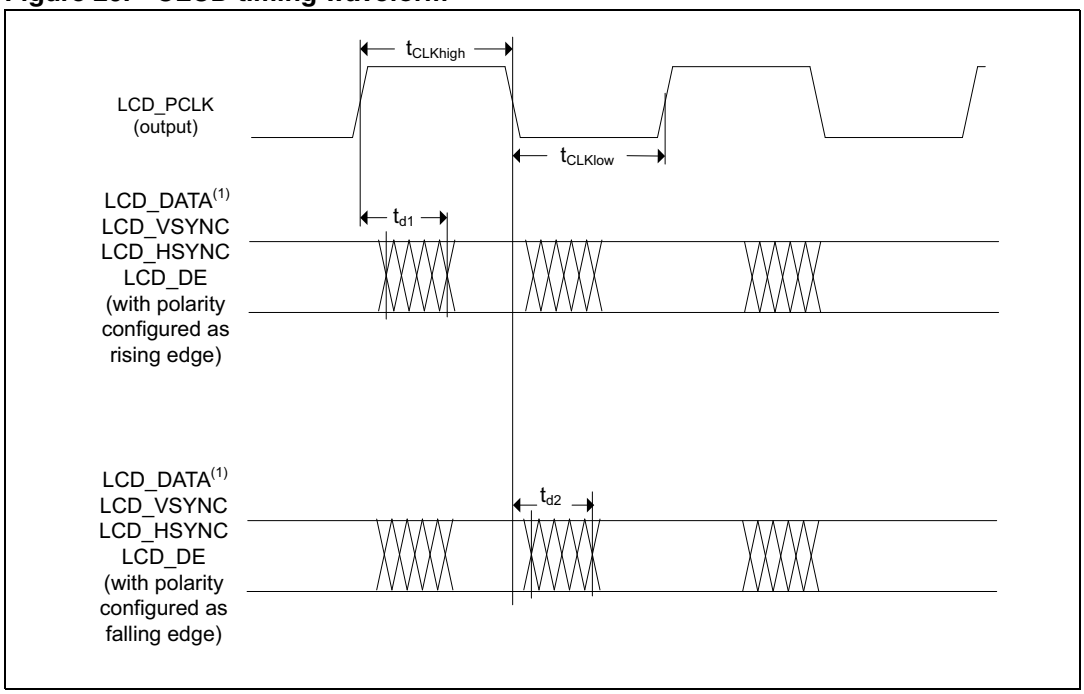
Symbol	Description	Min	Max	Unit
CAM3				
T_{spos}	Setup time for CAM3 data respect to clock rising edge	5.5	–	ns
T_{hpos}	Hold time for CAM3 data respect to clock rising edge	-0.7	–	ns
T_{sneg}	Setup time for CAM3 data respect to clock falling edge	5.6	–	ns
T_{hneg}	Hold time for CAM3 data respect to clock falling edge	-0.7	–	ns
CAM4				
T_{spos}	Setup time for CAM4 data respect to clock rising edge	5.5	–	ns
T_{hpos}	Hold time for CAM4 data respect to clock rising edge	-0.8	–	ns
T_{sneg}	Setup time for CAM4 data respect to clock falling edge	5.6	–	ns
T_{hneg}	Hold time for CAM4 data respect to clock falling edge	-0.9	–	ns

5.5 CLCD timing characteristics

This section describes the timing characteristics for the LCD display controller which can work on the clock rising edge or on the clock falling edge.

The timing characterization is performed assuming an output load capacitance of 10 pF on all outputs and using PLL3 as the clock source for the timing extractions.

Figure 20. CLCD timing waveform



1. LCD_DATA = LCD_R[0-7], LCD_XR[0-7], LCD_B[0-7], LCD_XB[0-7], LCD_G[0-7], LCD_XG[0-7].

Table 63. CLCD timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	LCD_PCLK clock period	6.5	–	ns
$T_{CLKhigh}$	LCD_PCLK pulse high	3	–	ns
T_{CLKlow}	LCD_PCLK pulse low	3	–	ns
T_{D1}	LCD_PCLK rising edge to LCD_DATA, LCD_VSYNC, LCD_HSYNC LCD_DE output data delay	0.9	5.6	ns
T_{D2}	LCD_PCLK falling edge to LCD_DATA, LCD_VSYNC, LCD_HSYNC LCD_DE output data delay	1	5.8	ns

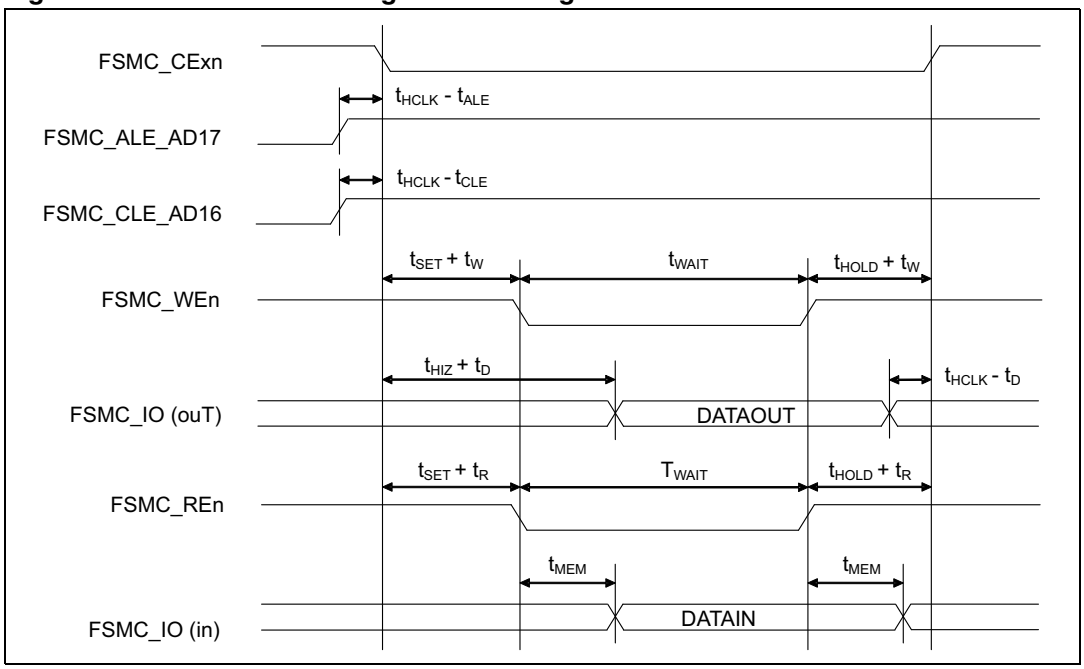
5.6 FSMC timing characteristics

This section describes the timing characteristics of the flexible static memory controller. The FSMC can interface NAND Flash, NOR and SRAM. All the possible scenarios are described below.

The timing characterization is performed assuming an output load capacitance of 10 pF on all outputs.

5.6.1 NAND Flash configuration timing characteristics

Figure 21. NAND Flash configuration timing waveform



T_{ALE}, T_{CLE}, T_W, T_R and T_D are fixed values: they depend only on the internal timings of SPEAr.

T_{SET}, T_{HOLD}, T_{WAIT} and T_{HIZ} are programmable timings defined by FSMC registers. They can be calculated as:

T_{SET} = (Set + 1) * T_{HCLK} (min value for Set is 0)

T_{WAIT} = (Wait + 1) * T_{HCLK} (min value for Wait is 1)

T_{HOLD} = (Hold + 1) * T_{HCLK} (min value for Hold is 1)

T_{HIZ} = Hiz * T_{HCLK} (min value for Hiz is 0)

T_{HCLK} = 6 ns (period of the AHB clock, the FSMC input clock)

T_{MEM} is the output delay of the NAND Flash.

When writing a data, since the NAND Flash strobes it on the rising edge of FSMC_WEn, the user should choose the correct values of Set, Wait, Hold and Hiz in order to satisfy the following constraints:

$$T_{SET} + T_W + T_{WAIT} - T_{HIZ} - T_D \geq T_{SETUP} \text{ (NAND\_FLASH)}$$

$$T_{HOLD} + T_W - T_{HCLK} + T_D \geq T_{HOLD} \text{ (NAND\_FLASH)}$$

When reading a data, since the FSMC strobes it 1 HCLK cycle before the rising edge of FSMC_REn, the user should choose the correct value of Data_ST in order to satisfy the following setup constraint:

$$T_{WAIT} - T_{MEM} - T_{DEL} \geq T_{SETUP} \text{ (FSMC\_FFs)}$$

TDEL is the sum of 2 internal delays of SPEAr:

- From the FSMC flops to the FSMC_REn pad;
- From the FSMC_IO pads to the FSMC flops.

Table 64. Timings for 8-/16-bit NAND Flash configuration on FSMC_CE0n

Symbol	Min	Max	Unit
T_{ALE}	-1.47	2.44	ns
T_{CLE}	-1.77	1.83	
T_D (8-bit)	-2.76	6.48	
T_D (16-bit)	-2.82	6.48	
T_W	-1.56	2.21	
T_R	-1.29	2.50	

Table 65. Timings for 8-/16-bit NAND Flash configuration on FSMC_CE1n

Symbol	Min	Max	Unit
T_{ALE}	-1.44	2.41	ns
T_{CLE}	-1.76	1.80	
T_D (8-bit)	-2.75	6.45	
T_D (16-bit)	-2.81	6.45	
T_W	-1.50	2.18	
T_R	-1.23	2.47	

Table 66. Internal delays for 8-/16-bit NAND Flash configuration

Symbol	Min	Max	Unit
T_{DEL} (8-bit)	3.82	16.34	ns
T_{DEL} (16-bit)	3.82	16.63	
T_{SETUP} (FSMC_FFs)	0.06	0.49	

5.6.2 NOR Flash configuration timing characteristics

Figure 22. NOR configuration timing waveform (Extended_Mode = 0)

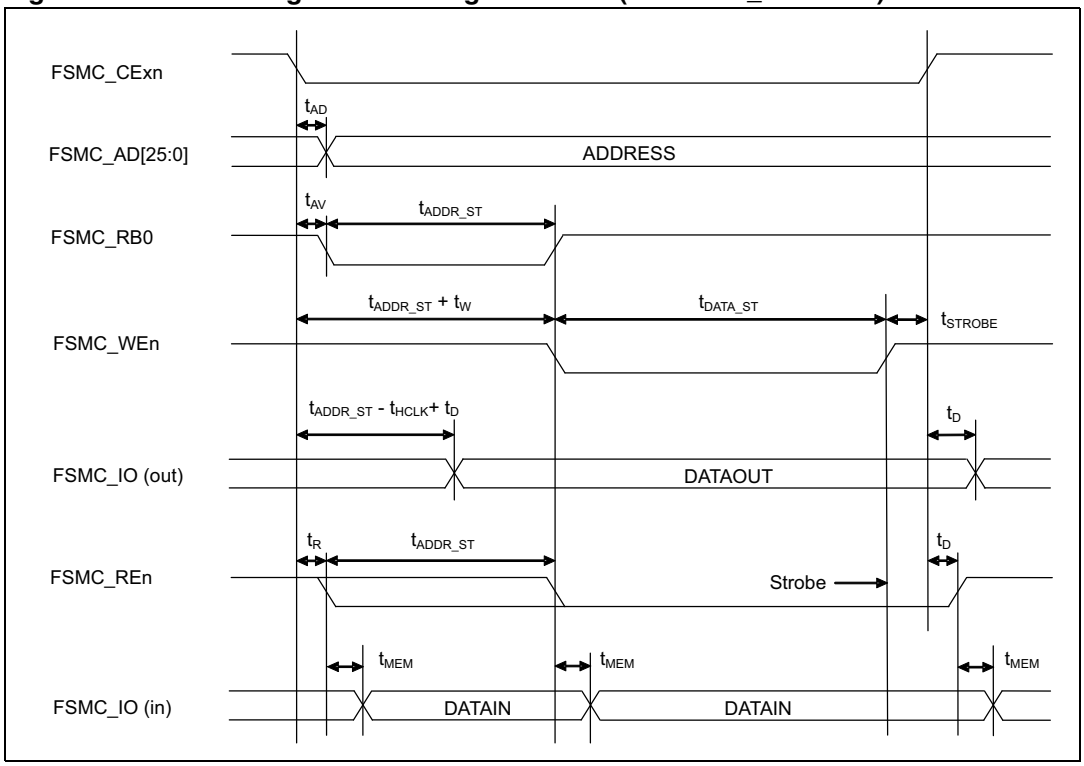
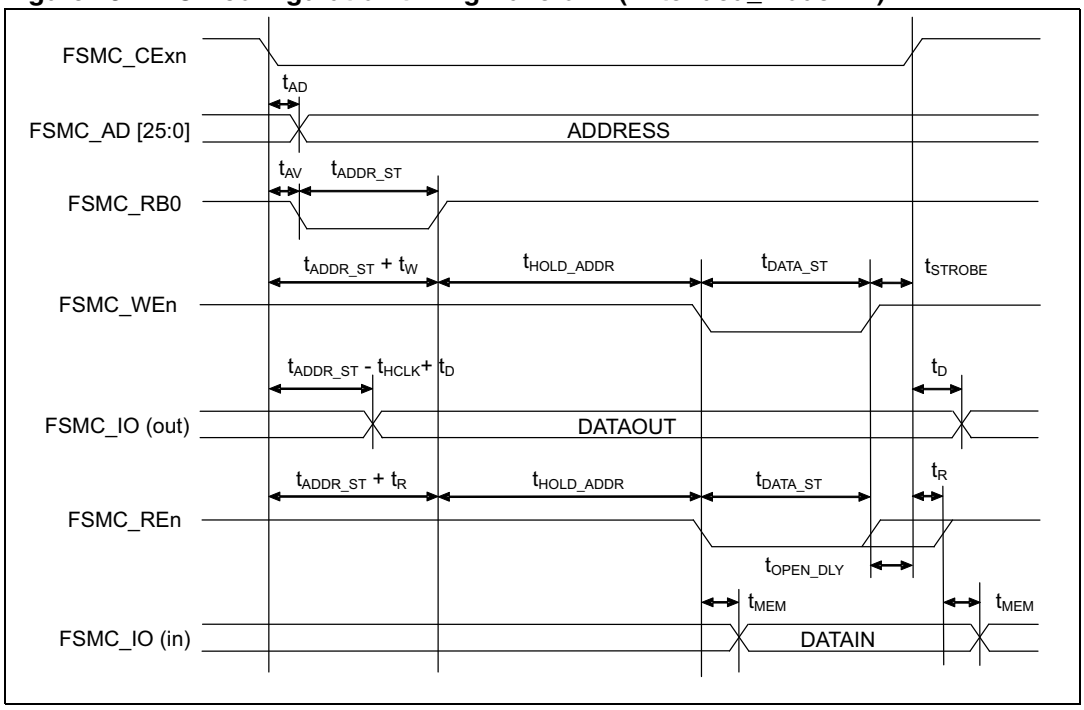


Figure 23. NOR configuration timing waveform (Extended_Mode = 1)



T_{AD}, T_{AV}, T_D, T_W, T_R and T_{STROBE} are fixed values: they depend only on the internal timings of SPEAr.

T_{ADDR_ST}, T_{HOLD_ADDR}, T_{DATA_ST} and T_{OEN_DLY} are programmable timings defined by FSMC registers. They can be calculated as:

T_{ADDR_ST} = (Addr_ST + 1) * T_{HCLK} (min value for Addr_ST is 0)

T_{HOLD_ADDR} = (Hold_addr + 1) * T_{HCLK} (min value for Hold_addr is 0)

T_{DATA_ST} = Data_ST * T_{HCLK} (min value for Data_ST is 0 for Read and 1 for Write)

T_{OEN_DLY} = OEn_delay * T_{HCLK} (when 1, the output enable rises 1 HCLK cycle before the chip select)

Since the data strobe always happens 1 HCLK cycle before the rising edge of the chip select, TSTROBE can be calculated as:

$$T_{STROBE} = T_{HCLK} - T_W$$

T_{HCLK} = 6 ns (period of the AHB clock, the FSMC input clock)

T_{MEM} is the output delay of the NOR Flash.

The FSCM_REn signal can toggle either after the de-assertion of the chip select (Extended_Mode = 0) or after the Addr_ST phase (Extended_Mode = 1).

In the 1st case the programmable timings for Read and Write are unique while in the 2nd case they can be different from each other.

When writing a data, since the NOR strobes it on the rising edge of FSMC_WEn, the user should choose the correct values of Data_ST (and eventually Hold_addr) in order to satisfy the setup constraint:

$$T_{HCLK} + T_W (+ T_{HOLD\_ADDR}) + T_{DATA\_ST} - T_D \geq T_{SETUP} \text{ (NOR\_FLASH)}$$

The hold constraint, vice versa, is fixed:

$$T_{HCLK} - T_W + T_D \geq T_{HOLD} \text{ (NOR\_FLASH)}$$

When reading a data, since the FSMC strobes it 1 HCLK cycle before the rising edge of FSMC_REn, the user should choose the correct value of Data_ST in order to satisfy the following setup constraint:

$T_{DATA\_ST} - T_{MEM} - T_{DEL} \geq T_{SETUP}$ (FSMC_FFs)

T_{DEL} is the sum of 2 internal delays of SPEAr:

- From the FSMC flops to the FSMC_REn pad;
- From the FSMC_IO pads to the FSMC flops.

Table 67. Timings for 8-/16-bit NOR Flash configuration on FSMC_CE0n

Symbol	Min	Max	Unit
T_{AD}	-2.19	4.33	ns
T_{AV}	-2.79	4.61	
T_D (8-bit)	-2.78	6.40	
T_D (16-bit)	-3.02	6.40	
T_W	-1.66	1.99	
T_R	-1.41	2.27	

Table 68. Timings for 8-/16-bit NOR Flash configuration on FSMC_CE1n

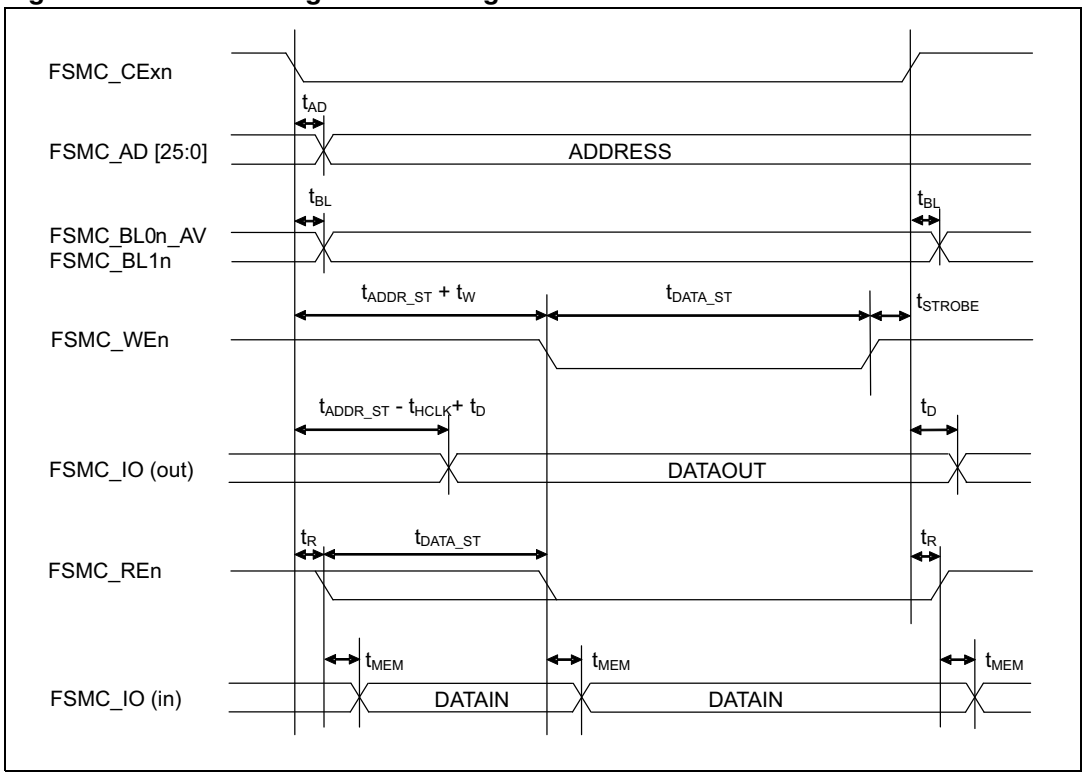
Symbol	Min	Max	Unit
T_{AD}	-1.82	4.60	ns
T_{AV}	-2.43	4.88	
T_D (8-bit)	-2.41	6.67	
T_D (16-bit)	-2.65	6.67	
T_W	-1.30	2.27	
T_R	-1.08	2.55	

Table 69. Internal delays for 8-/16-bit NOR Flash configuration

Symbol	Min	Max	Unit
T_{DEL} (8-bit)	4.03	16.25	ns
T_{DEL} (16-bit)	4.01	16.54	
T_{SETUP} (FSMC_FFs)	0.05	0.46	

5.6.3 SRAM configuration timing characteristics

Figure 24. SRAM configuration timing waveform



T_{AD}, T_{BL}, T_D, T_W, T_R and T_{STROBE} are fixed values: they depend only on the internal timings of SPEAr.

T_{ADDR_ST} and T_{DATA_ST} are programmable timings defined by FSMC registers. They can be calculated as:

$T_{ADDR\_ST} = (Addr\_ST + 1) * T_{HCLK}$ (min value for Addr_ST is 0)

$T_{DATA\_ST} = Data\_ST * T_{HCLK}$ (min value for Data_ST is 0 for Read and 1 for Write)

Since the data strobe always happens 1 HCLK cycle before the rising edge of the chip select, T_{STROBE} can be calculated as:

$$T_{STROBE} = T_{HCLK} - T_W$$

T_{HCLK} = 6 ns (period of the AHB clock, the FSMC input clock)

T_{MEM} is the output delay of the Static RAM.

The FSCM_REn signal can toggle either after the de-assertion of the chip select (Extended_Mode = 0) or after the Addr_ST phase (Extended_Mode = 1).

In the 1st case the programmable timings for Read and Write are unique while in the 2nd case they can be different from each other.

When writing a data, since the SRAM strobes it on the rising edge of FSMC_WEn, the user should choose the correct values of Data_ST in order to satisfy the setup constraint:

$T_{HCLK} + T_W + T_{DATA\_ST} - T_D \geq T_{SETUP}$ (SRAM)

The hold constraint, vice versa, is fixed:

$$T_{HCLK} - T_W + T_D \geq T_{HOLD} \text{ (SRAM)}$$

When reading a data, since the FSMC strobes it 1 HCLK cycle before the rising edge of FSMC_REn, the user should choose the correct value of Data_ST in order to satisfy the following setup constraint:

$$T_{DATA\_ST} - T_{MEM} - T_{DEL} \geq T_{SETUP} \text{ (FSMC\_FFs)}$$

T_{DEL} is the sum of 2 internal delays of SPEAr:

- From the FSMC flops to the FSMC_REn pad;
- From the FSMC_IO pads to the FSMC flops.

Table 70. Timings for 8-/16-bit SRAM configuration on FSMC_CE0n

Symbol	Min	Max	Unit
T_{AD}	-2.19	4.33	ns
T_{BL} (16-bit)	-2.79	4.80	
T_D (8-bit)	-2.78	6.40	
T_D (16-bit)	-3.02	6.40	
T_W	-1.66	1.99	
T_R	-1.41	2.27	

Table 71. Timings for 8-/16-bit SRAM configuration on FSMC_CE1n

Symbol	Min	Max	Unit
T_{AD}	-1.82	4.60	ns
T_{BL} (16-bit)	-2.43	5.08	
T_D (8-bit)	-2.41	6.67	
T_D (16-bit)	-2.65	6.67	
T_W	-1.30	2.27	
T_R	-1.08	2.55	

Table 72. Internal delays for 8-/16-bit SRAM configuration

Symbol	Min	Max	Unit
T_{DEL} (8-bit)	4.03	16.25	ns
T_{DEL} (16-bit)	4.01	16.54	
T_{SETUP} (FSMC_FFs)	0.05	0.46	

5.7 GMAC timing characteristics

This section describes the AC timing characteristics for the Giga/Fast Ethernet port. The GMAC is designed to support 10, 100 and 1000 Mbps Ethernet/IEEE 802.3 networks. It supports GMII, RMII and MII interfaces.

Note: For the pin list of the supported interfaces, see Table 5: MAC Ethernet port multiplexing scheme and Table 15: Connectivity - MAC PHY interface signals description.

5.7.1 GMII transmit timing characteristics

The timing characterization is performed assuming an output load capacitance of 10 pF on the output pads and using PLL2 as internal clock source or MAC_GTXCLK125 as external clock source for GMII TX interface timings extraction.

These timings are valid for 10, 100 and 1000 Mbps operation.

Figure 25. GMII TX timing waveform

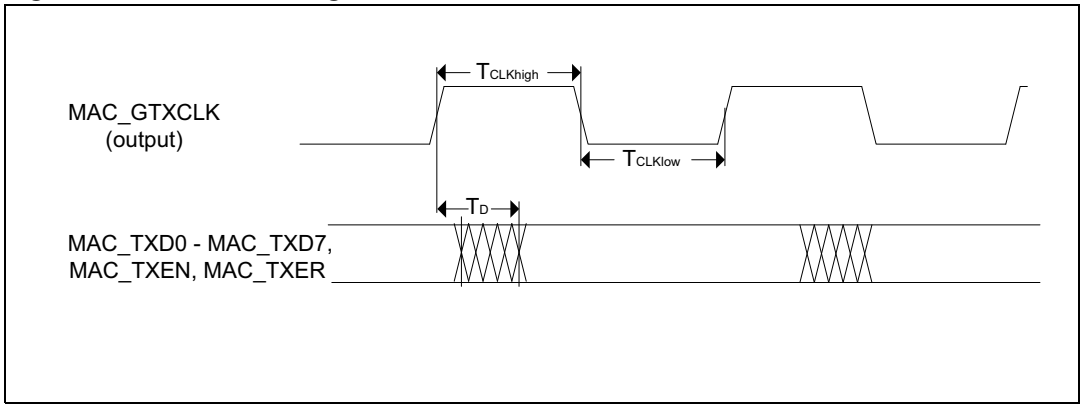


Table 73. GMII TX timing characteristics

Parameter	Description	Conditions(1)	Min	Max	Unit
T_{CLK}	MAC_GTXCLK clock period		8		ns
$T_{CLKhigh}$	MAC_GTXCLK pulse high	Clock source= MAC_GTXCLK125@125 MHz (50% ideal duty cycle)	1.5		ns
T_{CLKlow}	MAC_GTXCLK pulse low		1.0		ns
$T_{CLKhigh}$	MAC_GTXCLK pulse high	Clock source= MAC_GTXCLK125@250 MHz internally divided by 2	2.1		ns
T_{CLKlow}	MAC_GTXCLK pulse low		1.4		ns
$T_{CLKhigh}$	MAC_GTXCLK pulse high	Clock source= PLL2	2.2		ns
T_{CLKlow}	MAC_GTXCLK pulse low		1.2		ns
T_D	MAC_GTXCLK to GMII output data		0.4	5.6	ns

1. Characterizations based on external clock sources are performed assuming an ideal 50% duty cycle clock.

5.7.2 GMII receive timing characteristics

The timing characterization is performed assuming an input transition of 2 ns on all the inputs and using MAC_RXCLK as source of clock for GMII RX interface timings extraction.

Figure 26. GMII RX timing waveform

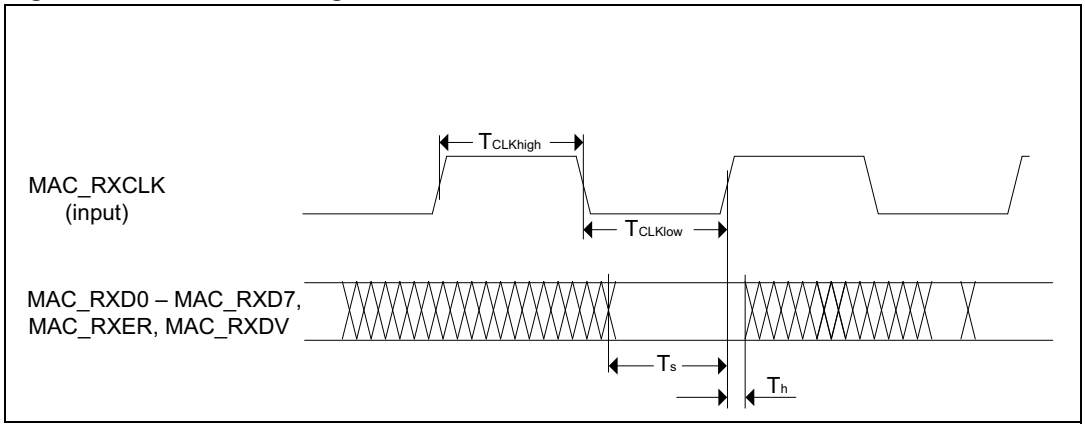


Table 74. GMII RX timing characteristics

Parameter	Description[1]	Min	Max	Unit
T_{CLK}	MAC_RXCLK clock period	8	–	ns
$T_{CLKhigh}$	MAC_RXCLK pulse high	2.5	–	ns
T_{CLKlow}	MAC_RXCLK pulse low	2.5	–	ns
t_{setup} (T_s)	Setup time for GMII receive data	4		ns
t_{hold} (T_h)	Hold time for GMII receive data	0.5		ns

1. Characterizations based on external clock sources are performed assuming an ideal 50% duty cycle clock.

5.7.3 MII transmit timing characteristics

The timing characterization is performed assuming an output load capacitance of 10 pF on the output pads and using a 2 ns transition on MAC_TXCLK for interface timings extraction.

These timings are valid for 10 and 100 Mbps operation.

Figure 27. MII TX timing waveform

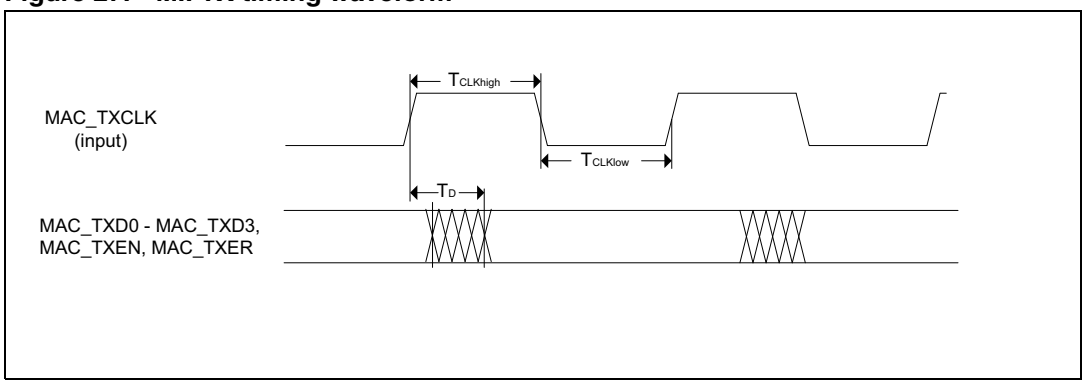


Table 75. MII TX timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	MAC_TXCLK clock period	40	–	ns
$T_{CLKhigh}$	MAC_TXCLK pulse high	12	–	ns
T_{CLKlow}	MAC_TXCLK pulse low	12	–	ns
T_D	MAC_TXCLK to MII output data	5.1	18	ns

5.7.4 MII receive timing characteristics

The timing characterization is performed assuming an input transition of 2 ns on all the inputs.

These timings are valid for 10 and 100 Mbps operation.

Figure 28. MII RX timing waveform

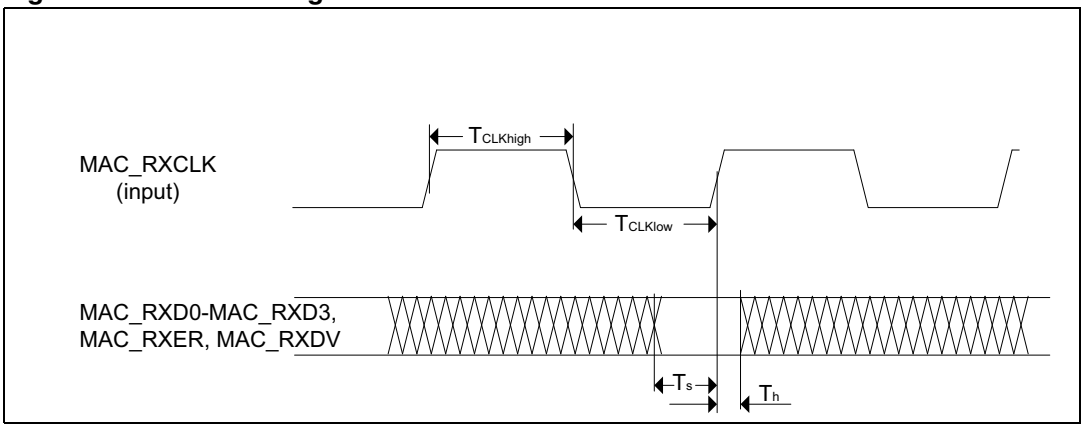


Table 76. MII RX timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	MAC_RXCLK clock period	40	–	ns
$T_{CLKhigh}$	MAC_RXCLK pulse high	12	–	ns
T_{CLKlow}	MAC_RXCLK pulse low	12	–	ns
T_s	Setup time for MII receive data	3.8		ns
T_h	Hold time for MII receive data	0		

5.7.5 MAC Ethernet asynchronous signals timing characteristics (MAC_CRS and MAC_COL)

MAC_CRS and MAC_COL signals are used only by the GMII and MII interfaces.

Figure 29. MAC asynchronous input signals timing waveform

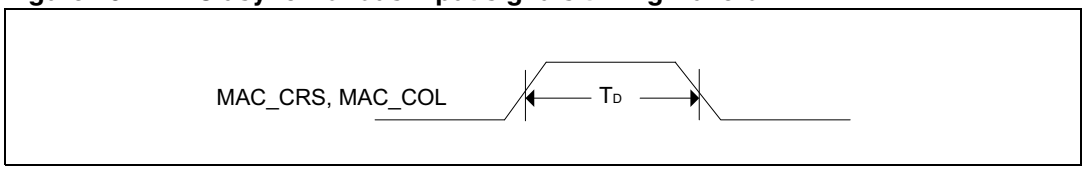


Table 77. MAC asynchronous input signals timing characteristics

Symbol	Description	Min	Max	Unit
T_D	MAC_CRS to MAC_COL minimum pulse width	3	-	ns

5.7.6 MAC serial management channel timing characteristics (MDIO/MDC)

The MAC_MDIO and MAC_MDC signals are used to perform serial management channel timing.

The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However, MAC can function correctly with a maximum MDC frequency of 15 MHz.

Figure 30. MAC_MDC/MAC_MDIO timing waveform

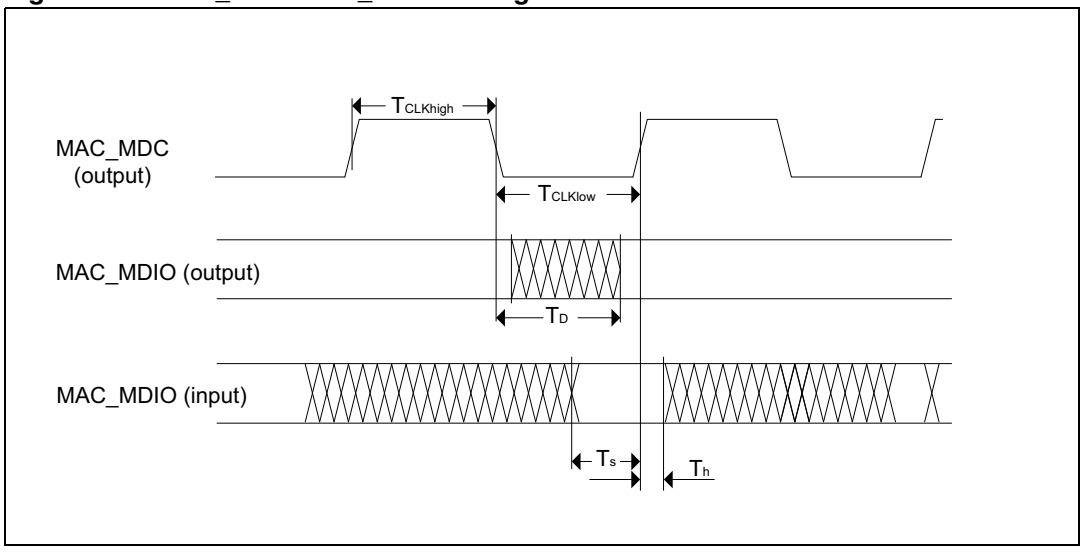


Table 78. MAC_MDC/MAC_MDIO timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	MAC_MDC clock period	200	–	ns
T_D	Falling edge of MDC to MDIO output delay(1)	10	20	ns
$T_{CLKhigh}$	MAC_MDC pulse width high	60		ns

Table 78. MAC_MDC/MAC_MDIO timing characteristics (continued)

Symbol	Description	Min	Max	Unit
T_{CLKlow}	MAC_MDC pulse width low	60		ns
T_s	Setup time for MDIO input	30		ns
T_h	Hold time for MDIO input	0		ns

1. When MDIO is used as output, the data is launched on the falling edge of the clock as shown in *Figure 30*.

5.8 GPIO/XGPIO timing characteristics

For edge-sensitive signals, the interrupt line is sampled by flip flops clocked by PCLK for GPIOs and HCLK for XGPIOs, the APB and AHB clocks, normally running at 83 MHz and 166 MHz respectively.

The minimum pulse width required for interrupt detection on signal edge is:

$3*T_{PCLK}$ (36 ns at 83 MHz) for GPIO

$3*T_{HCLK}$ (18 ns at 166 MHz) for XGPIO

5.9 I2C timing characteristics

The timing of high and low level of SCL (TSCLHigh and TSCLLow) are programmable.

Figure 31. I2C timing waveform

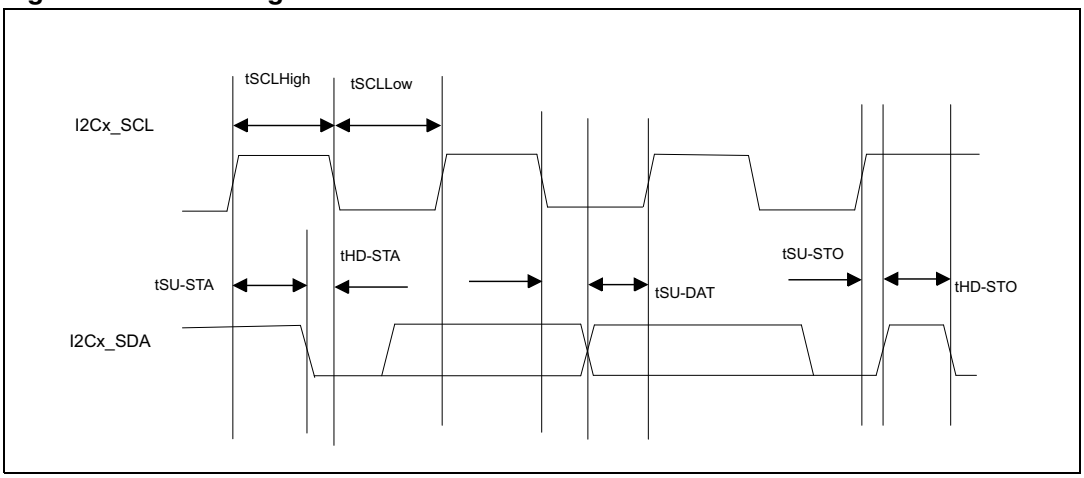


Table 79. Timing characteristics for I2C in High-Speed mode

Parameter	Min(1)
T_{SU-STA}	(HS_SCL_HCNT+7)*T_{HCLK}
T_{HD-STA}	(HS_SCL_LCNT+2)*T_{HCLK}
T_{SU-DAT}	TSCLLow - $T_{HD-DATmax}$
T_{HD-DAT}	(IC_SDA_HOLD)* T_{HCLK}
T_{SU-STO}	(FS_SCL_HCNT+7)*T_{HCLK}
T_{HD-STO}	685*T_{HCLK}

1. HS_SCL_HCNT = 10, HS_SCL_LCNT = 33, FS_SCL_HCNT = 183, FS_SCL_LCNT = 233, IC_SDA_HOLD=1

T_{HCLK} is the clock period of the HCLK internal clock. The frequency is programmable, for details refer to the RCG section of *RM0078, Reference manual, SPEAr1340 architecture and functionality*.

Table 80. Time characteristics for I2C in Fast-Speed mode

Parameter	Min(1)
T_{SU-STA}	(SCL_HCNT+7)*T_{HCLK}
T_{HD-STA}	(SCL_HCNT+3)*T_{HCLK}
T_{SU-DAT}	T_{SCLLow} - $T_{HD-DATmax}$
T_{HD-DAT}	(IC_SDA_HOLD)* T_{HCLK}
T_{SU-STO}	(SCL_HCNT+7)*T_{HCLK}
T_{HD-STO}	685*T_{HCLK}

1. SCL_HCNT = 183, SCL_LCNT = 233 IC_SDA_HOLD=1

Table 81. Timing characteristics for I2C in Standard-Speed mode

Parameter	Min(1)
T_{SU-STA}	(SCL_LCNT+7)*T_{HCLK}
T_{HD-STA}	(SCL_HCNT+3)*T_{HCLK}
T_{SU-DAT}	T_{SCLLow} - $T_{HD-DATmax}$
T_{HD-DAT}	(IC_SDA_HOLD)* T_{HCLK}
T_{SU-STO}	(SCL_HCNT+7)*T_{HCLK}
T_{HD-STO}	685*T_{HCLK}

1. SCL_HCNT = 664, SCL_LCNT = 780 IC_SDA_HOLD=1

For the I2C working as SLAVE, the only significant parameters are TSU-DAT and THD-DAT.

5.10 I2S timing characteristics

This section describes the timing characteristics for the two I2S digital audio ports (I2S_IN and I2S_OUT).

The timing characterization is performed assuming an input transition of 2 ns on all the inputs, an output load capacitance of 10 pF on all outputs and using PLL1 as source of I2S OUT_BITCLK with a nominal period of 40 ns.

I2S transmit timing characteristics

Figure 32. I2S transmit timing waveform

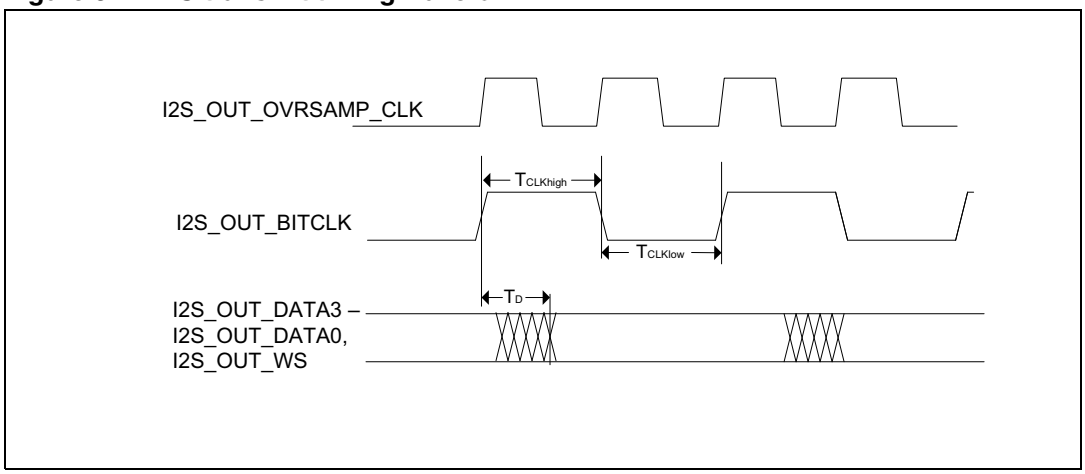


Table 82. I2S transmit timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	I2S_OUT_BITCLK clock period	40	–	ns
$T_{CLKhigh}$	I2S_OUT_BITCLK pulse high	15	–	ns
T_{CLKlow}	I2S_OUT_BITCLK pulse low	15	–	ns
f_{OVRCLK}	I2S_OUT_OVERSAMP_CLK frequency	$f_{I2S\_OUT\_BITCLK}/2$		
$T_{OVRCLKhigh}$	I2S_OUT_OVERSAMP_CLK pulse high	7.5	–	ns
$T_{OVRCLKCLKlow}$	I2S_OUT_OVERSAMP_CLK pulse low	7.5	–	ns
T_D	I2S_OUT_BITCLK to I2S_OUT data delay	13	30	ns

I2S receive timing characteristics

Figure 33. I2S receive timing waveform

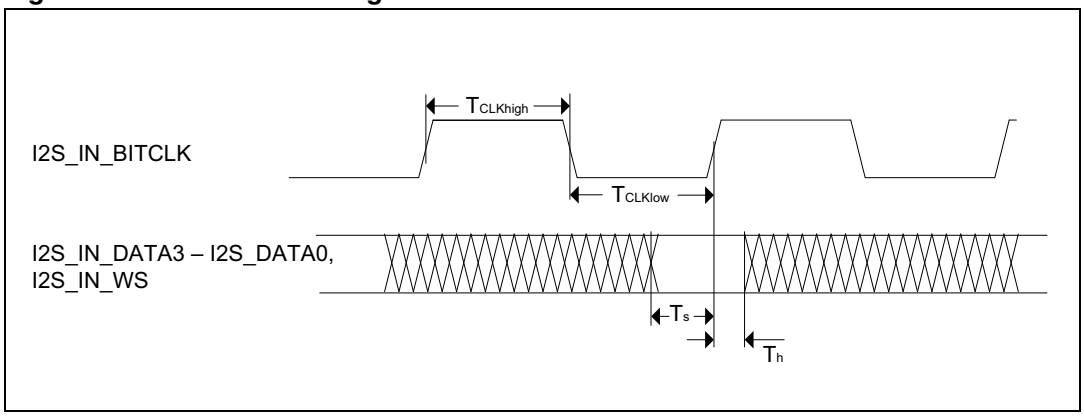


Table 83. I2S receive timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	I2S_IN_BITCLK clock period	40	–	ns
$T_{CLKhigh}$	I2S_IN_BITCLK pulse high	15	–	ns
T_{CLKlow}	I2S_IN_BITCLK pulse low	15	–	ns
T_s	I2S_IN_DATA, I2S_IN_WS Setup time	6		ns
T_h	I2S_IN_DATA, I2S_IN_WS hold time	0		ns

5.11 MCIF timing characteristics

5.11.1 Synchronous mode (SD/SDIO/MMC)

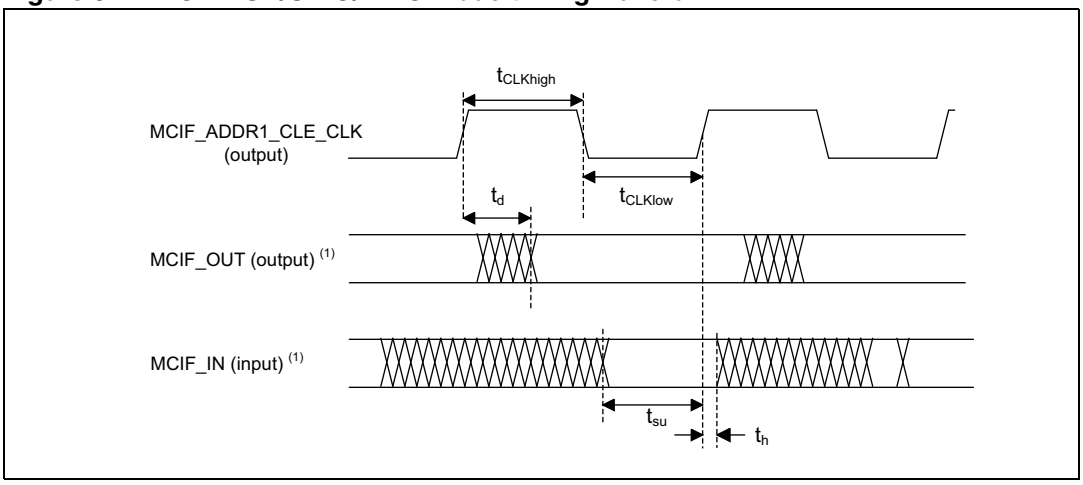
This section describes the timing characteristics for MCIF when interfacing SD/SDIO/MMC synchronous memories.

The tables below show the timings for the high-speed and full-speed modes.

The timing characterization is performed assuming an output load capacitance of 10 pF on all the outputs, an input transition of 2ns on all the inputs and using PLL1 as source of the clock used for the timings extraction.

The MCI_ADDR_CLE_CLK signal is programmable via the MCIF registers. Refer to *RM0089, Reference manual, SPEAr1340 address map and registers*

Figure 34. MCIF - SD/SDIO/MMC mode timing waveform



1. MCIF_OUT/MCIF_IN synchronous signals: MCIF_DATA0, MCIF_DATA[7..4], MCIF_DATAx_SD (x= 1..3), MCIF_SD_CMD

Table 84. MCIF - SD/SDIO High speed mode timing characteristics

Symbol	Description	Min	Max	Unit
t_{CLK}	MCIF_ADDR1_CLE_CLK clock period	20	–	ns
$t_{CLKhigh}$	MCIF_ADDR1_CLE_CLK pulse high	t_{CLK}/2-1	–	ns
t_{CLKlow}	MCIF_ADDR1_CLE_CLK pulse low	t_{CLK}/2-1	–	ns
t_D	MCIF_ADDR1_CLE_CLK to MCIF_OUT output delay	0.2	6.1	ns
t_s	Setup time for MCIF_IN data	14		ns
t_h	Hold time for MCIF_IN data	1.3		ns

Table 85. MCIF - SD/SDIO Full speed mode timing characteristics

Symbol	Description	Min	Max	Unit
t_{CLK}	MCIF_ADDR1_CLE_CLK clock period	40	–	ns
$t_{CLKhigh}$	MCIF_ADDR1_CLE_CLK pulse high	t_{CLK}/2-1	–	ns

Table 85. MCIF - SD/SDIO Full speed mode timing characteristics (continued)

Symbol	Description	Min	Max	Unit
t_{CLKlow}	MCIF_ADDR1_CLE_CLK pulse low	t_{CLK}/2-1	–	ns
t_D	MCIF_ADDR1_CLE_CLK to MCIF_OUT output delay	20.1	25.9	ns
t_s	Setup time for MCIF_IN data	14		ns
t_h	Hold time for MCIF_IN data	0		ns

Table 86. MCIF - MMC High speed mode timing characteristics

Symbol	Description	Min	Max	Unit
t_{CLK}	MCIF_ADDR1_CLE_CLK clock period	20	–	ns
$t_{CLKhigh}$	MCIF_ADDR1_CLE_CLK pulse high	t_{CLK}/2-1	–	ns
t_{CLKlow}	MCIF_ADDR1_CLE_CLK pulse low	t_{CLK}/2-1	–	ns
t_D	MCIF_ADDR1_CLE_CLK to MCIF_OUT output delay	0.2	6.1	ns
t_s	Setup time for MCIF_IN data	14		ns
t_h	Hold time for MCIF_IN data	1.3		ns

Table 87. MCIF - MMC Full speed mode timing characteristics

Symbol	Description	Min	Max	Unit
t_{CLK}	MCIF_ADDR1_CLE_CLK clock period	40	–	ns
$t_{CLKhigh}$	MCIF_ADDR1_CLE_CLK pulse high	t_{CLK}/2-1	–	ns
t_{CLKlow}	MCIF_ADDR1_CLE_CLK pulse low	t_{CLK}/2-1	–	ns
t_D	MCIF_ADDR1_CLE_CLK to MCIF_OUT output delay	20.1	25.9	ns
t_s	Setup time for MCIF_IN data	14		ns
t_h	Hold time for MCIF_IN data	0		ns

5.11.2 CompactFlash true IDE PIO mode/UDMA mode

This section describes the timing characteristics for MCIF when interfacing CompactFlash in true IDE mode PIO mode and UDMA mode.

The data in *Table 88* has been measured in the following configuration:

- True IDE PIO mode = Mode 6
- HCLK period = 6 ns
- CF/XD (clk_xin) base clock period obtained by programming the MISC register MCIF_CFXD_CLK_SYNT.
- $T_{clk\_xin} = T$
- t0 is the minimum total cycle time. t0 must satisfy the following constraint

  t0 ≥ t2 + t2i

  t2 is the minimum command active time.

  t2i is the minimum command active recovery time or command inactive time.

Figure 35. MCIF - CF true IDE PIO mode waveform

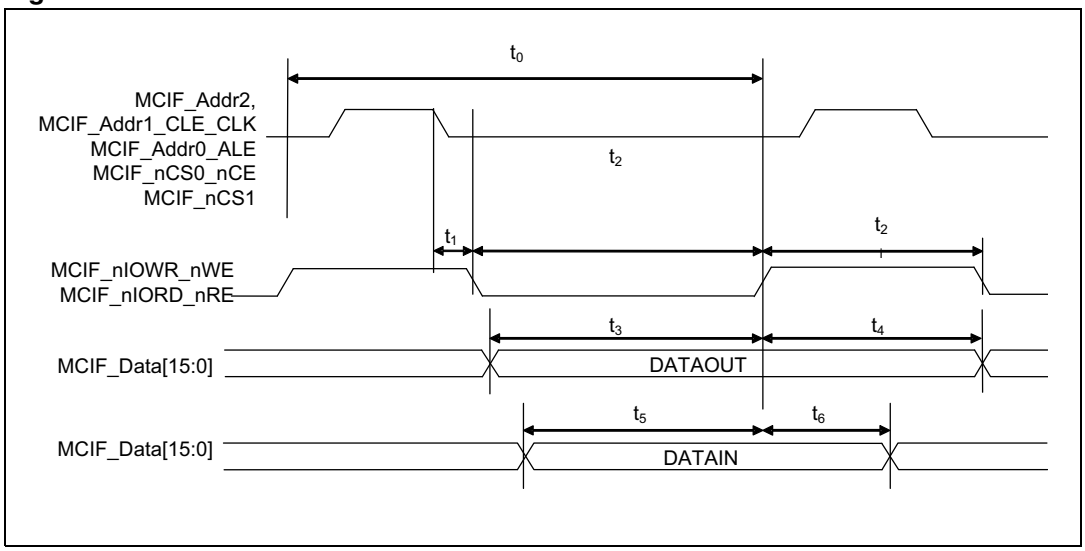


Table 88. MCIF - CF true IDE PIO mode timing characteristics

Symbol	Description	Min	Max	Unit
t_0	Cycle time	18*T		ns
t_1	Address Valid to IORD/IOWR setup	2*T		ns
t_2	IORD/-IOWR	10*T		ns
t_{2i}	IORD/-IOWR recovery time	8*T		ns
t_3	IOWR data setup	9.5*T		ns
t_4	IOWR data hold	T - 3.2		ns
t_5	IORD data setup	5(1)		ns
t_6	IORD data hold	4(1)		ns

1. t5 and t6 are the minimum timing requirements the external card has to respect in order to ensure correct Read Data sampling inside SPEAr1340.

Figure 36. MCIF - CF true IDE UDMA mode waveform

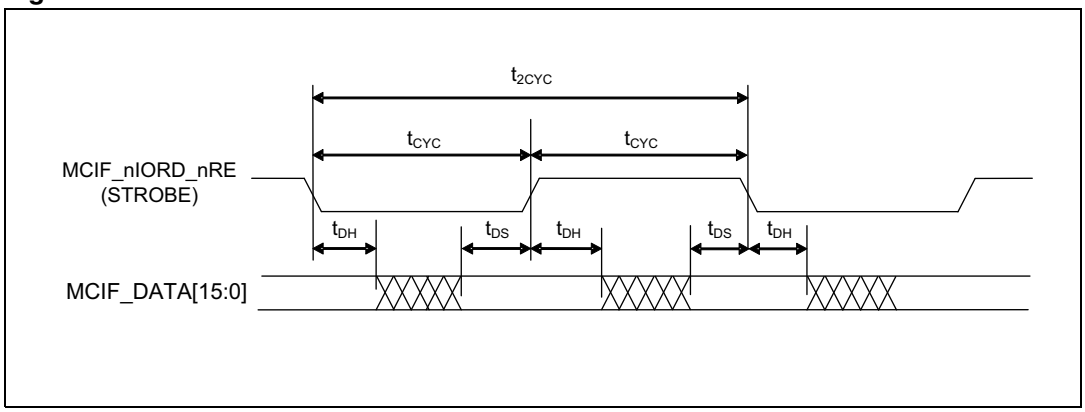


Table 89. TrueIDE Ultra DMA timing characteristics

Symbol	Item	Min	Max	Unit
t_{DH}	Data hold time (from STROBE edge until data become invalid)	T		ns
t_{DS}	Data setup time (the time from data valid until STROBE edge)	2*T		
t_{CYC}	Cycle time (the time from STROBE edge to STROBE edge)	$>t_{DH}+t_{DS}=3*T$		
t_{2CYC}	Two cycle times (the time from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	$2*t_{CYC}>6*T$		

5.12 MPMC timing characteristics

This section describes the timing characteristics for the multiport DDR controller. The DDR interface is designed to support the following standards:

- DDR3-800 and DDR3-1066 standards, as defined in the JESD79-3E JEDEC standard.
- All DDR2 standards: DDR2-1066, DDR2-800, DDR2-667, DDR2-533, DDR2-400.

Note: For more information on JEDEC standards, refer to JEDEC Website: www.jedec.org.

This section provides the timing specifications for DDR3 and for DDR2.

For DDR3 the timing values reported below can been obtained only upon successfully completing the procedure of leveling. Leveling is mandatory for the fly-by topology used for SDRAM cuts on the PCB. The fly-by topology for the commands, addresses, control signals, and clocks allows better signal integrity.

For DDR2 you have to use a T branch topology and you have to calibrate the board without the support of the leveling.

The DDR PHY is an 8-clock sampling-based architecture. The eight clocks are equally delayed across a clock period equal to the PHY's core clock. The clocks are generated from dedicated internal DLLs (dll_clocks).

The timings have been calculated in best and worst case, without considering the pads contribution. These are the operating conditions used for the characterization:

- In worst case: V=1.10 V, T=125 ° C
- In best case: V=1.30 V, T= -40 ° C

ADDR/CTRL timing characteristics

The memory clock (mem_clk) is derived from a fixed dedicated PLL output. Address and control signals (mem_ctl) are launched on the negative edge of the mem_clk (+/- 1/8 * Tmem_clk) in order to have the control signals centered on the rising edge of the clock at memory side (assuming the same board flight-time delay for mem_clk and mem_ctl).

The address and control signals have the same output stage, but they present a skew of about 114 ps due to the physical implementation.

For a frequency of 533.3 MHz, the period of the clock is T_{CLK} = 1.875 ns.

Table 90. ADDR/CTRL timing characteristics

Symbol	Description	Value	Unit
T_{CLK}	Mem_clk period	1.875	ns
T_s	Setup time for ADDR/CTRL receive data	589	ps
T_h	Hold time for ADDR/CTRL receive data	824	ps

The setup time is calculated considering:

- maximum error = 235 ps
- maximum data skew = 114 ps

Ts calculation formula

Ts= Tclk/2–data_skew –max_error= 938 ps – 114 ps – 235 ps= 589 ps

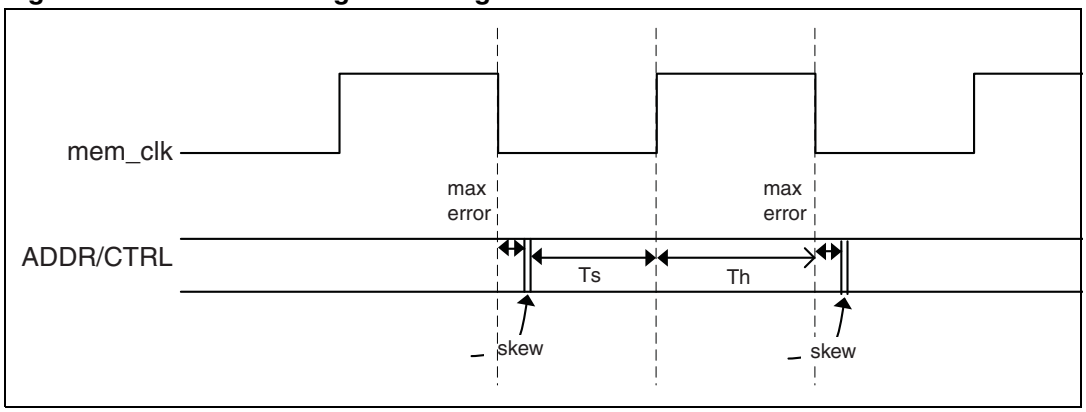
The hold time, instead, is calculated considering:

- maximum error = 0 ps
- maximum data skew = 114 ps

Th calculation formula

Th= Tclk/2–data_skew + max_error= 938 ps – 114 ps + 0 ps= 824 ps

Figure 37. ADDR/CTRLsignals timing waveform

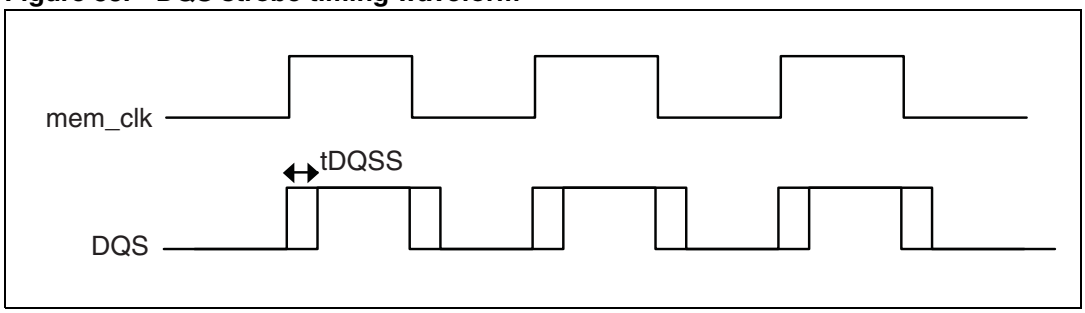


Write DQS timing characteristics

The DDR3 SDRAM supports a write-leveling feature to allow the controller to compensate the skew between the mem_clk and the data strobe (DQS) at each memory cut. During the write leveling phase, the controller uses the feedback from the DDR3 SDRAM to adjust the DQS to mem_clk relationship. The DQS delay established through this procedure helps to ensure tDQSS specifications in systems using a fly-by topology by deskewing the trace length mismatch. Based on the 8-phase PHY architecture, the DQS signal is derived from one of the eight dll_clocks, so it is adjustable with a minimum step of 1/8 of the clock period (max_error). The sampled value coming from the memory is processed so that the tDQSS value can vary from 0 to 1/8 Tclk (see *Figure 38*).

For the DDR2 you have to find the right alignment without the write-leveling support.

Figure 38. DQS strobe timing waveform



Write DQ/DM timing characteristics

Similar to the creation of the write DQS signal, the write DQ/DM signals are created through a clock derived from one of the eight dll_clocks.

The clock generating DQ/DM signals should always be set two phases before the clock generating DQS. This would ensure a 90-degree phase difference between DQ and DQS. Due to the path delay difference between DQ and DQS, the maximum error respect to the ideal case is one phase off, so the max error is 1/8 Tclk.

The maximum skew among the DQ/DM signals in a single data slice is about 30 ps.

For a frequency of 533.3 MHz, the period of the clock is T_{CLK}= 1.875 ns.

Table 91. DQ/DM signals timing characteristics

Symbol	Description	Value	Unit
T_{CLK}	Mem_clk period	1.875	ns
T_s	Setup time for DQ/DM receive data	204	ps
T_h	Hold time for DQ/DM receive data	439	ps

The setup time is calculated considering:

- maximum error = 235 ps
- maximum data skew = 30 ps

Ts calculation formula

Ts= Tclk/4–data_skew –max_error= 469 ps – 30 ps – 235 ps= 204 ps

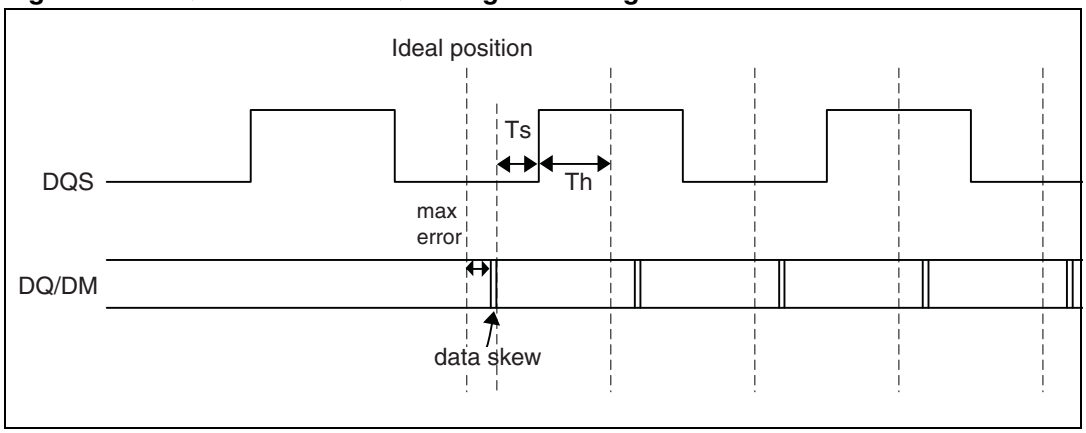
The hold time, instead, is calculated considering:

- maximum error = 0 ps
- maximum data skew = 30 ps

Th calculation formula

Th= Tclk/4–data_skew + max_error= 469 ps – 30 ps + 0 ps= 439 ps

Figure 39. DQS strobe and DQ/DM signals timing waveform



Read DQS and DQ timing characteristics

The DDR PHY is a sampling-based architecture; this means that the incoming DQS and DQ signals are sampled by each of the eight dll_clocks. DM signals are not used for reading.

For DQS strobe, a pattern of “000111” is used to detect a rising edge and a pattern of “111000” is used to detect a falling edge. The maximum error to detect these edges is 1/8 Tclk.

The incoming DQ data is sampled, then the sampled data is analyzed in a window of 4 sampled bits relative to detected DQS edges. The maximum skew, without the contribution of the pads, between the DQ signals in a single data slice is about 20 ps.

For a frequency of 533.3 MHz, the period of the clock is T_{CLK}= 1.875 ns.

Table 92. DQS and DQ signals timing characteristics

Symbol	Description	Value	Unit
T_{CLK}	Mem_clk period	1.875	ns
T_s	Setup time for DQS/DQ receive data	214	ps
T_h	Hold time DQS/DQ receive data	449	ps

The setup time is calculated considering:

- maximum error = 235 ps
- maximum data skew = 20 ps

Ts calculation formula

Ts= Tclk/4–data_skew –max_error= 469 ps – 20 ps – 235 ps = 214 ps

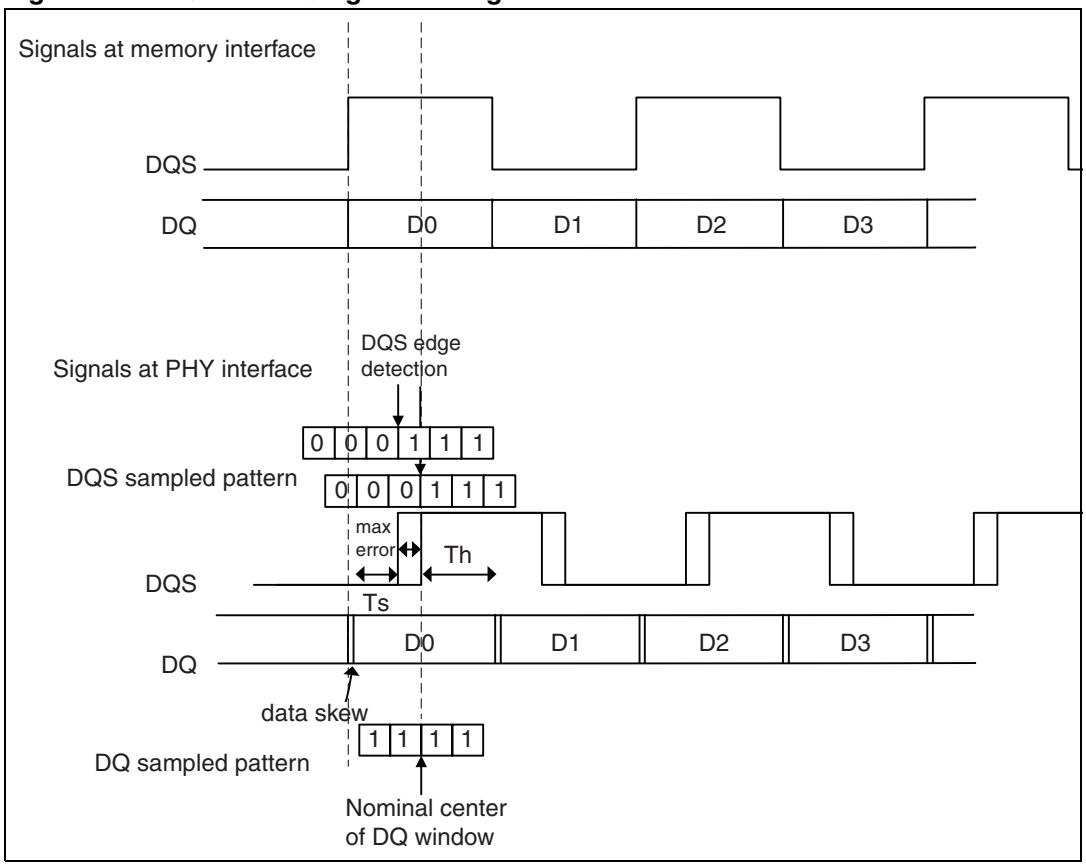
The hold time, instead, is calculated considering:

- maximum error = 0 ps
- maximum data skew = 20 ps

Th calculation formula

Th= Tclk/4-data_skew + max_error= 469 ps – 20 ps + 0 ps = 449 ps

Figure 40. DQS and DQ signals timing waveform



5.13 PWM timing characteristics

This section describes the timing characteristics of the four PWM generators.

The timing characterization is performed assuming an output load capacitance of 2 to 10 pF on the four outputs.

Table 93. PWM timing characteristics

Symbol	Parameter	Min	Max	Unit
t_w	Pulse width (T= programmed pulse width)	T– 2.2	T+ 2.2	ns

5.14 SMI timing characteristics

This section describes the timing characteristics of the serial NOR Flash controller.

The timing characterization is performed assuming an output load capacitance of 10 pF on all outputs, an input transition of 2ns on all the inputs and using PLL1 as source of the clock for the timing extraction.

Figure 41. SMI timing waveform

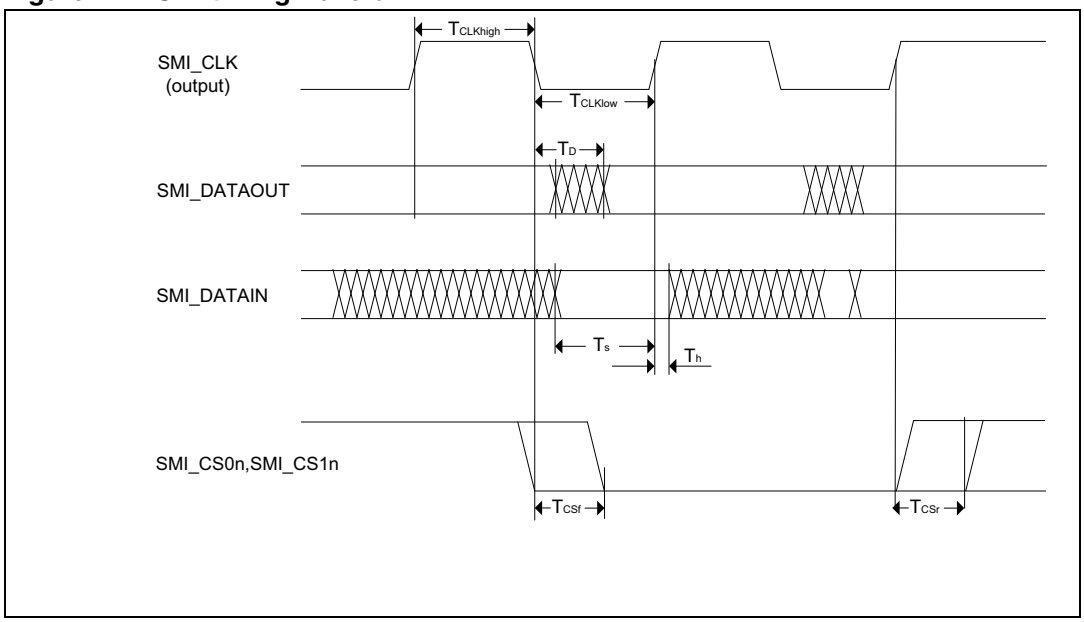


Table 94. SMI timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	SMI_CLK clock period	24	–	ns
$T_{CLKhigh}$	SMI_CLK output pulse high	T/2 - 1	–	ns
T_{CLKlow}	SMI_CLK output pulse low	T/2 - 1	–	ns
T_D	SMI_CLK out to SMI_DATAOUT output delay	0.81	9.65	ns
T_s	Setup time for SMI_DATAIN data	3.72	–	ns
T_h	Hold time for SMI_DATAIN data	-6.46	–	ns

Table 94. SMI timing characteristics (continued)

Symbol	Description	Min	Max	Unit
T_{CSf}	Min and max delay of falling edge of SMI_CLK to falling edge of SMI_CS0n and SMI_CS1n	0.75	9.60	ns
T_{CSr}	Min and max delay of rising edge of SMI_CLK to rising edge of SMI_CS0n and SMI_CS1n (1)	0.75+T_{HCLK}	9.60+T_{HCLK}	ns

1. T_{HCLK} is the period of the programmable HCLK clock

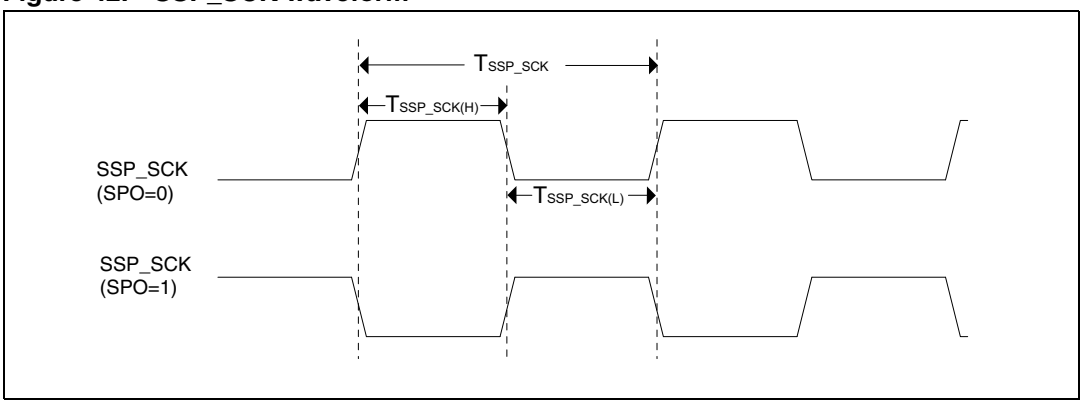
5.15 SSP timing characteristics

This section describes the timing characteristics of the synchronous serial port.

The timing characterization is performed assuming an input transition of 2 ns on all the inputs and an output load capacitance of 10 pF on all outputs and using PLL1 as the clock source for the timing extraction.

Note: The characterization of the SSP has been done using the SPI protocol.

Figure 42. SSP_SCK waveform



The clock polarity parameter (SPO) indicates the state of the clock signal when it is idle. This can be programmed in the SSPCR0 register (refer to *RM0089, Reference manual, SPEAr1340 address map and registers*).

SPO= 0 The clock idle state is low.

SPO= 1 The clock idle state is high.

5.15.1 SPI master mode timings

SSP_SCK is the SPI output clock. The SSP_SCK frequency is programmable and derived from PCLK, for details refer to the SSP section of the *RM0078, Reference manual, SPEAr1340 architecture and functionality*.

Table 95. SPI master mode timing characteristics of SSP_SCK

Symbol	Parameters	Min	Max	Unit
T_{SSP_SCK}	SSP_SCK clock period	48	Programmable	ns
$T_{SSP\_SCK(H)}$	SSP_SCK clock high pulse width	$(T_{SSP\_SCK}/2) - 1$	$(T_{SSP\_SCK}/2) + 1$	
$T_{SSP\_SCK(L)}$	SSP_SCK clock low pulse width	$(T_{SSP\_SCK}/2) - 1$	$(T_{SSP\_SCK}/2) + 1$	

Figure 43. SPI master mode external timing waveform (SPH= 0, SPO =0)

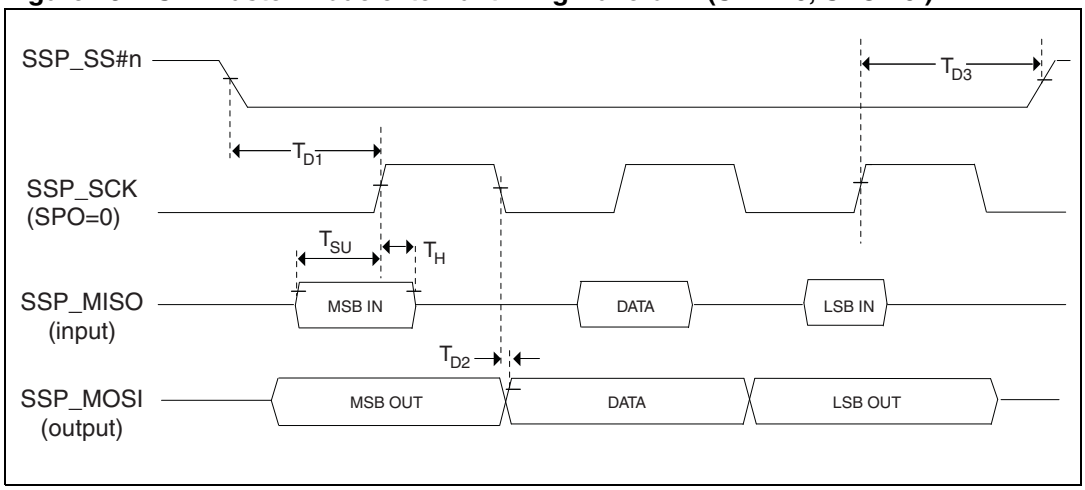


Table 96. SPI master mode timing characteristics (SPH = 0, SPO=0)

Symbol	Parameters	Min	Max	Unit
T_{SU}	Setup time, MISO (input) valid before SSP_SCK (output) rising edge	17		ns
T_H	Hold time, MISO (input) valid after SSP_SCK (output) rising edge	0		
T_{D1}	Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) rising edge	T_{SSP_SCK}-8	T_{SSP_SCK}-2	ns
T_{D2}	Delay time, SSP_SCK (output) falling edge to MOSI (output) transition	-4.64	12.4	ns
T_{D3}	Delay time, SSP_SCK (output) rising edge to SSP_SS#n (output) rising edge	T_{SSP_SCK} + 2	T_{SSP_SCK} +8	

Figure 44. SPI master mode external timing waveform (SPH= 0, SPO =1)

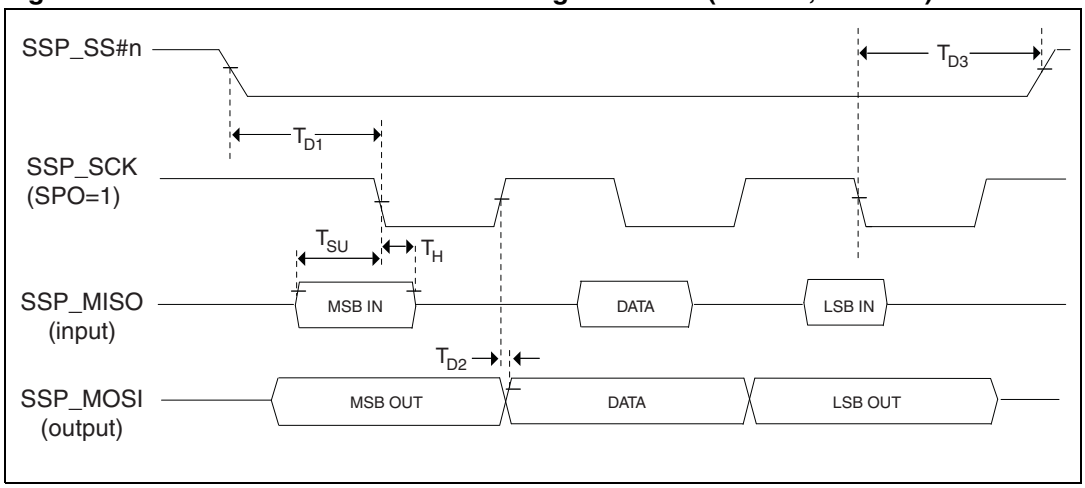


Table 97. SPI master mode timing characteristics (bit SPH = 0, SPO=1)

Symbol	Parameters	Min	Max	Unit
T_{SU}	Setup time, MISO (input) valid before SSP_SCK (output) falling edge	17.8		ns
T_H	Hold time, MISO (input) valid after SSP_SCK (output) falling edge	0		
T_{D1}	Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) falling edge	T_{SSP_SCK}-8	T_{SSP_SCK}-2	ns
T_{D2}	Delay time, SSP_SCK (output) rising edge to MOSI (output) transition	-3.8	12.5	ns
T_{D3}	Delay time, SSP_SCK (output) falling edge to SSP_SS#n (output) rising edge	T_{SSP_SCK} + 2	T_{SSP_SCK} +8	

Figure 45. SPI master mode external timing waveform (SPH = 1, SPO = 0)

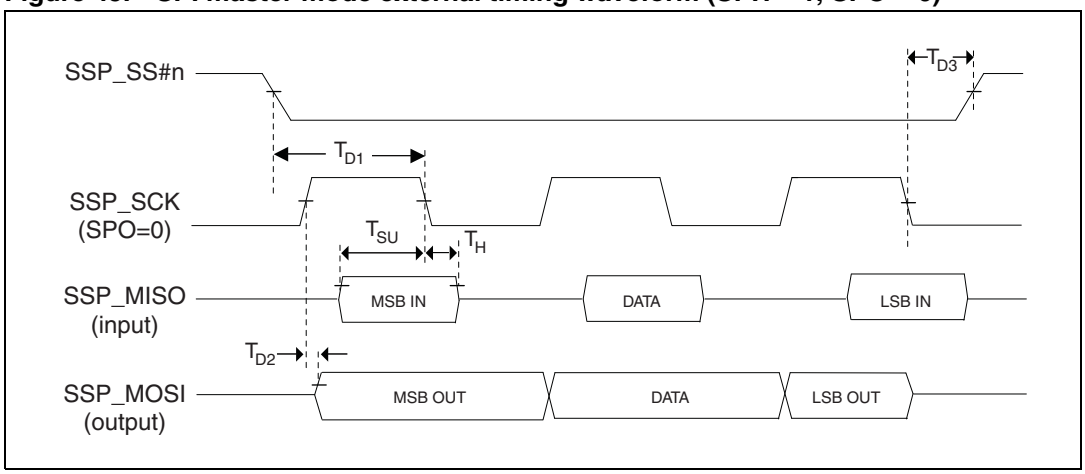


Table 98. SPI master mode timing characteristics (clock phase bit SPH = 1, SPO=0)

Symbol	Parameters	Min	Max	Unit
T_{SU}	Setup time, MISO (input) valid before SSP_SCK (output) falling edge	17.8		ns
T_H	Hold time, MISO (input) valid after SSP_SCK (output) falling edge	0		
T_{D1}	Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) falling edge	T_{SSP_SCK}-8	T_{SSP_SCK}-2	ns
T_{D2}	Delay time, SSP_SCK (output) rising edge to MOSI (output) transition	-3.8	12.5	ns
T_{D3}	Delay time, SSP_SCK (output) falling edge to SSP_SS#n (output) rising edge	T_{SSP_SCK} + 2	T_{SSP_SCK} +8	

Figure 46. SPI master mode external timing waveform (SPH = 1, SPO = 1)

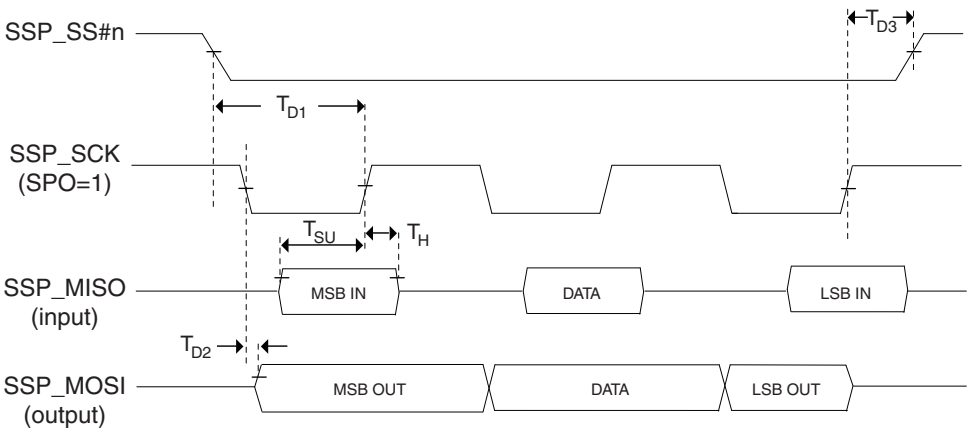


Table 99. SPI master mode timing characteristics (clock phase bit SPH = 1, SPO=1)

Symbol	Parameters	Min	Max	Unit
T_{SU}	Setup time, MISO (input) valid before SSP_SCK (output) rising edge	17		ns
T_H	Hold time, MISO (input) valid after SSP_SCK (output) rising edge	0		
T_{D1}	Delay time, SSP_SS#n (output) falling edge to first SSP_SCK (output) rising edge	T_{SSP_SCK}-8	T_{SSP_SCK}-2	ns
T_{D2}	Delay time, SSP_SCK (output) falling edge to MOSI (output) transition	-4.64	12.4	ns
T_{D3}	Delay time, SSP_SCK (output) rising edge to SSP_SS#n (output) rising edge	T_{SSP_SCK} + 2	T_{SSP_SCK} +8	

5.15.2 SPI slave mode timings

Table 100. SSP timing characteristics (slave mode)

Symbol	Parameters	Min	Max	Unit
T_{SSP_SCK}	SSP_CLK_IN input clock period	12 * T_{PCLK}	254 * 256 * T_{PCLK}	ns
$T_{SSP\_SCK(H)}$	SSP_SCK clock high pulse width	(T_{SSP_SCK} - T_{PCLK})/2		
$T_{SSP\_SCK(L)}$	SSP_SCK clock low pulse width	(T_{SSP_SCK} - T_{PCLK})/2		
T_{SU}	Data input setup time	4 * T_{SSP_SCK}		
T_H	Data input hold time	0		
T_D	Data output delay	3 * T_{SSP_SCK}	4 * T_{SSP_SCK}	

5.16 UART timing characteristics

$t_{UARTCLK} = 1/f_{UARTCLK}$ with $f_{UARTCLK}$ in MHz

$f_{BAUDRATE}$ = the programmed baud rate frequency

For information related to baud rate generation, refer to:

- *Section 2.14: UART ports*.
- *RM0078, Reference manual, SPEAr1340 architecture and functionality*

Figure 47. UART transmit and receive waveform

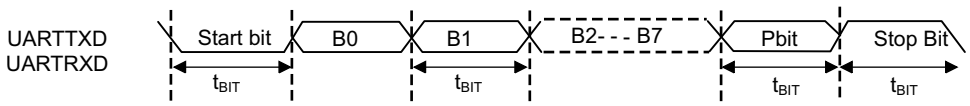


Table 101. UART transmit timing characteristics

Symbol	Parameters	Min	Max	Unit
t_{BIT}	UART duration of transmit data bit (B0..B7), Parity bit (Pbit), Start bit, Stop bits	$1/f_{baudrate} - t_{UARTCLK} -1$	$1/f_{baudrate} + t_{UARTCLK} +1$	ns

Table 102. UART receive timing characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
t_{BIT}	Pulse duration of receive data bit (B0 ..B7), Parity bit (Pbit), Start bit, Stop bits(1)	Baudrate = 6 Mbps	$1/f_{baudrate} - (t_{UARTCLK}/2)$	$1/f_{baudrate} + (t_{UARTCLK}/2)$	ns
			$1/f_{baudrate} -1/(16*f_{baudrate})$	$1/f_{baudrate} + (16*f_{baudrate})$	ns

1. The time margin is with respect to a single bit accumulation and not with respect to the whole UART frame. The start bit is sampled after the 8th baud cycle after a low is detected at input, Subsequently, each bit is sampled at consecutive 16 baud cycles.

Note: The above min. and max. values allow a deviation of ±1 baud cycle in a single bit time. The accumulated deviation of a UART character frame must not exceed $3/(16*f_{baudrate})$.

5.16.1 IrDA timing characteristics

Figure 48 and *Figure 49* show timing waveforms based on 1 start bit, 5 data bits and 1 stop bit.

$f_{BAUDRATE}$ = the programmed baud rate frequency

$t_{UARTCLK} = 1/f_{UARTCLK}$

Figure 48. IrDA transmit timing waveform

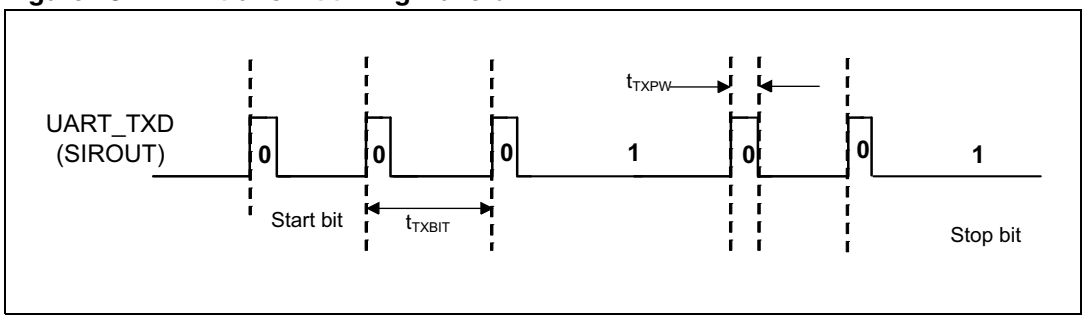


Table 103. IrDA transmit timing characteristics

Symbol	Parameter	Min	Max	Unit
t_{TXBIT}	IrDA transmit mode bit duration	$1/f_{baudrate} - t_{UARTCLK} -1$	$1/f_{baudrate} + t_{UARTCLK} +1$	ns
t_{TXPW}	IrDA transmit mode pulse width, start bit data bit value 0 (high pulse)	$(3/16)*1/f_{baudrate} - t_{UARTCLK} -1$	$(3/16)*1/f_{baudrate} + t_{UARTCLK} +1$	

Figure 49. IrDA receive timing waveform

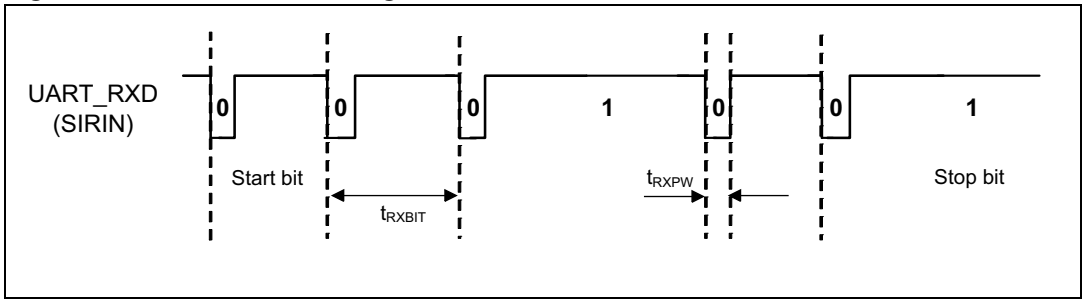


Table 104. IrDA receive timing characteristics

Symbol	Parameter	Min	Max	Unit
t_{RXBIT}	IrDA receive mode bit duration	$1/f_{baudrate} - t_{UARTCLK} -1$	$1/f_{baudrate} + t_{UARTCLK} +1$	ns
t_{RXPW}	IrDA receive mode pulse width, start bit data bit value 0 (low pulse)	$(3/16)*1/f_{baudrate}$		

5.17 VIP timing characteristics

This section describes the timing characteristics of the video input parallel block.

The timing characterization is performed assuming an input transition of 2 ns on all the inputs and using VIP_PIXCLK as source of the clock for the timings extraction.

Figure 50. VIP timing waveform

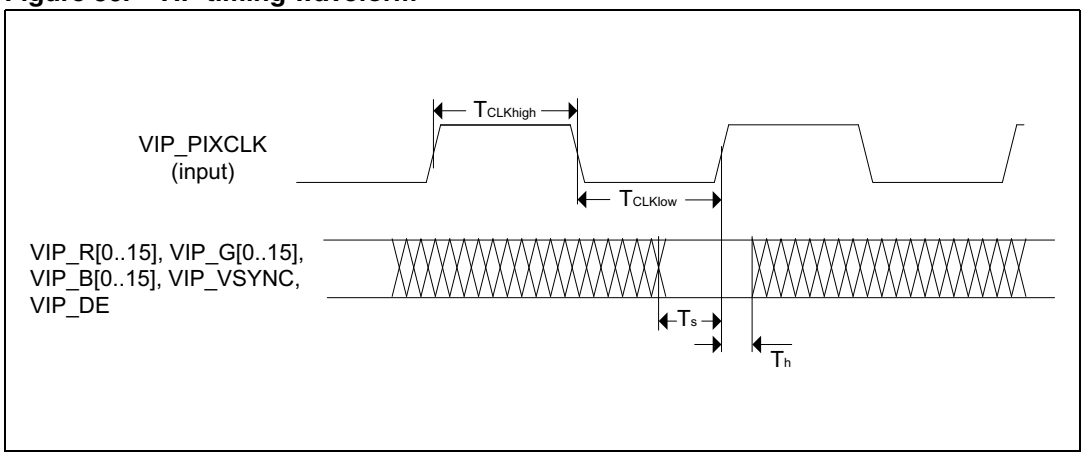


Table 105. VIP timing characteristics

Symbol	Description	Min	Max	Unit
T_{CLK}	VIP_PIXCLK clock period	6.5	–	ns
$T_{CLKhigh}$	VIP_PIXCLK pulse high	2.9	–	ns
T_{CLKlow}	VIP_PIXCLK pulse low	2.9	–	ns
T_s	Setup time for VIP data	6		ns
T_h	Hold time for VIP data	-0.71		ns

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 106. PGBA (23 x 23 mm, 0.8 mm pitch) package mechanical data

Dimensions						
Ref.	Databook (mm)			Drawing (mm)		
	Min	Typ	Max	Min	Typ	Max
A			2.06	1.80	1.93	2.06
A1	0.24			0.30	0.40	0.50
A2		0.56			0.56	
A4		0.97			0.97	
b	0.40	0.50	0.60	0.40	0.50	0.60
D	22.80	23.00	23.20	22.80	23.00	23.20
D1		21.60			21.60	
D2		20.00			20.00	
E	22.80	23.00	23.20	22.80	23.00	23.20
E1		21.60			21.60	
E2		20.00			20.00	
e		0.8			0.8	
F		0.7			0.7	
ddd			0.20			0.20
eee			0.25			0.25
fff			0.10			0.10

Figure 51. PGBA package - top view

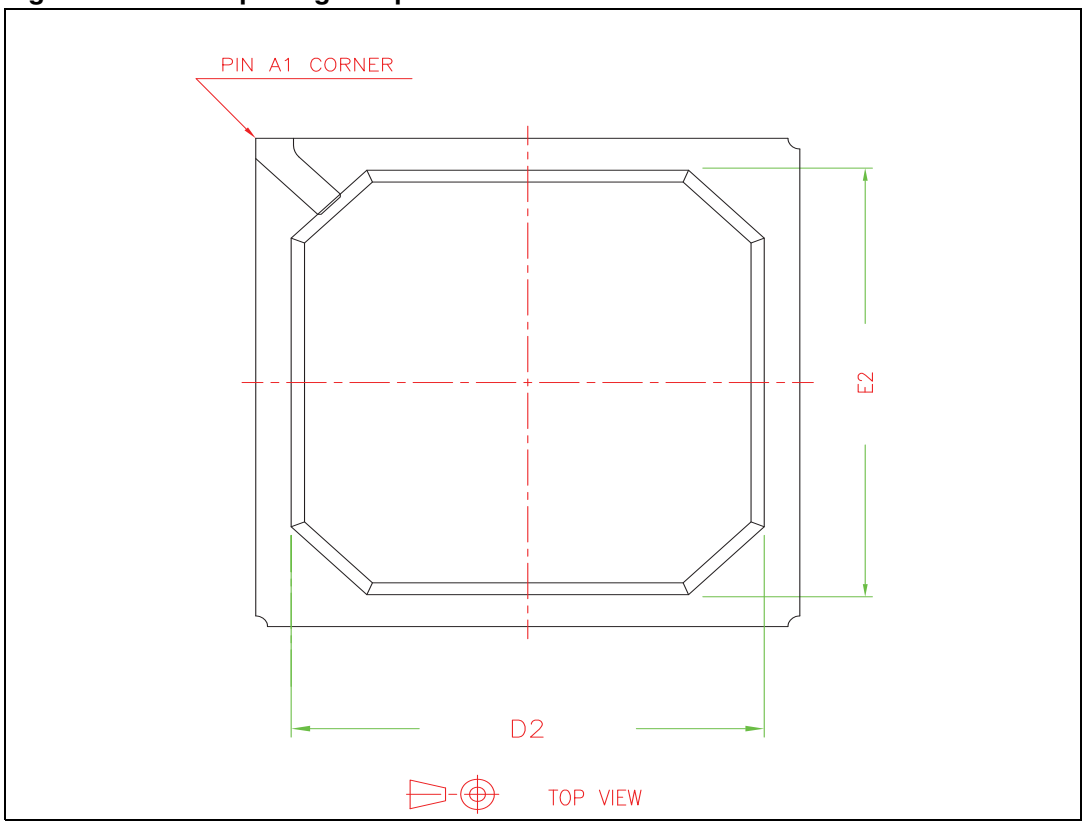


Figure 52. PGBA package - bottom view

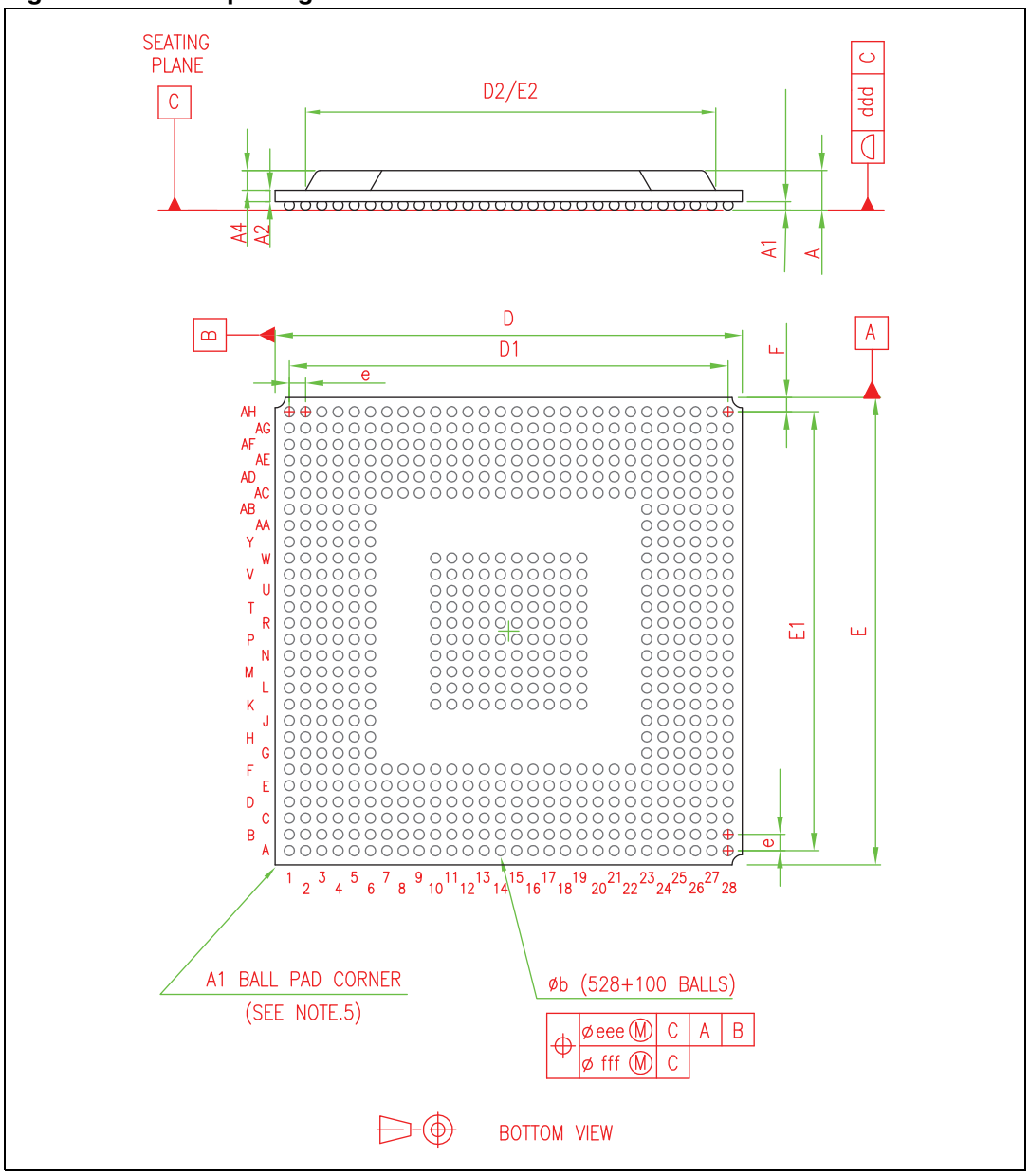


Table 107. PGBA (23 x 23 mm, 0.8 mm pitch) package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA} (1)	Thermal resistance junction-to-ambient	16.5	°C/W
Θ_{JB}	Thermal resistance junction-to-board	9	
Θ_{JC}	Thermal resistance junction-to-case	5	
Ψ_{JC}	Junction-to-case thermal characterisation parameter	0.23	

1. Measured on JESD51 2s2p test board.

Appendix A Acronyms

Table 108. List of acronyms

Acronym	Definition
ACP	Accelerator coherence port
ADC	Analog-to-digital converter
AES	Advanced encryption standard
AHB	AMBA high speed bus
AMBA	Advanced microcontroller bus architecture
AMP	Asymmetric multiprocessing
APB	Advanced peripheral bus
BIST	Built-In self test
CBC	Cipher block chaining
CF	Compact flash
CMOS	Complimentary metal-oxide semiconductor
CPU	Central processing unit
CRC	Cyclic redundancy check
DDR	Double data rate
DES	Data encryption standard
DLL	Delay locked loop (when applied to DDR memories)
DMA	Direct memory access
EMI	External memory interface
EP	Endpoint
ETM	Embedded trace macrocell
FIFO	First-in-first-out
FIQ	Fast interrupt request
FPGA	Field programmable gate array
FSMC	Flexible static memory controller
GB	Giga bytes
GMII	Gigabit media independent interface
GPIO	General purpose input / output
GPU	Graphics processing unit
HLOS	High-level operating system
HMI	Human machine interface
HW	Hardware
IrDA	Infrared data association

Table 108. List of acronyms (continued)

Acronym	Definition
IRQ	Interrupt request
JPEG	Joint photographic experts group
JTAG	Joint test action group
KB	Kilo bytes
LCD	Liquid color display
LSB	Least significant bit
MAC	Media access control
MB	Mega bytes
MCU	Microcontroller unit
MD5	Message digest 5
MII	Media independent interface
MMC	Multimedia card
MMU	Memory management unit
MSB	Most significant bit
ODT	On-die termination
OTG	On-the-go (USB)
PCIe	PCI express
PHY	Physical (device, transceiver, layer)
PLL	Real-time operating system
PTM	Program trace macrocell
PWM	Pulse width modulation
RAM	Random access memory
RAS	Reconfigurable array subsystem
RC	Root complex
RF	Radio frequency
RFU	Reserved for future use
RGMII	Reduced gigabit media independent interface
RISC	Reduced instruction set computing
RMII	Reduced media independent interface
ROM	Read only memory
RTC	Real-time clock
RTOS	Real-time operating system
RX	Receive
SATA	Serial ATA
SHA-1	Secure hash algorithm

Table 108. List of acronyms (continued)

Acronym	Definition
SIR	Serial InfraRed
SMI	Serial memory interface
SMP	Symmetric multiprocessing
SoC	System-on-chip
SPI	Serial peripheral interface
SPP	Standard parallel port
SRAM	Static RAM
SSP	Synchronous serial port
SSTL	Stub series terminated logic
SW	Software
TCM	Tightly coupled memory
TFT	Thin film transistor, a display technology
TTL	Transistor-transistor logic
TX	Transmit
UART	Universal asynchronous receiver transmitter
USB	Universal serial bus
VIC	Vectored interrupt controller
WDT	Watchdog timer
xD	Extreme digital (card standard)

Appendix B Copyright statement

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7 Revision history

Table 109. Document revision history

Date	Revision	Changes
05-Apr-2012	1	Initial release.
03-Aug-2012	2	*Features* – Added SD interface to bullet *"1x memory card interface"*. – Changed the bullet related to LCD from *"LCD display controller, up to 1920 x 1200,60 Hz, 24 bpp"* to *"LCD display controller, incl.support for Full HD, 1920 x 1080, 60 Hz, 24 bpp"*. – Added new sub-bullets *"Secure boot support"* and *"JTAG disable option"* under *"Security"* security. *Chapter 6: Package information* Updated *Table 107: PGBA (23 x 23 mm, 0.8 mm pitch) package thermal characteristics*: – Changed Θ_{JB} value from 8.2 to 9 °C/W. – Added Θ_{JA} and Ψ_{JC} values. – Added footnote. – Changed table title. *Chapter 2: Device functions* *Section 2.14: UART ports*: – Deleted bullet "Support baud rate up to UARTCLK_max_freq/16". – Changed bullet *"Programmable by software"* to *"Programmable by software: up to 125 MHz with a maximum baud rate of 7.81 Mbps (125/16)."* *Section 2.17: A/D converter (ADC)*: Changed bullet : *"10-bit resolution"* to *"10-bit resolution for the analog cell which can be extended up to 17 bits with embedded oversampling techniques performed by the controller"*. *Section 2.24: Camera input interfaces (CAM)*: Changed the numbering of CAMx from "CAM0, CAM1, CAM2 and CAM3" into "CAM1, CAM2, CAM3 and CAM4". *Section 2.23: Video encoder (VENC)*: updated the features. *Section 2.19: General purpose I/O (GPIO/XGPIO)*: Added information about XGPIO169 in the first bullet of *"XGPIO main features"* section. *Section 2.37: Temperature sensor (THSENS)*: – Moved 'offset-related' bullet closer to 'measurement range' bullet as they are related. – Removed reference to "calibration" from the 'offset-related' bullet. *Section 2.2: Multilayer interconnect matrix (BUSMATRIX)*: Corrected a typo error in *"Single interrupt for outband signaling"* bullet. *Section 2.3.1: BootROM*: added SD/MMC to the list of booting devices. *Section 2.1: CPU subsystem*:

Table 109. Document revision history (continued)

Date	Revision	Changes
03-Aug-2012	2 (cont'd)	Replaced *"Parity support to detect internal memory failures during runtime"* by *"Parity support to detect runtime failures for other internal memories"*. *Section 2.34: Clock and reset system*: corrected a typo error in bullet *"PLL2 programmable dithered PLL, dedicated for the 125 MHz clock of the Gigabit Ethernet MACs"* *Section 2.4: Multiport DDR controller (MPMC)*: Split bullet *"Exclusive and locked accesses support weighted round-robin arbitration scheme support to ensure high memory bandwidth utilization"* into 2 separate ones. *Section 2.9: Giga/Fast Ethernet port (GMAC)*: Deleted the phrase: *"note that this timing information is shared between the two Giga Ethernet controllers to provide highest precision in "bridging" operations"*, since only one Giga Ethernet controller is available. *Section 2.10: PCI Express controller (PCIe)*: updated the introduction. *Section 2.26: I2S digital audio ports (I2S)*: removed bullet *"External SCLK gating and enable signal"*, as SCLK is an internal signal. *Section 2.27: S/PDIF digital audio port*: removed bullet *"Can detect IEC-61937 compressed data"* and related footnote from the 'input' features group. *Section 2.20: LCD display controller (CLCD)*: replaced bullet *"Programmable pixel clock frequency up to bus clock frequency"* by *"Programmable pixel clock frequency up to 148MHz (1080p resolution)"*. *Section 2.22: Video decoder (VDEC)*: – Updated the bullet *"H.263 profile and level"* as follows: - added the image size limitation to Profile 0 - deleted sub-bullet *"Sorenson Spark"* and added it as a separate bullet – Split bullet "VP6, VP7 and VP8, versions 0-3" into two bullets: - *VP6 and VP7, versions 0-3* - *VP8 version 2 (WebM)* – Added sub-bullet *"Baseline interleaved"* to bullet *"JPEG, all common sampling formats"*. – Bullet *"Input image size"*: added limitation to standalone mode. – Bullet *"Image cropping / digital zoom"*: added limitation *"Usable only for JPEG or stand-alone mode"*. *Section 2.29: Cryptographic co-processor (C3)*: – Removed numerical IDs (such as ID: 0x00001020). – Removed Channel 7: empty bullet. *Section 2.32: General purpose timers (GPT)*: corrected "8-bit timer clock prescaler" to "4-bit timer clock prescaler" in the first two bullets. *Section 2.19: General purpose I/O (GPIO/XGPIO)*: updated the first paragraph of introduction. *Section 2.22: Video decoder (VDEC)*: – Changed *"Supported video profiles"* to *"Supported video codecs"*. – Updated bullet *"H.264 profile and level"*.

Table 109. Document revision history (continued)

Date	Revision	Changes
03-Aug-2012	2 (cont'd)	*Section 2.38: One-time programmable antifuse (OTP)*: updated Bank M description. Updated *Section 2.6: Flexible static memory controller (FSMC)*. *Section 2.4: Multiport DDR controller (MPMC)*: added a note at the first bullet referring to a limitation of maximum memory address space usage. *Section 2.24: Camera input interfaces (CAM)*: added a note about feature capability. *Section 2.37: Temperature sensor (THSENS)*: – Changed measurement of junction temperature starting value from 0 to 20 ° C. – Added typical correction value. *Chapter 3: Pin description* Updated the introduction. *Table 3: Ball characteristics*: – Modified the power supply for USB_UOC_ID from "USB_UOC_VDD3V3" to "USB_VDD2V5". – Modified the power supply for USB_UOC_VBUS from "USB_UOC_VDD3V3" to "5V". – Added a footnote about XGPIO169 Inserted description for SPDIF_IN and SPDIF_OUT in *Table 27: Audio - S/PDIF signals description*. Updated footnote under *Figure 6: SPEAr1340 multiplexing scheme*. Added a footnote to *Table 16: Connectivity - PCIe/SATA physical interface (MIPHY) signals description*. Updated STRAP5 description in *Table 37: Strapping options*. Added a footnote related to chip selection and booting in *Table 11: Memories - FSMC signals description*, *Table 12: Memories - SMI signals description* and *Table 38: Hardware boot selection (STRAP[0..3])* *Table 19: Connectivity - USB 2.0 PHY signals description*: updated the description of USB_UOC_VBUS adding the phrase *"The voltage range is 0-5.25 V"*. *Chapter 4: Electrical characteristics* Added a reference to AN3317 Application note at the beginning of the chapter. *Section 4.3: Clocking parameters*: – Added *Table 42: MCLK oscillator characteristics* and new *Section : MCLK generated from an external clock source*. – Added *Table 44: RTC oscillator characteristics* and new *Section : RTC clock generated from an external clock source*. Changed I/O types from TTL1, TTL2, TTL3 and PCI/3V3 TTL to IOTYPE1, IOTYPE2, IOTYPE3 and IOTYPE4 (throughout document).

Table 109. Document revision history (continued)

Date	Revision	Changes
03-Aug-2012	2 (cont'd)	Updated *Section 4.4.1: 3V3/2V5/1V8 I/O buffers (IOTYPE1/IOTYPE2/IOTYPE3)* and *Section 4.4.2: IOTYPE4 I/O buffers*. Updated *Section 4.5: Voltage regulator characteristics*. Inserted *Section 4.7: Required external components* (moved from Pin description chapter). Added *Section 4.6: MiPHY characteristics* Updated *Section 4.10: Reset release*: – Updated the introduction. – Renamed and updated *Figure 14: Cold reset release*. – Added new *Figure 15: Warm reset release*. *Chapter 5: Timing characteristics* – Added new *Section 5.1: Reset timing characteristics*. – Updated the entire chapter (timing waveforms and tables for each IP) with new timing information. – Removed RGMII information (see SPEAr1340 Errata sheet for more information).
11-Oct-2012	3	Updated *Section 2.29: Cryptographic co-processor (C3)* Added infomation on compensation cells *Table 2: Headers/abbreviations* Added I/O compensation cell column to table *Table 3: Ball characteristics* Updated *Table 59: Reset timing characteristics* Updated *Section 5.7: GMAC timing characteristics* Corrected *Figure 34: MCIF - SD/SDIO/MMC mode timing waveform* Updated t2i in *Table 88: MCIF - CF true IDE PIO mode timing characteristics* Updated SSP *Figure 42*, *Table 100* added *Table 95* Updated T_{D3} in *Figure 43* and *Figure 44* Updated notes below tables in *Section 5.9: I2C timing characteristics* Corrected *Table 41: SMI timing waveform* Updated *Section 5.16: UART timing characteristics*
26-10-2012	4	Updated *Figure 15: Warm reset release on page 149* Updated *Table 100: SSP timing characteristics (slave mode)*

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