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74VCX162240

Low Voltage 16-Bit Inverting Buffer/Line Driver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in Outputs

General Description

The VCX162240 contains sixteen inverting buffers with 3-STATE outputs to be employed as a memory and address driver, clock driver, or bus oriented transmitter/ receiver. The device is nibble (4-bit) controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

The 74VCX162240 is designed for low voltage (1.4V to 3.6V) V_{CC} applications with I/O capability up to 3.6V. The 74VCX162240 is also designed with 26Ω series resistors in the outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74VCX162240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

■ 1.4V to 3.6V V_{CC} supply operation

■ 3.6V tolerant inputs and outputs

■ 26Ω series resistors in outputs

■ t_{PD}
    3.3 ns max for 3.0V to 3.6V V_{CC}

■ Power-off high impedance inputs and outputs

■ Supports live insertion and withdrawal (Note 1)

■ Static Drive (I_{OH}/I_{OL})
    ±12 mA @ 3.0V V_{CC}

■ Uses patented noise/EMI reduction circuitry

■ Latch-up performance exceeds 300 mA

■ ESD performance:
    Human body model > 2000V
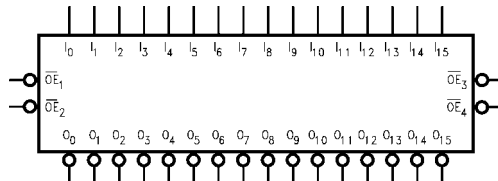   Machine model > 200V

Note 1: To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Descriptions
74VCX162240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
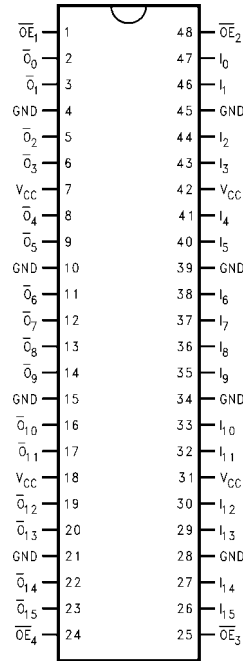
Logic Symbol

Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active LOW)
I_0—I_{15}	Inputs
$\overline{O}_0$—$\overline{O}_{15}$	Outputs

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Connection Diagram

Pin		Pin	
$\overline{OE}_1$	1	48	$\overline{OE}_2$
$\overline{O}_0$	2	47	I_0
$\overline{O}_1$	3	46	I_1
GND	4	45	GND
$\overline{O}_2$	5	44	I_2
$\overline{O}_3$	6	43	I_3
V_{CC}	7	42	V_{CC}
$\overline{O}_4$	8	41	I_4
$\overline{O}_5$	9	40	I_5
GND	10	39	GND
$\overline{O}_6$	11	38	I_6
$\overline{O}_7$	12	37	I_7
$\overline{O}_8$	13	36	I_8
$\overline{O}_9$	14	35	I_9
GND	15	34	GND
$\overline{O}_{10}$	16	33	I_{10}
$\overline{O}_{11}$	17	32	I_{11}
V_{CC}	18	31	V_{CC}
$\overline{O}_{12}$	19	30	I_{12}
$\overline{O}_{13}$	20	29	I_{13}
GND	21	28	GND
$\overline{O}_{14}$	22	27	I_{14}
$\overline{O}_{15}$	23	26	I_{15}
$\overline{OE}_4$	24	25	$\overline{OE}_3$

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	$\overline{O}_0$–$\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	$\overline{O}_4$–$\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	$\overline{O}_8$–$\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

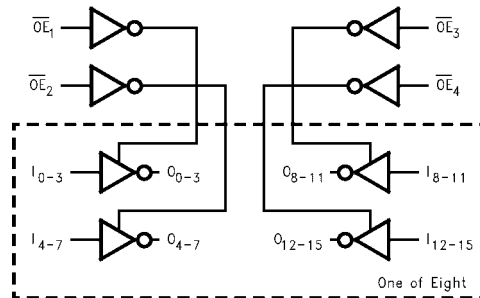| Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	$\overline{O}_{12}$–$\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial (HIGH or LOW, inputs may not float)
Z = High Impedance

Functional Description

The 74VCX162240 contains sixteen inverting buffers with 3-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of each other. The control pins may be shorted together to obtain full 16-bit operation.The 3-STATE outputs are controlled by an Output Enable ($\overline{OE}_n$) input. When $\overline{OE}_n$ is LOW, the outputs are in the 2-state mode. When $\overline{OE}_n$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the inputs.

Logic Diagram

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
Output Voltage (V_O)	
Outputs 3-STATED	−0.5V to +4.6V
Outputs Active (Note 3)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0V	−50.0 mA
DC Output Diode Current (I_{OK})	
V_O < 0V	−50.0 mA
V_O > V_{CC}	+50.0 mA
DC Output Source/Sink Current	
(I_{OH}/I_{OL})	±50.0 mA
DC V_{CC} or GND Current per	
Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.4V to 3.6V
Data Retention Only	1.2V to 3.6V
Input Voltage	−0.3V to +3.6V
Output Voltage (V_O)	
Output in Active States	0V to V_{CC}
Output in 3-State	0.0V to 3.6V
Output Current in I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±12.0 mA
V_{CC} = 2.3V to 2.7V	±8.0 mA
V_{CC} = 1.65V to 2.3V	±3.0 mA
V_{CC} = 1.4V to 1.6V	±2.0 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10.0 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{IH}	HIGH Level Input Voltage		2.7 – 3.6	2.0		V
			2.3 – 2.7	1.6		
			1.65 - 2.3	$0.65 \times V_{CC}$		
			1.4 - 1.6	$0.65 \times V_{CC}$		
V_{IL}	LOW Level Input Voltage		2.7 – 3.6		0.8	V
			2.3 – 2.7		0.7	
			1.65 - 2.3		$0.35 \times V_{CC}$	
			1.4 - 1.6		$0.35 \times V_{CC}$	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.7 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −6 mA	2.7	2.2		
		I_{OH} = −8 mA	3.0	2.4		
		I_{OH} = −12 mA	3.0	2.2		
		I_{OH} = −100 µA	2.3 – 2.7	V_{CC} − 0.2		
		I_{OH} = −4 mA	2.3	2.0		
		I_{OH} = −6 mA	2.3	1.8		
		I_{OH} = −8 mA	2.3	1.7		
		I_{OH} = −100 µA	1.65 - 2.3	V_{CC} − 0.2		
		I_{OH} = −3 mA	1.65	1.25		
		I_{OH} = −100 µA	1.4 - 1.6	V_{CC} − 0.2		
		I_{OH} = −1 mA	1.4	1.05		

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DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.7 – 3.6		0.2	
		I_{OL} = 6 mA	2.7		0.4	
		I_{OL} = 8 mA	3.0		0.55	
		I_{OL} = 12 mA	3.0		0.80	
		I_{OL} = 100 µA	2.3 – 2.7		0.2	
		I_{OL} = 6 mA	2.3		0.4	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 100 µA	1.65 - 2.3		0.2	
		I_{OL} = 3 mA	1.65		0.3	
		I_{OL} = 100 µA	1.4 - 1.6		0.2	
		I_{OL} = 1 mA	1.4		0.35	
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.4 - 3.6		±5.0	µA
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$ $V_I = V_{IH}$ or V_{IL}	1.4 - 3.6		±10.0	µA
I_{OFF}	Power-OFF Leakage Current	$0 \leq (V_I, V_O) \leq 3.6V$	0		10.0	µA
I_{CC}	Quiescent Supply Current	$V_I = V_{CC}$ or GND	1.4 - 3.6		20.0	µA
		$V_{CC} \leq (V_I, V_O) \leq 3.6V$ (Note 5)	1.4 - 3.6		±20.0	
ΔI_{CC}	Increase in I_{CC} per Input	$V_{IH} = V_{CC} -0.6V$	2.7 - 3.6		750	µA

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = -40°C$ to $+85°C$		Units	Figure Number
				Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay	C_L = 30 pF, R_L = 500Ω	3.3± 0.3	0.8	3.3	ns	Figures 1, 2
			2.5 ± 0.2	1.0	3.8		
			1.8 ± 0.15	1.5	7.6		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	15.2		Figures 5, 6
t_{PZL}, t_{PZH}	Output Enable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.8	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	5.1		
			1.8 ± 0.15	1.5	9.8		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	19.6		Figures 5, 7, 8
t_{PLZ}, t_{PHZ}	Output Disable Time	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3	0.8	3.6	ns	Figures 1, 3, 4
			2.5 ± 0.2	1.0	4.0		
			1.8 ± 0.15	1.5	7.2		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1	1.0	14.4		Figures 5, 7, 8
t_{OSHL} t_{OSLH}	Output to Output Skew (Note 7)	C_L = 30 pF, R_L = 500Ω	3.3 ± 0.3		0.5	ns	
			2.5 ± 0.2		0.5		
			1.8 ± 0.15		0.75		
		C_L = 15 pF, R_L = 2kΩ	1.5 ± 0.1		1.5		

**Note 6:** For C_L = 50$_P$F, add approximately 300 ps to the AC maximum specification.

Note 7: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = +25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	0.15	
			2.5	0.25	V
			3.3	0.35	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	−0.15	
			2.5	−0.25	V
			3.3	−0.35	
V_{OHV}	Quiet Output Dynamic Valley V_{OH}	C_L = 30 pF, V_{IH} = V_{CC}, V_{IL} = 0V	1.8	1.55	
			2.5	2.05	V
			3.3	2.65	

Capacitance

Symbol	Parameter	Conditions	$T_A = +25°C$ Typical	Units
C_{IN}	Input Capacitance	V_{CC} = 1.8, 2.5V or 3.3V, V_I = 0V or V_{CC}	6.0	pF
C_{OUT}	Output Capacitance	V_I = 0V or V_{CC}, V_{CC} = 1.8V, 2.5V or 3.3V	7.0	pF
C_{PD}	Power Dissipation Capacitance	V_I = 0V or V_{CC}, f = 10 MHz, V_{CC} = 1.8V, 2.5V or 3.3V	20.0	pF

AC Loading and Waveforms (V_{CC} 3.3V $\pm$ 0.3V to 1.8V $\pm$ 0.15V)
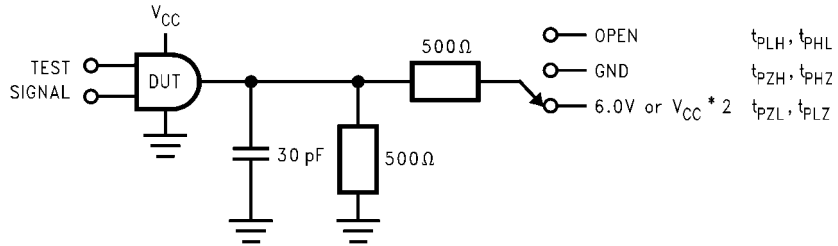
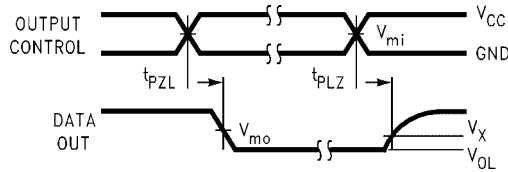| TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at V_{CC} = 3.3 $\pm$ 0.3V; V_{CC} x 2 at V_{CC} = 2.5 $\pm$ 0.2V; 1.8V $\pm$ 0.15V
t_{PZH}, t_{PHZ}	GND

FIGURE 1. AC Test Circuit
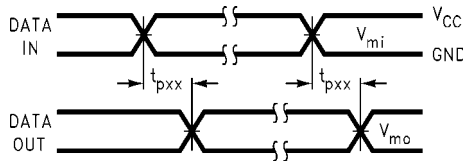
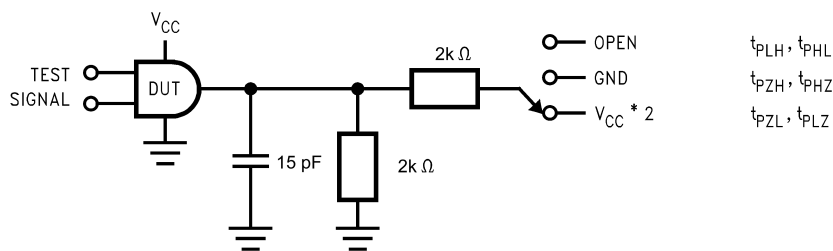**FIGURE 2. Waveform for Inverting and Non-Inverting Functions**
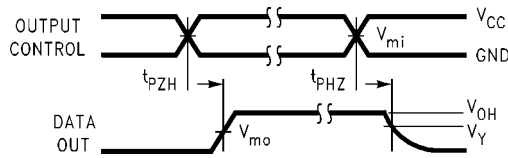
FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	2.5V $\pm$ 0.2V	1.8V $\pm$ 0.15V
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.15V
V_Y	V_{OH} – 0.3V	V_{OH} – 0.15V	V_{OH} – 0.15V

AC Loading and Waveforms (V$_{CC}$ 1.5V $\pm$ 0.1V)

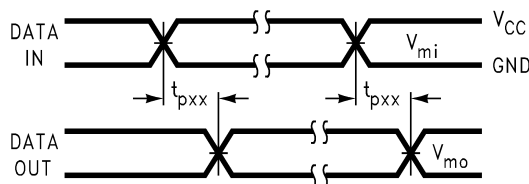| TEST	SWITCH
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	V$_{CC}$ x 2 at V$_{CC}$ = 1.5 $\pm$ 0.1V
t$_{PZH}$, t$_{PHZ}$	GND

FIGURE 5. AC Test Circuit

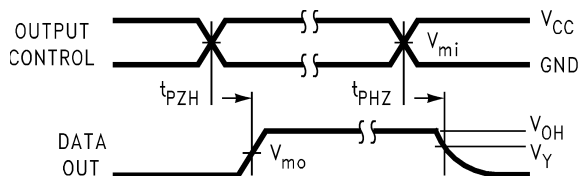**FIGURE 6. Waveform for Inverting and Non-Inverting Functions**

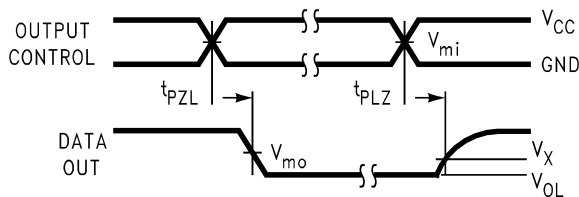**FIGURE 7. 3-STATE Output Enable and Disable Times for Low Voltage Logic**

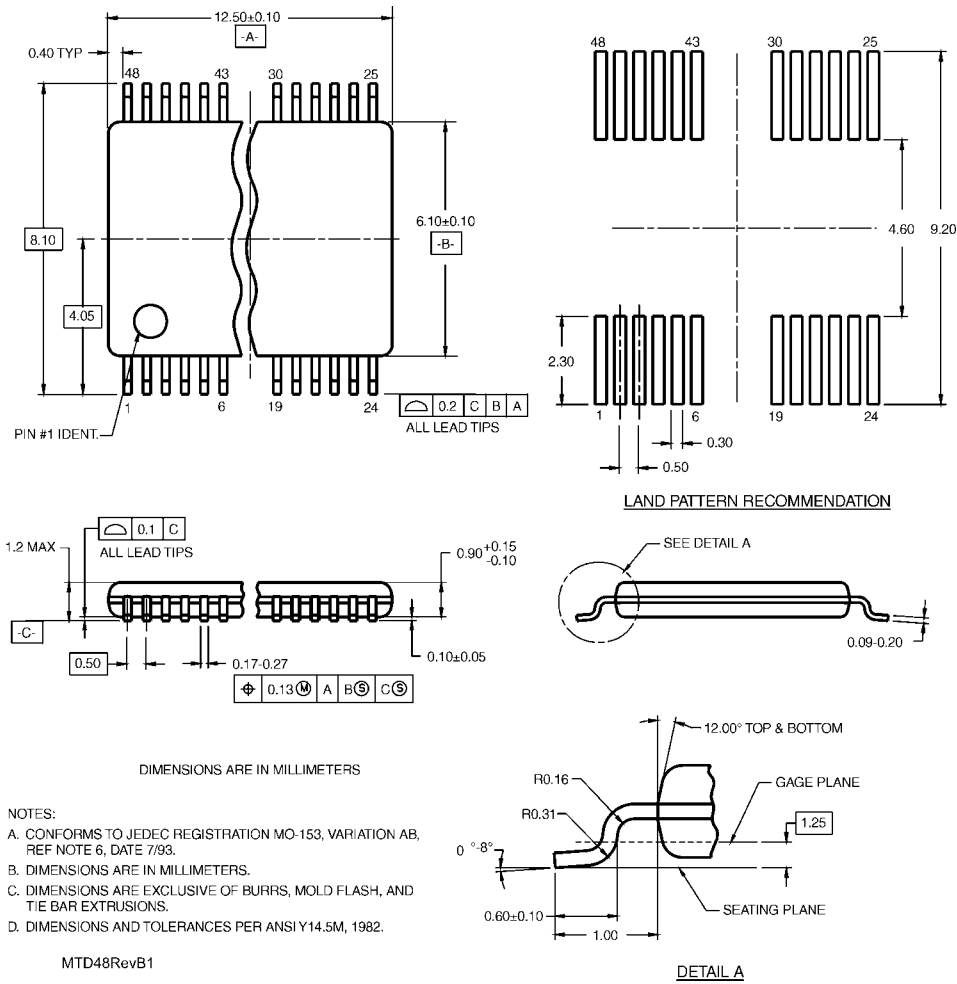**FIGURE 8. 3-STATE Output Enable and Disable Times for Low Voltage Logic**

Symbol	V$_{CC}$
	1.5V $\pm$ 0.1V
V$_{mi}$	V$_{CC}$/2
V$_{mo}$	V$_{CC}$/2
V$_X$	V$_{OL}$ + 0.1V
V$_Y$	V$_{OH}$ − 0.1V

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Physical Dimensions inches (millimeters) unless otherwise noted

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

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