Document Title

512K x8 bit Super Low Power and Low Voltage Full CMOS Static RAM

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial draft	August 30, 1999	Preliminary
1.0	Finalize - Adopt new code. - Improve V_{IN}, V_{OUT} max. on ′ABSOLUTE MAXIMUM RATINGS′ from 3.6V to V_{CC}+0.5V.	March 22, 2000	Final
2.0	Change for AC parameter - Change for tWHZ: 25 to 20ns for 70ns product - Change for tDW: 20 to 25ns for 55ns product 25 to 30ns for 70ns product	April 24, 2000	Final

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512K x 8 bit Super Low Power and Low Voltage Full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 512K x8 bit
- Power Supply Voltage: 2.7~3.3V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output status and TTL Compatible
- Package Type: 32-TSOP1-0813.4F

GENERAL DESCRIPTION

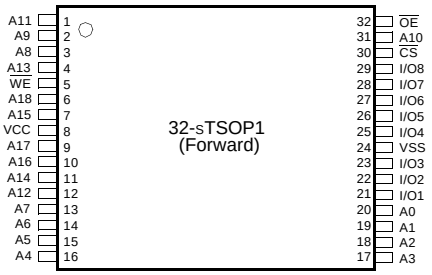
The K6F4008U1C families are fabricated by SAMSUNG′s advanced full CMOS process technology. The families support small package type for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Typ.)	Operating (I_{CC1}, Max)	
K6F4008U1C-F	Industrial(-40~85°C)	2.7~3.3V	55[1]/70ns	0.5µA	3mA	32-TSOP1-0813.4F

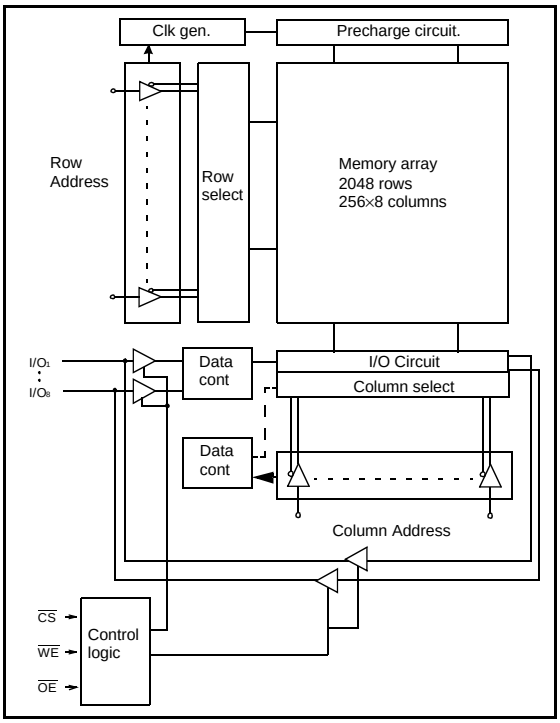
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
$\overline{OE}$	Output Enable Input	I/O_1~I/O_8	Data Inputs/Outputs
A_0~A_{18}	Address Inputs		

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	**Function**
K6F4008U1C-YF55 K6F4008U1C-YF70	32-sTSOP1-F, 55ns, 3.0V 32-sTSOP1-F, 70ns, 3.0V

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	High-Z	Output Disabled	Active
L	L	H	Dout	Read	Active
L	X[1)]	L	Din	Write	Active

1. X means don't care.(Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.5V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 4.0V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	2.7	3.0	3.3	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.6	V

Note:
1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: Vcc+2.0V in case of pulse width ≤20ns.
3. Undershoot: -2.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

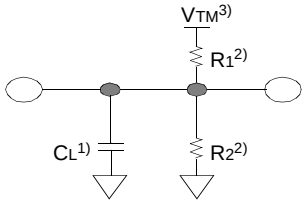
Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, $\overline{WE}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	2	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100%duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	3	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, VIN=V_{IL} or V_{IH}	-	-	30	mA
Output low voltage	V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output high voltage	V_{OH}	I_{OH} = -1.0mA	2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IL} or V_{IH}	-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other input =0~Vcc	-	0.5	12[1)]	µA

1. Super low power product=5µA with special handling.

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.1V
Output load (See right): C_L=100pF+1TTL
C_L=30pF+1TTL



1. Including scope and jig capacitance
2. R_1=3070Ω, R_2=3150Ω
3. V_{TM} =2.8V

AC CHARACTERISTICS(Vcc=2.7~3.3V, Industrial product: T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	tRC	55	-	70	-	ns
	Address Access Time	tAA	-	55	-	70	ns
	Chip Select to Output	tCO	-	55	-	70	ns
	Output Enable to Valid Output	tOE	-	25	-	35	ns
	Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
	Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
	Chip Disable to High-Z Output	tHZ	0	20	0	25	ns
	Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
	Output Hold from Address Change	tOH	10	-	10	-	ns
Write	Write Cycle Time	tWC	55	-	70	-	ns
	Chip Select to End of Write	tCW	45	-	60	-	ns
	Address Set-up Time	tAS	0	-	0	-	ns
	Address Valid to End of Write	tAW	45	-	60	-	ns
	Write Pulse Width	tWP	40	-	50	-	ns
	Write Recovery Time	tWR	0	-	0	-	ns
	Write to Output High-Z	tWHZ	0	20	0	20	ns
	Data to Write Time Overlap	tDW	25	-	30	-	ns
	Data Hold from Write Time	tDH	0	-	0	-	ns
	End Write to Output Low-Z	tOW	5	-	5	-	ns

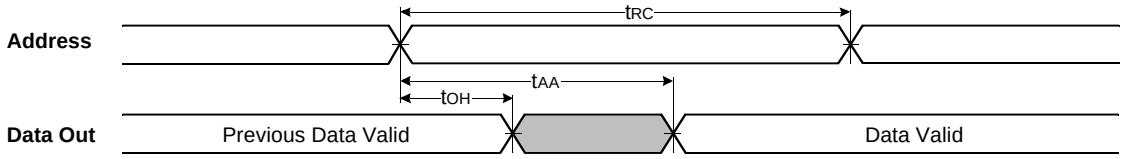
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	VDR	$\overline{CS}$≥Vcc-0.2V	1.5	-	3.3	V
Data retention current	IDR	Vcc=1.5V, $\overline{CS}$≥Vcc-0.2V	-	0.5	3[1]	µA
Data retention set-up time	tSDR	See data retention waveform	0	-	-	ns
Recovery time	tRDR		tRC	-	-	

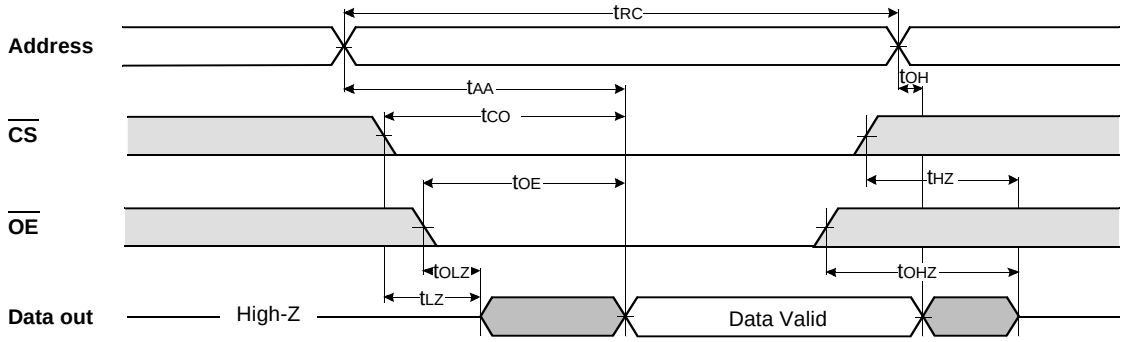
1. Super low power product=2µA with special handling.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



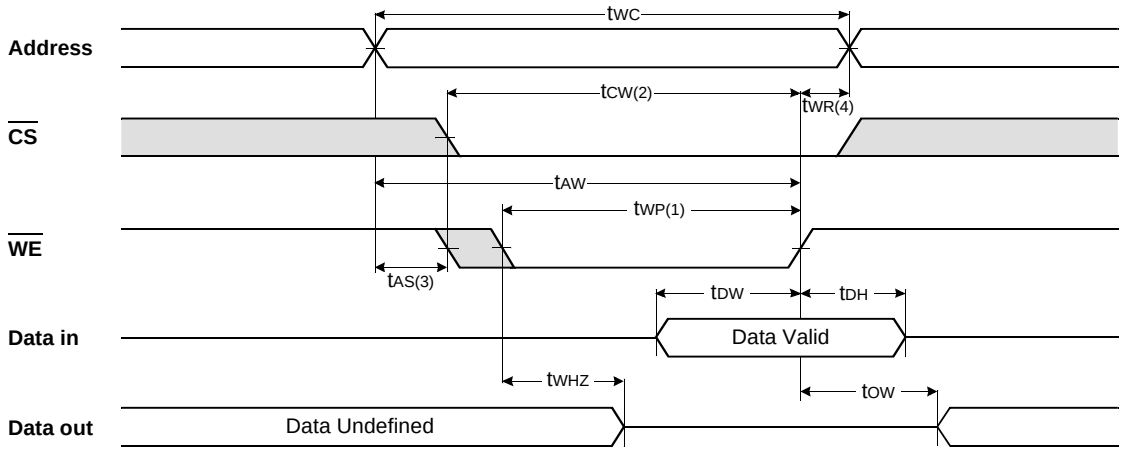
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



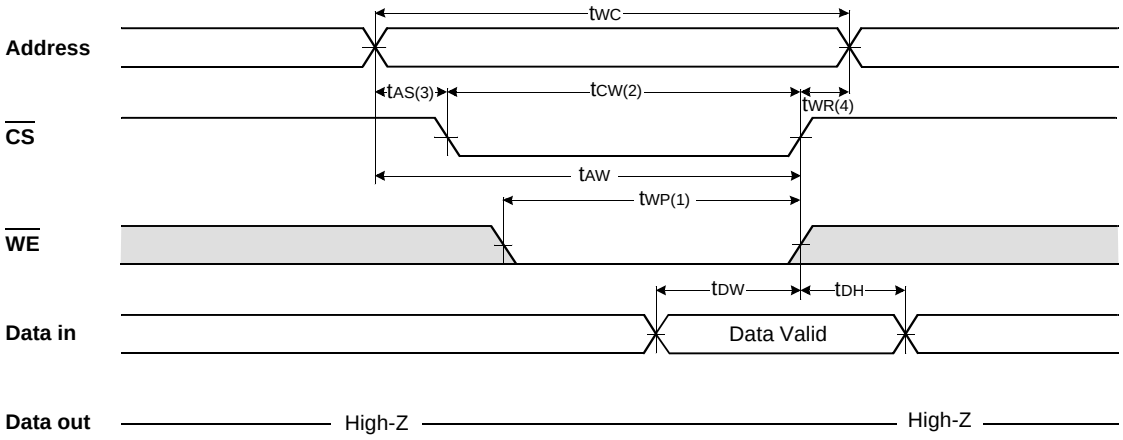
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

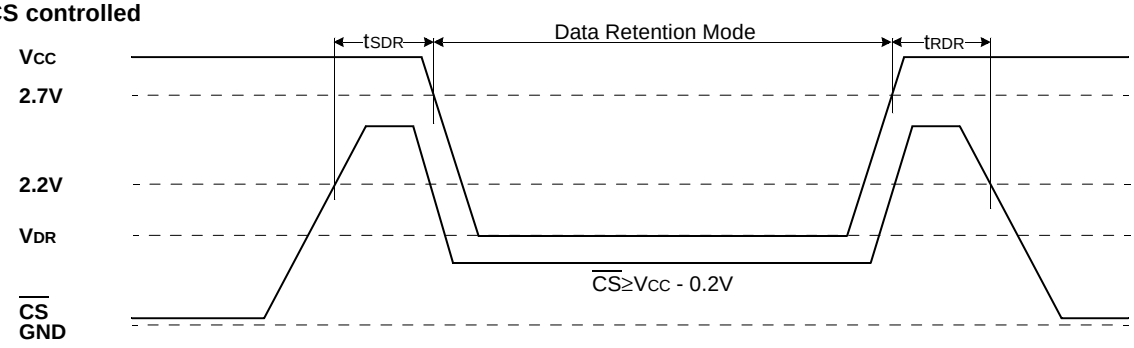


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low: A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled



32 PIN SMALLER THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)

Unit: millimeters(inches)