PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840-75

75MHz, LVCMOS/LVTTL OSCILLATOR REPLACEMENT

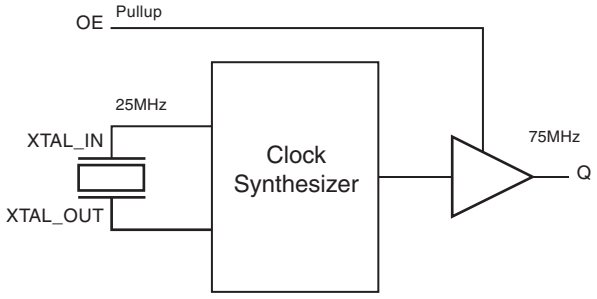
GENERAL DESCRIPTION

The ICS840-75 is a SAS/SATA Oscillator Replacement and a member of the HiPerClocks™ family of high performance devices from ICS. The ICS840-75 uses a 25MHz crystal to synthesize 75MHz. The ICS840-75 has excellent jitter performance. The ICS840-75 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

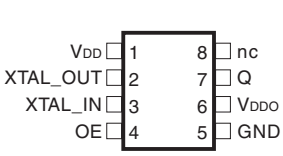
FEATURES

- One LVCMOS/LVTTL output, 15Ω output impedence
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency: 75MHz
- Random jitter: 3ps (typical)
- Deterministic jitter: 0.14ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840-75

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View

ICS840-75

8-Lead SOIC
3.90mm x 4.92mm x 1.37mm body package
M Package
Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD}	Power		Power supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	OE	Input	Pullup	Output enable pin. When HIGH, Q output is enabled. When LOW, forces Q output to HiZ state. LVCMOS/LVTTL interface levels.
5	GND	Power		Power supply ground.
6	V_{DDO}	Power		Output supply pin.
7	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels. 15Ω output impedence.
8	nc	Unused		No connect

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
R_{OUT}	Output Impedance			15		Ω

TABLE 3. CONTROL FUNCTION TABLE

Control Inputs	Output
OE	**Q**
0	Hi-Z
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	
8 Lead TSSOP	101.7°C/W (0 mps)
8 Lead SOIC	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±0.3V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	OE = V_{DD} (output enabled)		80		mA
I_{DDO}	Output Supply Current			8		mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 3.3V±0.3V, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.6V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

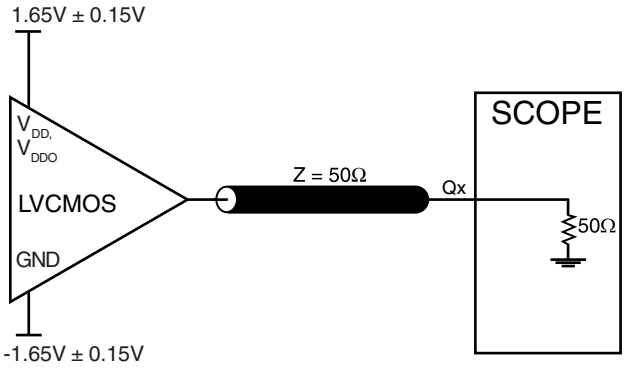
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)			TBD		Ω
Shunt Capacitance				7	pF
Drive Level				TBD	µW

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$,, $T_A = 0°C$ TO $70°C$

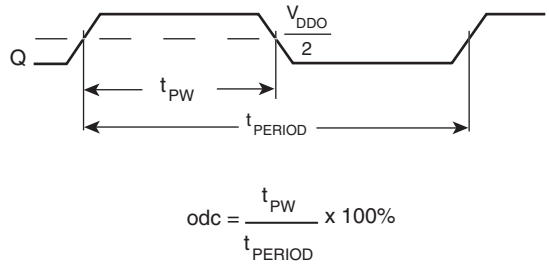
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			75		MHz
t_{DJ}	Deterministic Jitter; NOTE 1			0.14		ps
t_{RJ}	Random Jitter; NOTE 1			3		ps
t_{RMS}	RMS of Total Distribution (σ); NOTE 1			3.05		ps
t_{p-p}	Peak-to-Peak Jitter; NOTE 1			2.7		ps
t_{acc}	Accumulated Jitter (σ); NOTE 1	n = 2 to 50000 cycles		TBD		ps
t_{OSC}	Oscillation Start Up Time	Time at minimum operating voltage to be 0 s			10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		TBD		ps
odc	Output Duty Cycle			50		%

NOTE 1: Measured using Wavecrest SIA-3000.

PARAMETER MEASUREMENT INFORMATION

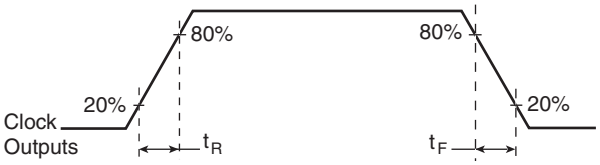


3.3V OUTPUT LOAD AC TEST CIRCUIT



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The ICS840-75 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

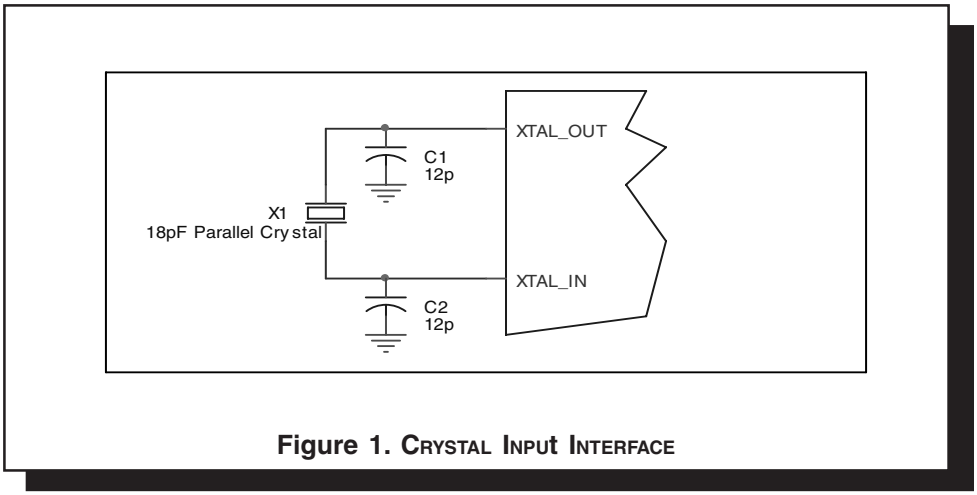


Figure 1. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 7B. θ_{JA} VS. AIR FLOW TABLE 8 LEAD SOIC

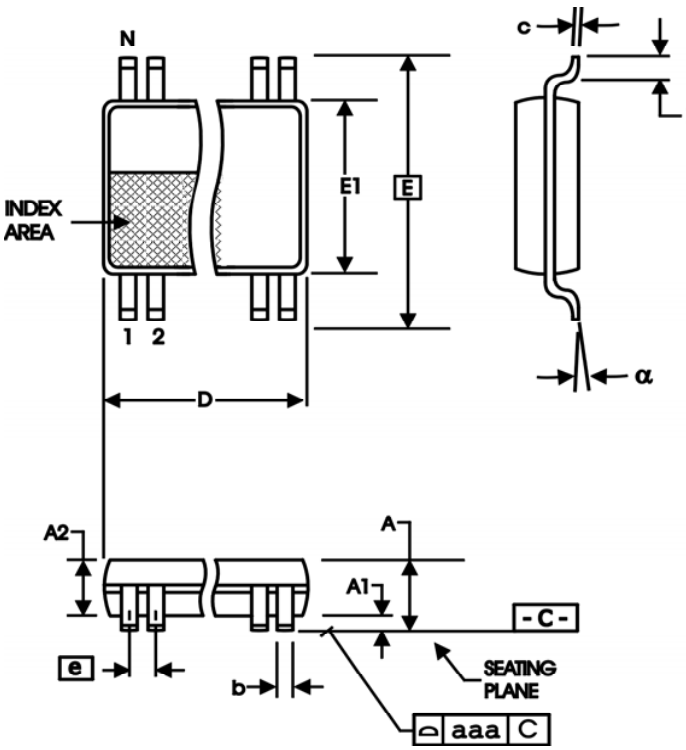
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840-75 is: 2423

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

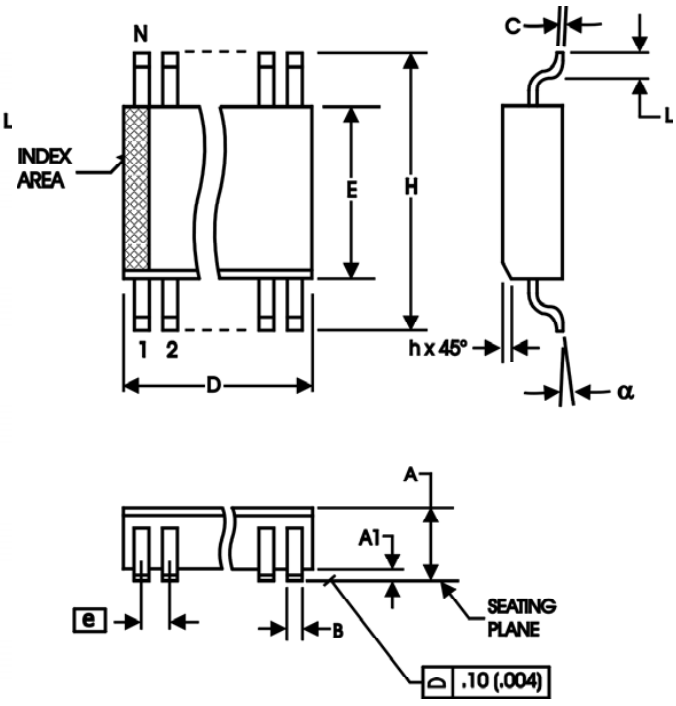


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840AG-75	40A75	8 lead TSSOP	tube	0°C to 70°C
ICS840AG-75T	40A75	8 lead TSSOP	2500 tape & reel	0°C to 70°C
ICS840AG-75LF	0A75L	8 lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS840AG-75LFT	0A75L	8 lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C
ICS840AM-75	TBD	8 lead SOIC	tube	0°C to 70°C
ICS840AM-75T	TBD	8 lead SOIC	2500 tape & reel	0°C to 70°C
ICS840AM-75LF	TBD	8 lead "Lead-Free" SOIC	tube	0°C to 70°C
ICS840AM-75LFT	TBD	8 lead "Lead-Free" SOIC	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.