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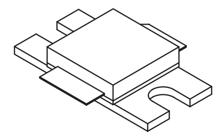
The RF MOSFET Line
RF Power Field Effect Transistors
N–Channel Enhancement–Mode Lateral MOSFETs

MRF21045R3
MRF21045SR3

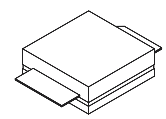
Designed for W–CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN–PCS/cellular radio and WLL applications.

- Typical 2–carrier W–CDMA Performance for V_{DD} = 28 Volts, I_{DQ} = 500 mA, f1 = 2135 MHz, f2 = 2145 MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels measured over 3.84 MHz Bandwidth at f1 –5 MHz and f2 +5 MHz, Distortion Products measured over a 3.84 MHz Bandwidth at f1 –10 MHz and f2 +10 MHz, Peak/Avg. = 8.3 dB @ 0.01% Probability on CCDF.
  Output Power — 10 Watts Avg.
  Efficiency — 23.5%
  Gain — 15 dB
  IM3 — –37.5 dBc
  ACPR — –41 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, 2170 MHz, 45 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large–Signal Impedance Parameters
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

**2170 MHz, 45 W, 28 V
LATERAL N–CHANNEL
RF POWER MOSFETs**



**CASE 465E–03, STYLE 1
NI–400
MRF21045R3**



**CASE 465F–03, STYLE 1
NI–400S
MRF21045SR3**

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	65	Vdc
Gate–Source Voltage	V_{GS}	–0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	105 0.60	Watts W/°C
Storage Temperature Range	T_{stg}	–65 to +200	°C
Operating Junction Temperature	T_J	200	°C

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M2 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.65	°C/W

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

REV 5

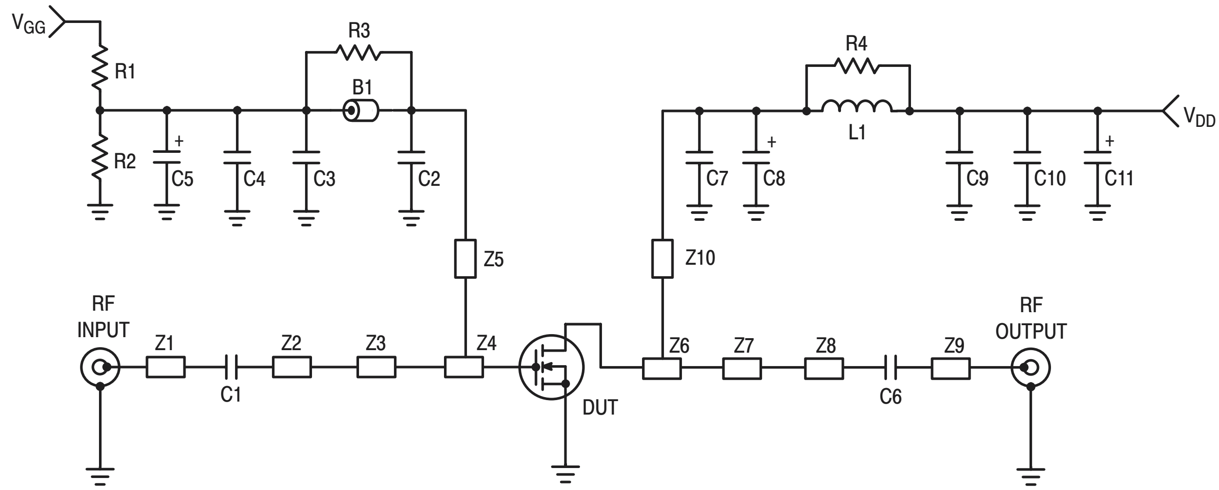
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 100 μAdc)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS (DC)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	—	4	Vdc
Gate Quiescent Voltage (V_{DS} = 28 Vdc, I_D = 500 mAdc)	$V_{GS(Q)}$	3	3.9	5	Vdc
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1 Adc)	$V_{DS(on)}$	—	0.19	0.21	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1 Adc)	g_{fs}	—	3	—	S
DYNAMIC CHARACTERISTICS (1)					
Reverse Transfer Capacitance (V_{DS} = 28 Vdc, V_{GS} = 0, f = 1 MHz)	C_{rss}	—	1.8	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA. Peak/Avg. ratio = 8.3 dB @ 0.01% Probability on CCDF.					
Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	G_{ps}	13.5	15	—	dB
Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	η	21	23.5	—	%
Third Order Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; IM3 measured over 3.84 MHz Bandwidth at f1 –10 MHz and f2 +10 MHz.)	IM3	—	–37.5	–35	dBc
Adjacent Channel Power Ratio (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz; ACPR measured over 3.84 MHz Bandwidth at f1 –5 MHz and f2 +5 MHz.)	ACPR	—	–41	–38	dBc
Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 10 W Avg., I_{DQ} = 500 mA, f1 = 2112.5 MHz, f2 = 2122.5 MHz and f1 = 2157.5 MHz, f2 = 2167.5 MHz)	IRL	—	–12	–9	dB
Output Mismatch Stress (V_{DD} = 28 Vdc, P_{out} = 45 W CW, I_{DQ} = 500 mA, f = 2170 MHz VSWR = 5:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) Part is internally matched both on input and output.

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) — continued					
Two–Tone Common–Source Amplifier Power Gain (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	G_{ps}	—	14.9	—	dB
Two–Tone Drain Efficiency (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	η	—	36	—	%
Intermodulation Distortion (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IMD	—	–30	—	dBc
Two–Tone Input Return Loss (V_{DD} = 28 Vdc, P_{out} = 45 W PEP, I_{DQ} = 500 mA, f1 = 2110 MHz, f2 = 2120 MHz and f1 = 2160 MHz, f2 = 2170 MHz)	IRL	—	–12	—	dB
P_{out}, 1 dB Compression Point (V_{DD} = 28 Vdc, I_{DQ} = 500 mA, f = 2170 MHz)	P1dB	—	50	—	W



Z1, Z9	0.750″ x 0.084″ Transmission Line	Board	0.030″ Glass Teflon®, Keene GX–0300–55–22, ε_r = 2.55
Z2	0.160″ x 0.084″ Transmission Line	PCB	Etched Circuit Boards MRF21045 Rev. 3, CMR
Z3	1.195″ x 0.176″ Transmission Line		
Z4	0.125″ x 0.320″ Transmission Line		
Z5	1.100″ x 0.045″ Transmission Line		
Z6	0.442″ x 0.650″ Transmission Line		
Z7	0.490″ x 0.140″ Transmission Line		
Z8	0.540″ x 0.084″ Transmission Line		
Z10	0.825″ x 0.055″ Transmission Line		

Figure 1. MRF21045 Test Circuit Schematic

Table 1. MRF21045 Component Designations and Values

Designators	Description
B1	Short Ferrite Bead, Fair Rite, #2743019447
C1, C2, C6	43 pF Chip Capacitors, ATC #100B430JCA500X
C7	5.6 pF Chip Capacitor, ATC #100B5R6JCA500X
C3, C9	1000 pF Chip Capacitors, ATC #100B102JCA500X
C4, C10	0.1 μF Chip Capacitors, Kemet #CDR33BX104AKWS
C5	1.0 μF Tantalum Chip Capacitor, Kemet #T491C105M050
C8	10 μF Tantalum Chip Capacitor, Kemet #T495X106K035AS4394
C11	22 μF Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
L1	1 Turn, #20 AWG, 0.100″ ID, Motorola
N1, N2	Type N Flange Mounts, Omni Spectra #3052–1648–10
R1	1.0 kΩ, 1/8 W Chip Resistor
R2	180 kΩ, 1/8 W Chip Resistor
R3, R4	10 Ω, 1/8 W Chip Resistors

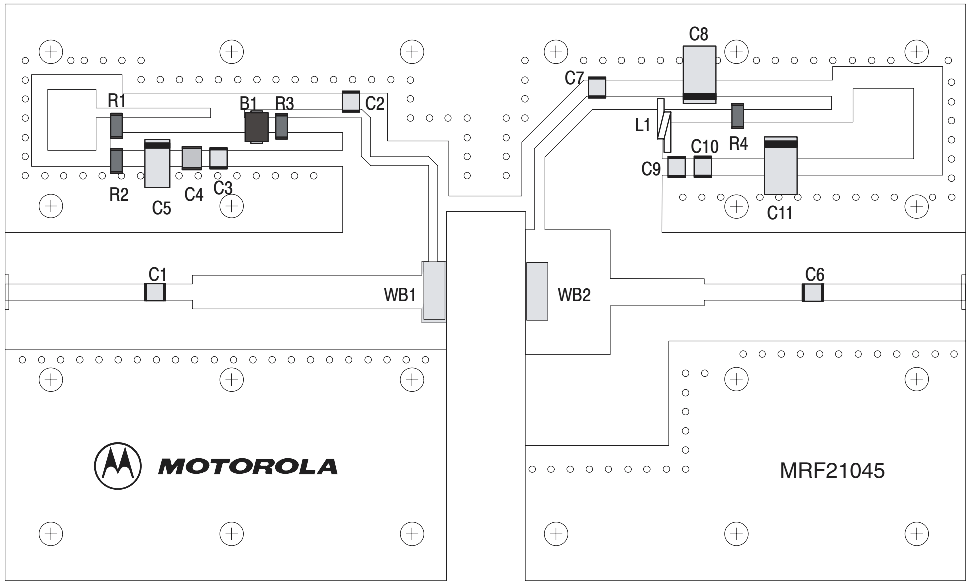


Figure 2. MRF21045 Test Circuit Component Layout

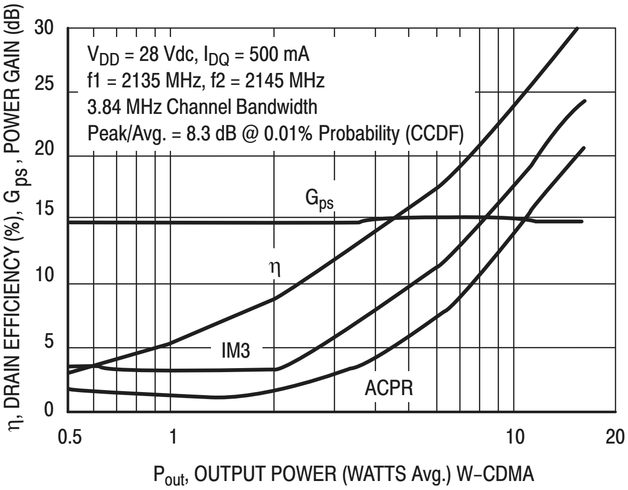


Figure 3. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

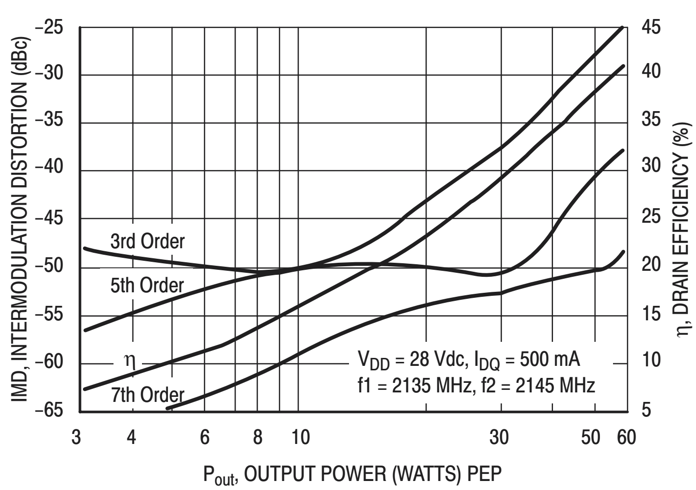


Figure 4. Intermodulation Distortion Products versus Output Power

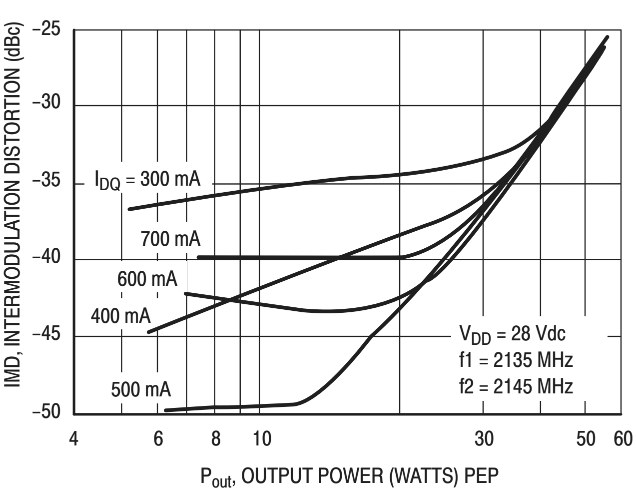


Figure 5. Intermodulation Distortion versus Output Power

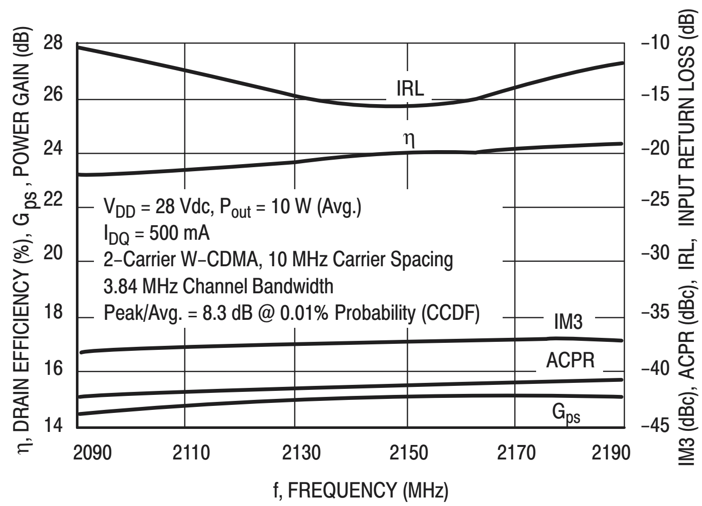


Figure 6. 2–Carrier W–CDMA Broadband Performance

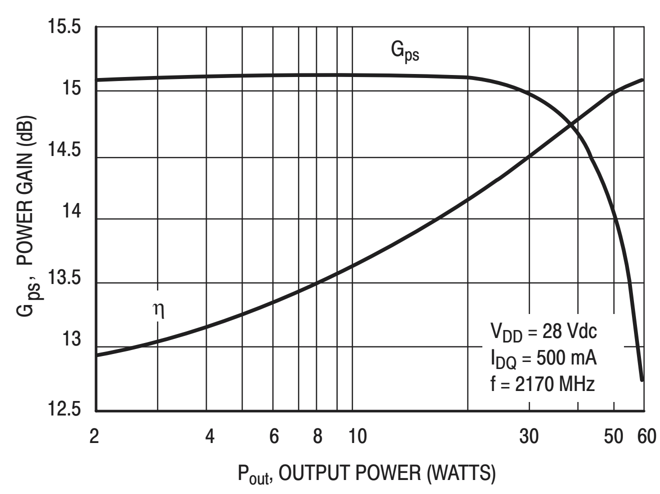


Figure 7. CW Performance

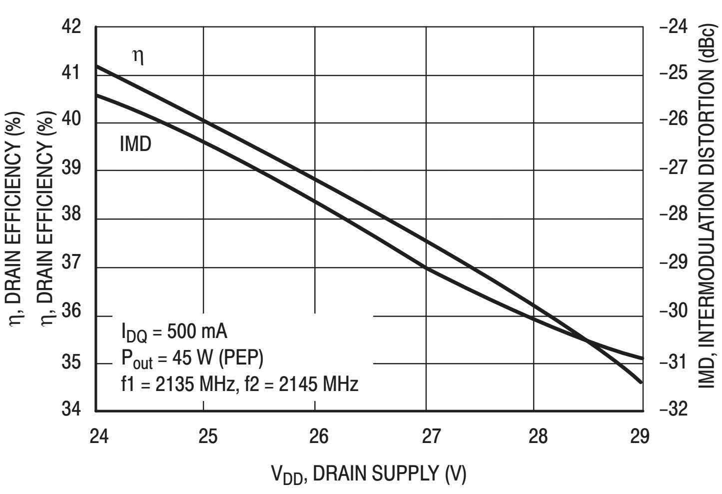


Figure 8. Two–Tone Intermodulation Distortion and Drain Efficiency versus Drain Supply

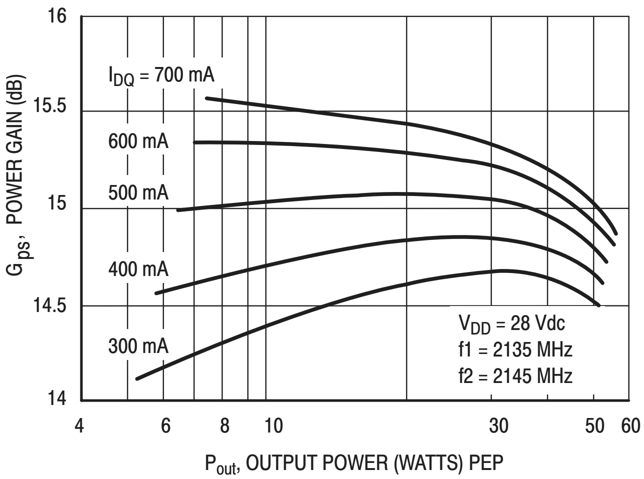


Figure 9. Two-Tone Power Gain versus Output Power

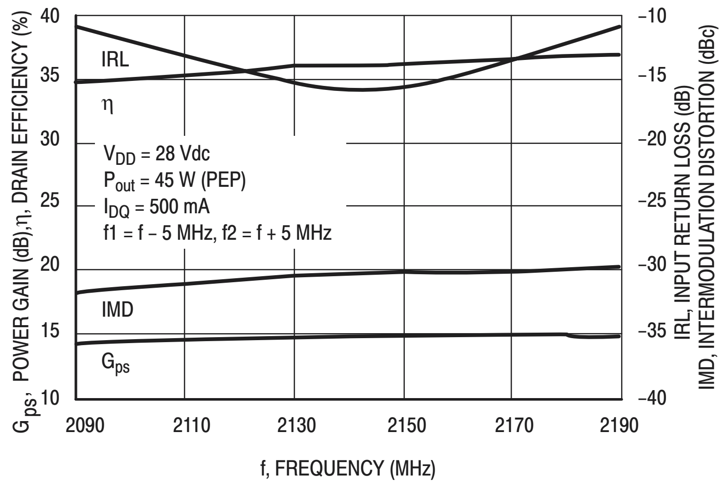


Figure 10. Two-Tone Broadband Performance

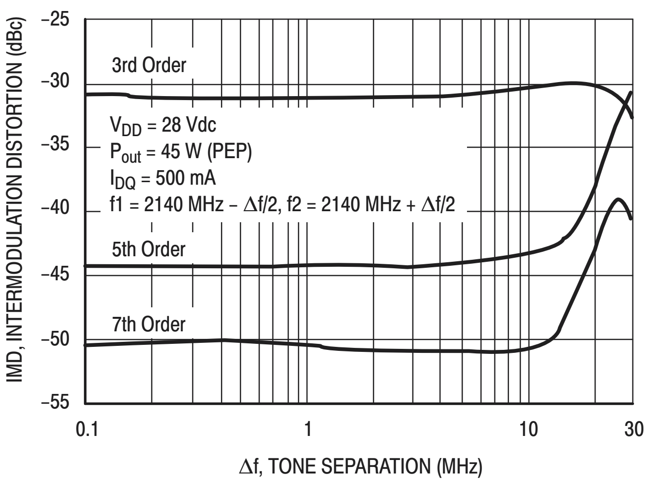


Figure 11. Intermodulation Distortion Products versus Two–Tone Spacing

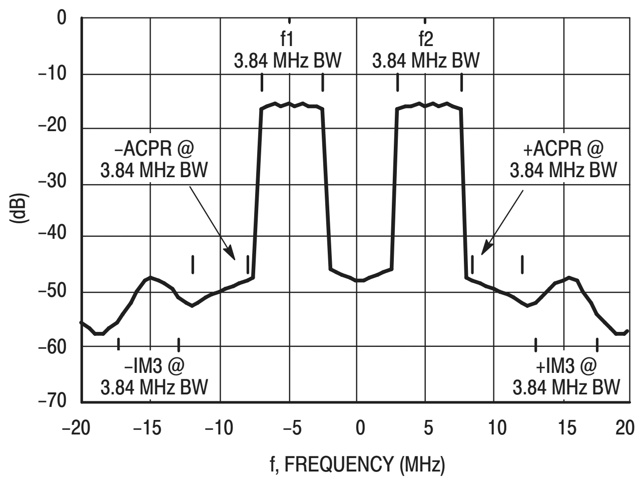
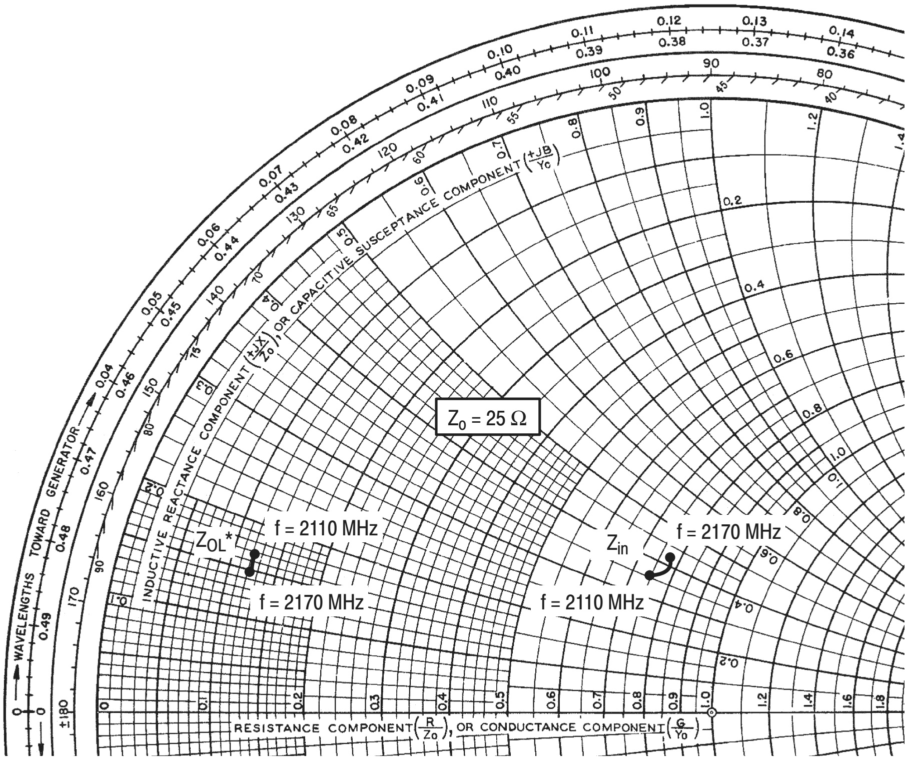


Figure 12. 2-Carrier W-CDMA Spectrum



V_{DD} = 28 Vdc, I_{DQ} = 500 mA, P_{out} = 10 W Avg.

f MHz	Z_{in} Ω	Z_{OL}* Ω
2110	18.88 + j8.86	3.11 + j4.18
2140	19.80 + j9.93	3.09 + j3.87
2170	19.68 + j10.44	3.12 + j3.72

Z_{in} = Complex conjugate of source impedance.

Z_{OL}* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

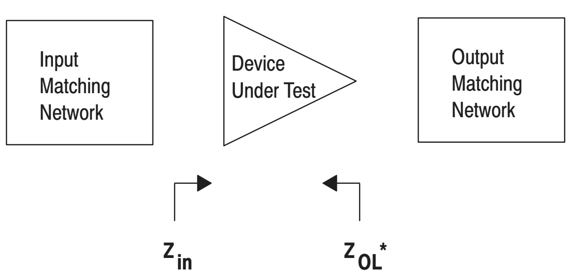
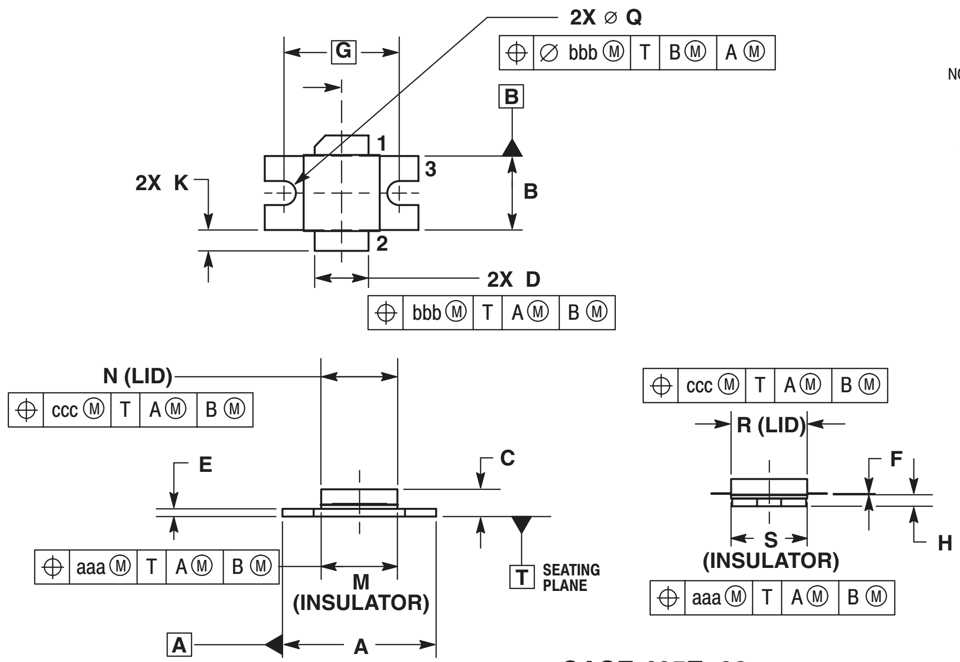


Figure 13. Series Equivalent Input and Output Impedance

NOTES

NOTES

PACKAGE DIMENSIONS

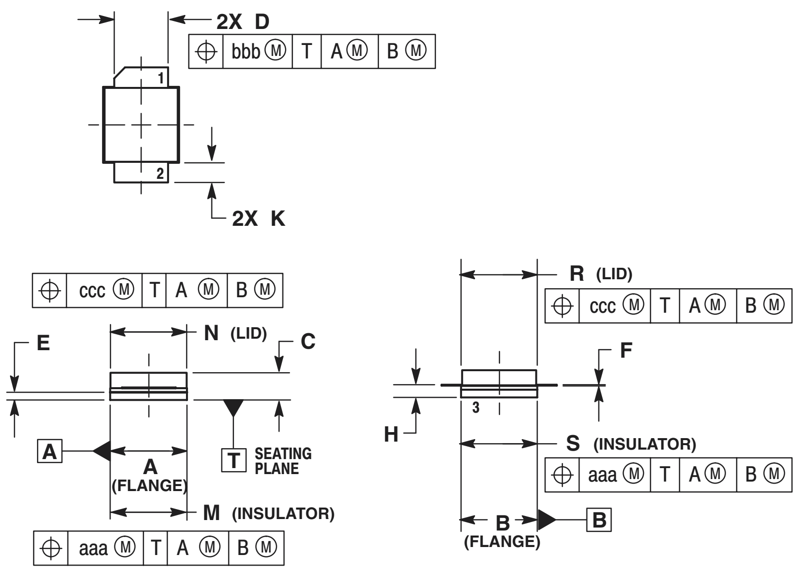


NOTES:
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.07	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	∅ .110	∅ .130	∅ 2.79	∅ 3.3
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465E–03
ISSUE D
NI–400
MRF21045R3



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	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.003	.006	0.08	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 465F–03
ISSUE B
NI–400S
MRF21045SR3

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