TJA1029

LIN 2.2A/SAE J2602 transceiver with TXD dominant timeout

Rev. 1 — 8 January 2013 Product data sheet

1. General description

The TJA1029 is the interface between the Local Interconnect Network (LIN) master/slave protocol controller and the physical bus in a LIN network. It is primarily intended for in-vehicle subnetworks using baud rates up to 20 kBd and is compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602. The TJA1029 is pin-compatible with the TJA1020, TJA1021, TJA1022 and TJA1027.

The protocol controller generates the transmit data stream. The TJA1029 converts the data stream into an optimized bus signal shaped to minimize ElectroMagnetic Emissions (EME). The LIN bus output pin is pulled HIGH via an internal termination resistor. For a master application, connect an external resistor in series with a diode between pin V_{BAT} and pin LIN. The receiver detects a receive data stream on the LIN bus input pin and transfers it via pin RXD to the microcontroller.

Power consumption is very low in Sleep mode. However, the TJA1029 can still be woken up via pins LIN and SLP_N. An integrated TXD dominant time-out function prevents the bus being driven to a permanent dominant state.

2. Features and benefits

2.1 General

- Compliant with LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602
- Baud rate up to 20 kBd
- Very low ElectroMagnetic Emissions (EME)
- Very low current consumption in Sleep mode with remote LIN wake-up
- Input levels compatible with 3.3 V and 5 V devices
- Integrated termination resistor for LIN slave applications
- Passive behavior in unpowered state
- Operational during cranking pulse: full operation from 5 V upwards
- Undervoltage detection
- K-line compatible
- Available in SO8 and HVSON8 packages
- Leadless HVSON8 package (3.0 mm × 3.0 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- Pin-compatible subset of the TJA1020, TJA1021 and TJA1022
- Pin-compatible with the TJA1027

2.2 Protection

- Very high ElectroMagnetic Immunity (EMI)
- Very high ESD robustness: ±8 kV according to IEC 61000-4-2 for pins LIN and V_{BAT}
- Bus terminal and battery pin protected against transients in the automotive environment (ISO 7637)
- Bus terminal short-circuit proof to battery and ground
- Thermally protected
- Initial TXD dominant check when switching to Normal mode
- TXD dominant time-out function

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	limiting values	–0.3	-	+42	V
		operating range	5	-	18	V
I_{BAT}	battery supply current	Sleep mode; $V_{LIN} = V_{BAT}$; $V_{SLP\_N} = 0$ V	2.5	7	10	µA
		Standby mode; $V_{LIN} = V_{BAT}$; $V_{SLP\_N} = 0$ V	2.5	7	10	µA
		Normal mode; $V_{LIN} = V_{BAT}$; $V_{SLP\_N} = 5$ V; $V_{TXD} = 5$ V	200	800	1600	µA
V_{LIN}	voltage on pin LIN	limiting value; with respect to GND and V_{BAT}	–42	-	+42	V
V_{ESD}	electrostatic discharge voltage	on pin LIN; according to IEC 61000-4-2	–8	-	+8	kV
T_{vj}	virtual junction temperature		–40	-	+150	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TJA1029T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TJA1029TK	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT782-1

5. Block diagram

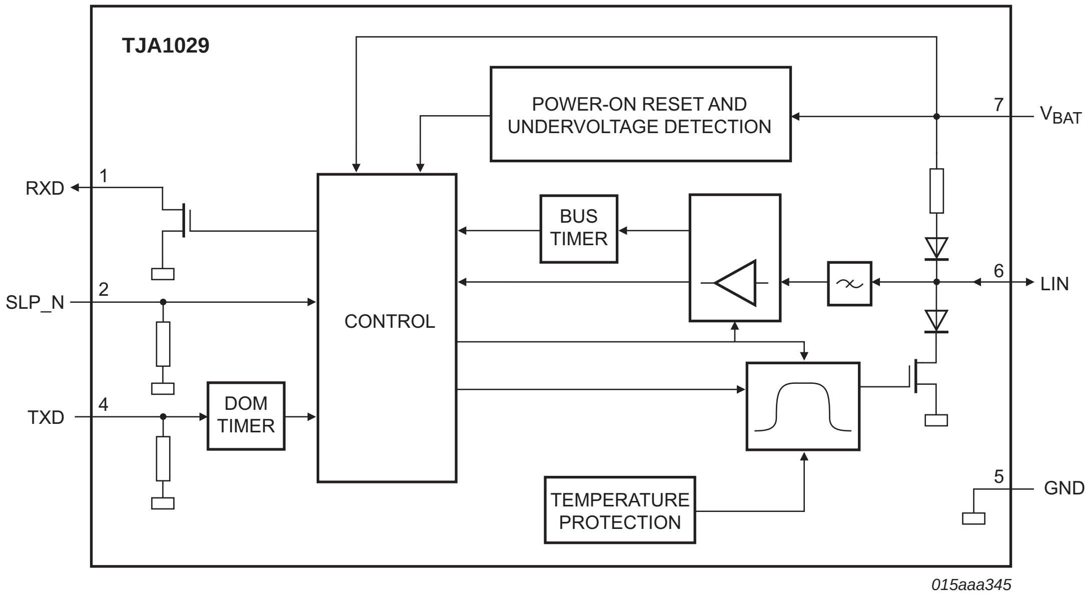
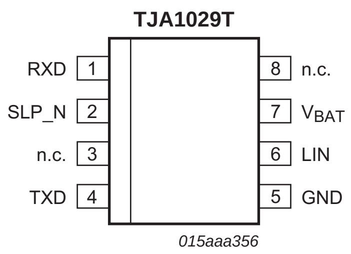


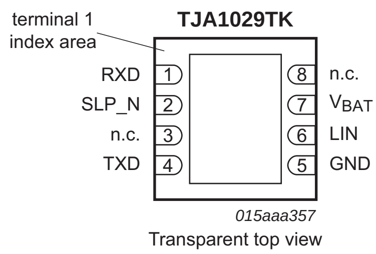
Fig 1. Block diagram

6. Pinning information

6.1 Pinning



a. TJA1029T: SO8 package



b. TJA1029TK: HVSON8 package

Fig 2. Pin configuration diagrams

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
RXD	1	receive data output (open-drain); active LOW after a wake-up event
SLP_N	2	sleep control input (active LOW); resets wake-up request on RXD
n.c.	3	not connected
TXD	4	transmit data input
GND	5[1]	ground
LIN	6	LIN bus line input/output
V_{BAT}	7	battery supply
n.c.	8	not connected

[1] For enhanced thermal and electrical performance, solder the exposed center pad of the HVSON8 package to board ground and not to any other voltage level.

7. Functional description

The TJA1029 is the interface between the LIN master/slave protocol controller and the physical bus in a LIN network. According to the Open System Interconnect (OSI) model, this interface makes up the LIN physical layer.

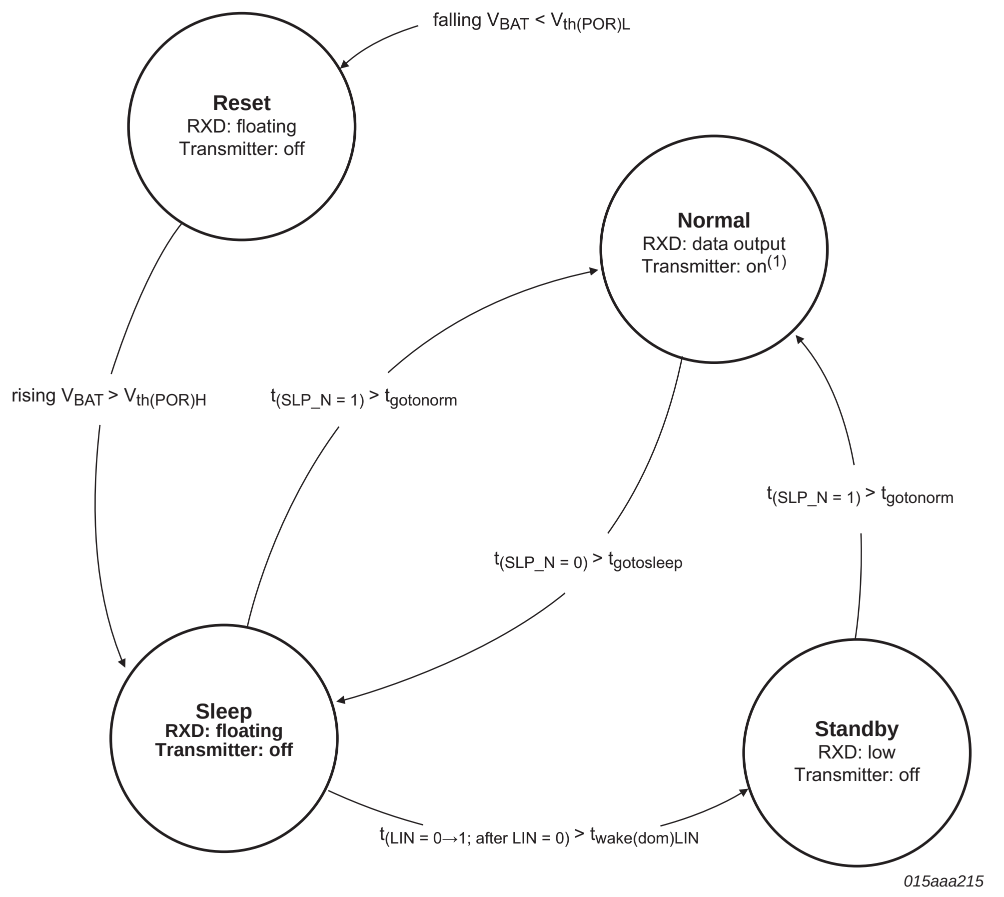
The LIN transceiver is optimized for, but not limited to, automotive applications with excellent ElectroMagnetic Compatibility (EMC) performance.

7.1 LIN 2.x/SAE J2602 compliant

The TJA1029 is fully LIN 2.0, LIN 2.1, LIN 2.2, LIN 2.2A and SAE J2602 compliant. The LIN physical layer is independent of higher OSI model layers (e.g. the LIN protocol). Consequently, nodes containing a LIN 2.2A-compliant physical layer can be combined, without restriction, with LIN physical layer nodes that comply with earlier revisions (LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3, LIN 2.0, LIN 2.1 and LIN 2.2).

7.2 Operating modes

The TJA1029 supports modes for normal operation (Normal mode) and very-low-power operation (Sleep mode). An intermediate wake-up mode between Sleep and Normal modes is also supported (Standby mode). The state diagram is shown in Figure 3.



(1) A positive edge on SLP_N triggers a transition to Normal mode. The transmitter is enabled when TXD goes HIGH. In the event of thermal shutdown, the transmitter is disabled.

Fig 3. State diagram

Table 4. Operating modes

Mode	SLP_N	RXD	Transmitter	Description
Reset	x	floating	off	all inputs ignored; all outputs drivers off
Sleep[1]	0	floating	off	no wake-up request detected
Standby[2]	0	LOW[3]	off	wake-up request detected
Normal	1	HIGH: recessive state LOW: dominant state	Normal mode[4]	bus signal shaping enabled

[1] The TJA1029 enters Sleep mode after a power-on reset (e.g. after switching on V_{BAT}).

[2] The TJA1029 switches automatically to Standby mode when a LIN wake-up event occurs in Sleep mode.

[3] The wake-up interrupt (on pin RXD) is released after a positive edge on pin SLP_N.

[4] A positive edge on SLP_N triggers a transition to Normal mode. The transmitter will be off if TXD is LOW and will be enabled as soon as TXD goes HIGH.

7.2.1 Reset mode

When the TJA1029 is in Reset mode, it ignores all input signals and all output drivers are off. The TJA1029 switches to Reset mode when the voltage on V_{BAT} drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$. When the voltage on V_{BAT} rises above the HIGH-level power-on reset threshold, $V_{th(POR)H}$, the TJA1029 switches to Sleep mode.

7.2.2 Sleep mode

The TJA1029 consumes significantly less power in Sleep mode than in Normal mode. Even though current consumption is extremely low in Sleep mode, the TJA1029 can still be woken up remotely via pin LIN or activated directly via pin SLP_N. Filters on the receiver input (LIN) and on pin SLP_N prevent unwanted wake-up events occurring due to automotive transients or radio frequency interference. All wake-up events must be maintained for a specific period ($t_{wake(dom)LIN}$ or $t_{gotonorm}$).

A falling edge on pin SLP_N in Normal mode initiates a transition to Sleep mode. The LIN transmit path is immediately disabled when pin SLP_N goes LOW. In order to ensure the TJA1029 switches successfully to Sleep mode, the sleep command (pin SLP_N = LOW) must be maintained for at least $t_{gotosleep}$.

Sleep mode activation is independent of the levels on pins LIN or TXD. So the lowest possible power consumption can be guaranteed, even when there is a continuous dominant level on pins LIN and TXD.

7.2.3 Standby mode

Standby mode is activated automatically when a local or remote wake-up event occurs while the TJA1029 is in Sleep mode. In Standby mode, pin RXD is held LOW to provide an interrupt flag for the microcontroller.

7.2.4 Normal mode

In Normal mode, the TJA1029 can transmit and receive data via the LIN bus.

The receiver detects the data stream on the LIN bus input pin and transfers it via pin RXD to the microcontroller (see Figure 6): HIGH for a recessive level and LOW for a dominant level on the bus. The receiver has a supply-voltage related threshold with hysteresis and an integrated filter to suppress bus line noise.

The transmitter converts the transmit data stream from the protocol controller, detected on pin TXD, into an optimized bus signal. The optimized bus signal is shaped to minimize EME. The LIN bus output pin is pulled HIGH via an internal slave termination resistor. For a master application, connect an external resistor in series with a diode between pin V_{BAT} and pin LIN (see Figure 6).

If pin SLP_N is pulled HIGH while the TJA1029 is in Sleep or Standby mode, the LIN transceiver switches to Normal mode after $t_{gotonorm}$.

7.3 Transceiver wake-up

7.3.1 Remote wake-up via the LIN bus

A falling edge on pin LIN, followed by a LOW level maintained for $t_{wake(dom)LIN}$, followed by a rising edge on pin LIN, triggers a remote wake-up (see Figure 4). Note that the time period $t_{wake(dom)LIN}$ is measured either in Normal mode while TXD is HIGH, or in Sleep mode irrespective of the status of pin TXD.

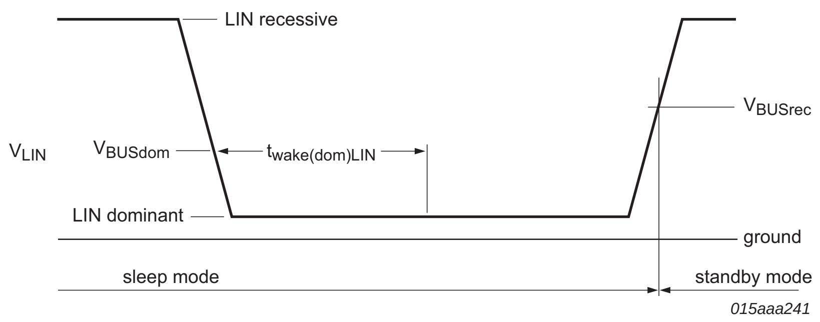


Fig 4. Remote wake-up behavior

7.3.2 Wake-up via pin SLP_N

If SLP_N is held HIGH for $t_{gotonorm}$, the TJA1029 switches from Sleep mode to Normal mode.

7.4 Operation during automotive cranking pulses

TJA1029 remains fully operational during automotive cranking pulses because the LIN transceiver is fully specified down to V_{BAT} = 5 V.

7.5 Operation when supply voltage is outside specified operating range

If V_{BAT} > 18 V or V_{BAT} < 5 V, the TJA1029 may remain operational, but parameter values cannot be guaranteed to remain within the operating ranges specified in Table 7 and Table 8.

If the voltage on pin V_{BAT} drops below the LOW-level power-on reset threshold, $V_{th(POR)L}$, the TJA1029 switches to Reset mode. All output drivers are disabled and all inputs are ignored. The TJA1029 switches to Sleep mode if $V_{BAT} > V_{th(POR)H}$.

In Normal mode:

- If the input level on pin TXD is HIGH, the LIN transmitter output on pin LIN will be recessive.
- If the input level on pin LIN is recessive, the receiver output on pin RXD will be HIGH.
- If the voltage on pin V_{BAT} rises to 27 V (e.g. during an automotive jump-start), the total LIN network pull-up resistance should be greater than 680 Ω and the total LIN network capacitance should be less than 6.8 nF to ensure reliable LIN data transfer.

- If the voltage on pin V_{BAT} drops below the LOW-level V_{BAT} LOW threshold, $V_{th(VBATL)L}$, the LIN transmit path is interrupted and the LIN output remains recessive. The LIN transmit path is switched on again when V_{BAT} rises above $V_{th(VBATL)H}$ and the input to pin TXD is recessive.

7.6 TXD dominant time-out function

An initial TXD dominant check prevents the bus line being driven to a permanent dominant state (blocking all network communications) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The TXD input level is checked after a transition to Normal mode. If TXD is LOW, the transmit path remains disabled and is only enabled when TXD goes HIGH.

Once the transmitter has been enabled, a TXD dominant time-out timer is started every time pin TXD goes LOW. If the LOW state on pin TXD persists for longer than the TXD dominant time-out time ($t_{to(dom)TXD}$), the transmitter is disabled, releasing the bus line to recessive state. The TXD dominant time-out timer is reset when pin TXD goes HIGH.

7.7 Fail-safe features

A pull-down to GND on pin TXD forces a predefined level on the transmit data input if the pin is disconnected.

A pull-down to GND on pin SLP_N forces the transceiver into Sleep mode if pin SLP_N is disconnected.

Pin RXD is set floating if V_{BAT} is disconnected.

The current in the transmitter output stage is limited in order to protect the transmitter against short circuits to pins V_{BAT} or GND.

A loss of power (pins V_{BAT} and GND) has no impact on the bus line or on the microcontroller. No reverse currents flow from the bus into pin LIN. The current path from V_{BAT} to LIN via the integrated LIN slave termination resistor remains. The LIN transceiver can be disconnected from the power supply without influencing the LIN bus.

The output driver on pin LIN is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the thermal protection circuit disables the output driver. The driver is enabled again when the junction temperature falls below $T_{j(sd)}$ and pin TXD is recessive.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to pin GND, unless otherwise specified. Positive currents flow into the IC.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{BAT}	battery supply voltage			–0.3	+42	V
V_{TXD}	voltage on pin TXD			–0.3	+7	V
V_{RXD}	voltage on pin RXD			–0.3	+7	V
V_{SLP_N}	voltage on pin SLP_N			–0.3	+7	V
V_{LIN}	voltage on pin LIN	with respect to GND and V_{BAT}		–42	+42	V
V_{ESD}	electrostatic discharge voltage					
	according to IEC 61000-4-2	on pins LIN and V_{BAT}	[1]	–8	+8	kV
	human body model	on pins LIN and V_{BAT}	[2]	–8	+8	kV
		on pins TXD, RXD and SLP_N	[2]	–2	+2	kV
	charge device model	all pins		–750	+750	V
	machine model	all pins	[3]	–200	+200	V
T_{vj}	virtual junction temperature		[4]	–40	+150	°C
T_{stg}	storage temperature			–55	+150	°C

[1] Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.

[3] Equivalent to discharging a 200 pF capacitor through a 10 Ω resistor and a 0.75 μH coil.

[4] Junction temperature in accordance with IEC 60747-1. An alternative definition is: $T_j = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).

9. Thermal characteristics

Table 6. Thermal characteristics

According to IEC 60747-1.

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	SO8 package; in free air	145	K/W
		HVSON8 package; in free air	50	K/W

10. Static characteristics

Table 7. Static characteristics

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{BAT}	battery supply voltage			5	-	18	V
I_{BAT}	battery supply current	Sleep mode; bus recessive; $V_{LIN} = V_{BAT}$; V_{SLP_N} = 0 V		2.5	7	10	μA
		Sleep mode; bus dominant; V_{LIN} = 0 V; V_{BAT} = 12 V; V_{SLP_N} = 0 V		150	400	1200	μA
		Standby mode; bus recessive; $V_{LIN} = V_{BAT}$; V_{SLP_N} = 0 V		2.5	7	10	μA
		Standby mode; bus dominant; V_{LIN} = 0 V; V_{BAT} = 12 V; V_{SLP_N} = 0 V	[2]	100	300	1000	μA
		Normal mode; bus recessive; $V_{LIN} = V_{BAT}$; V_{SLP_N} = 5 V; V_{TXD} = 5 V		200	800	1600	μA
		Normal mode; bus dominant; V_{TXD} = 0 V; V_{SLP_N} = 5 V; V_{BAT} = 12 V		1	2	4	mA
Undervoltage reset							
$V_{th(POR)L}$	LOW-level power-on reset threshold voltage	power-on reset		1.6	3.1	3.9	V
$V_{th(POR)H}$	HIGH-level power-on reset threshold voltage			2.3	3.4	4.3	V
$V_{hys(POR)}$	power-on reset hysteresis voltage		[2]	0.05	0.3	1	V
$V_{th(VBATL)L}$	LOW-level V_{BAT} LOW threshold voltage			3.9	4.4	4.7	V
$V_{th(VBATL)H}$	HIGH-level V_{BAT} LOW threshold voltage			4.2	4.7	4.9	V
$V_{hys(VBATL)}$	V_{BAT} LOW hysteresis voltage		[2]	0.15	0.3	0.6	V
Pins TXD and SLP_N							
V_{IH}	HIGH-level input voltage			2	-	7	V
V_{IL}	LOW-level input voltage			−0.3	-	+0.8	V
V_{hys}	hysteresis voltage		[2]	50	200	400	mV
R_{pd}	pull-down resistance	on TXD		50	125	325	kΩ
		on SLP_N		100	250	650	kΩ
Pin RXD (open-drain)							
I_{OL}	LOW-level output current	V_{RXD} = 0.4 V		2	-	-	mA
I_{LH}	HIGH-level leakage current		[2]	−5	-	+5	μA

Table 7. Static characteristics *...continued*

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V; unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Pin LIN							
I_{BUS_LIM}	current limitation for driver dominant state	V_{BAT} = 18 V; V_{LIN} = 18 V; V_{TXD} = 0 V		40	-	100	mA
$I_{BUS\_PAS\_dom}$	receiver dominant input leakage current including pull-up resistor	V_{BAT} = 12 V; V_{LIN} = 0 V; V_{TXD} = 5 V	[2]	−600	-	-	μA
$I_{BUS\_PAS\_rec}$	receiver recessive input leakage current	V_{BAT} = 5 V; V_{LIN} = 18 V; V_{TXD} = 5 V	[2]	-	0	1	μA
$I_{BUS\_NO\_GND}$	loss-of-ground bus current	V_{BAT} = 18 V; V_{LIN} = 0 V	[2]	−750	-	+10	μA
$I_{BUS\_NO\_BAT}$	loss-of-battery bus current	V_{BAT} = 18 V; V_{LIN} = 18 V	[2]	-	-	1	μA
V_{BUSdom}	receiver dominant state			-	-	$0.4V_{BAT}$	V
V_{BUSrec}	receiver recessive state			$0.6V_{BAT}$	-	-	V
V_{BUS_CNT}	receiver center voltage	V_{BUS_CNT} = (V_{BUSdom} + V_{BUSrec}) / 2		$0.475V_{BAT}$	$0.5V_{BAT}$	$0.525V_{BAT}$	V
V_{HYS}	receiver hysteresis voltage	V_{HYS} = V_{BUSrec} − V_{BUSdom}		-	-	$0.175V_{BAT}$	V
$V_{SerDiode}$	voltage drop at the serial diode	in pull-up path with R_{slave}; $I_{SerDiode}$ = 0.9 mA	[2]	0.4	-	1.0	V
$V_{O(dom)}$	dominant output voltage	Normal mode; V_{TXD} = 0 V; V_{BAT} = 7.0 V	[2]	-	-	1.4	V
		Normal mode; V_{TXD} = 0 V; V_{BAT} = 18 V	[2]	-	-	2.0	V
R_{slave}	slave resistance			20	30	60	kΩ
C_{LIN}	capacitance on pin LIN	with respect to GND	[2]	-	-	20	pF
Thermal shutdown							
$T_{j(sd)}$	shutdown junction temperature		[2]	150	-	200	°C

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

[2] Not tested in production; guaranteed by design.

11. Dynamic characteristics

Table 8. Dynamic characteristics

V_{BAT} = 5 V to 18 V; T_{vj} = −40 °C to +150 °C; $R_{L(LIN-VBAT)}$ = 500 Ω; all voltages are referenced to pin GND; positive currents flow into the IC; typical values are given at V_{BAT} = 12 V, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Duty cycles							
δ1	duty cycle 1	$V_{th(rec)(max)}$ = 0.744 × V_{BAT}; $V_{th(dom)(max)}$ = 0.581 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7 V to 18 V	[2][4][5]	0.396	-	-	
		$V_{th(rec)(max)}$ = 0.768 × V_{BAT}; $V_{th(dom)(max)}$ = 0.6 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5 V to 7 V	[2][4][5]	0.396	-	-	
δ2	duty cycle 2	$V_{th(rec)(min)}$ = 0.422 × V_{BAT}; $V_{th(dom)(min)}$ = 0.284 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 7.6 V to 18 V	[3][4][5]	-	-	0.581	
		$V_{th(rec)(min)}$ = 0.405 × V_{BAT}; $V_{th(dom)(min)}$ = 0.271 × V_{BAT}; t_{bit} = 50 µs; V_{BAT} = 5.6 V to 7.6 V	[3][4][5]	-	-	0.581	
δ3	duty cycle 3	$V_{th(rec)(max)}$ = 0.778 × V_{BAT}; $V_{th(dom)(max)}$ = 0.616 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7 V to 18 V	[2][4][5]	0.417	-	-	
		$V_{th(rec)(max)}$ = 0.805 × V_{BAT}; $V_{th(dom)(max)}$ = 0.637 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 5 V to 7 V	[2][4][5]	0.417	-	-	
δ4	duty cycle 4	$V_{th(rec)(min)}$ = 0.389 × V_{BAT}; $V_{th(dom)(min)}$ = 0.251 × V_{BAT}; t_{bit} = 96 µs; V_{BAT} = 7.6 V to 18 V	[3][4][5]	-	-	0.590	
		$V_{th(rec)(min)}$ = 0.372 × V_{BAT} $V_{th(dom)(min)}$ = 0.238 × V_{BAT} t_{bit} = 96 µs; V_{BAT} = 5.6 V to 7.6 V	[3][4][5]	-	-	0.590	
Timing characteristics							
t_{rx_pd}	receiver propagation delay	rising and falling; C_{RXD} = 20 pF; R_{RXD} = 2.4 kΩ	[5]	-	-	6	µs
t_{rx_sym}	receiver propagation delay symmetry	C_{RXD} = 20 pF; R_{RXD} = 2.4 kΩ; rising edge with respect to falling edge	[5]	−2	-	+2	µs
$t_{wake(dom)LIN}$	LIN dominant wake-up time	Sleep mode		30	80	150	µs
$t_{gotonorm}$	go to normal time	time period for mode change from Sleep or Standby mode to Normal mode		2	6	10	µs
$t_{init(norm)}$	normal mode initialization time			7	-	20	µs
$t_{gotosleep}$	go to sleep time	time period for mode change from Normal to Sleep mode		2	6	10	µs
$t_{to(dom)TXD}$	TXD dominant time-out time	timer started at falling edge on TXD		6	12	50	ms

[1] All parameters are guaranteed over the virtual junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.

[2] $\delta 1, \delta 3 = \frac{t_{bus(rec)(min)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(min)}$ is illustrated in the LIN timing diagram in Figure 5.

[3] $\delta2, \delta4 = \frac{t_{bus(rec)(max)}}{2 \times t_{bit}}$. Variable $t_{bus(rec)(max)}$ is illustrated in the LIN timing diagram in Figure 5.

[4] Bus load conditions: C_{BUS} = 1 nF and R_{BUS} = 1 kΩ; C_{BUS} = 6.8 nF and R_{BUS} = 660 Ω; C_{BUS} = 10 nF and R_{BUS} = 500 Ω.

[5] See timing diagram in Figure 5.

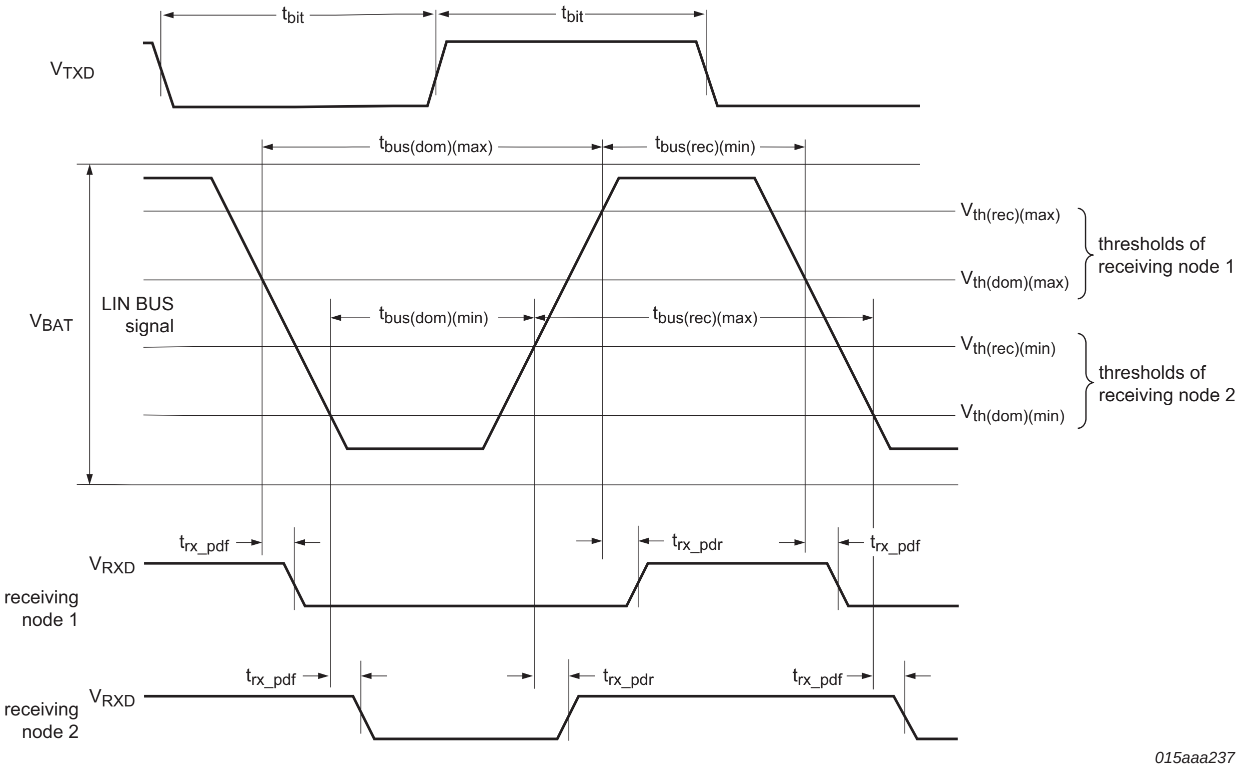
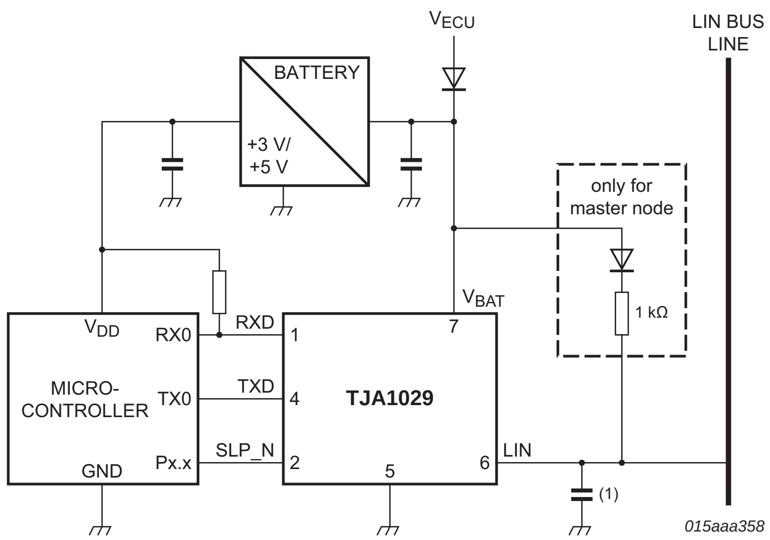


Fig 5. Timing diagram of LIN transceiver duty cycle

12. Application information

12.1 Application diagram



(1) Master: C = 1 nF; slave: C = 220 pF

Fig 6. Application diagram

12.2 ESD robustness according to LIN EMC test specification

ESD robustness (IEC 61000-4-2) has been tested by an external test house according to the LIN EMC test specification (part of Conformance Test Specification Package for LIN 2.1, October 10th, 2008). The test report is available on request.

Table 9. ESD robustness (IEC 61000-4-2) according to LIN EMC test specification

Pin	Test configuration	Value	Unit
LIN	no capacitor connected to LIN pin	±12	kV
	220 pF capacitor connected to LIN pin	±12	kV
V_{BAT}	100 nF capacitor connected to V_{BAT} pin	> |14|	kV

12.3 Hardware requirements for LIN interfaces in automotive applications

The TJA1029 satisfies the "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications", Version 1.3, May 2012.

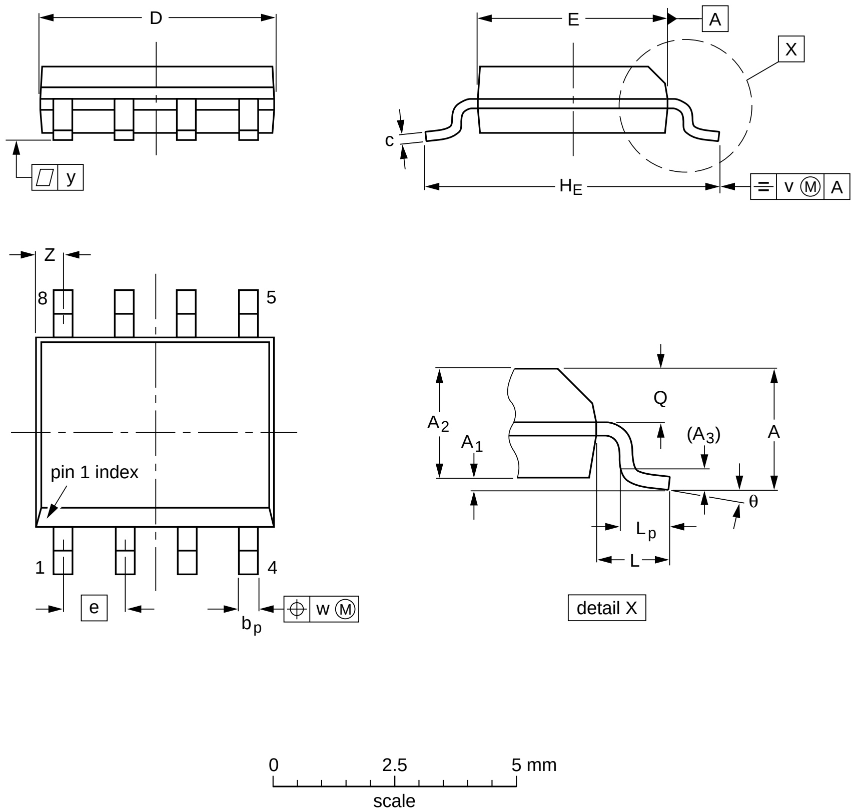
13. Test information

13.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive applications.

14. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

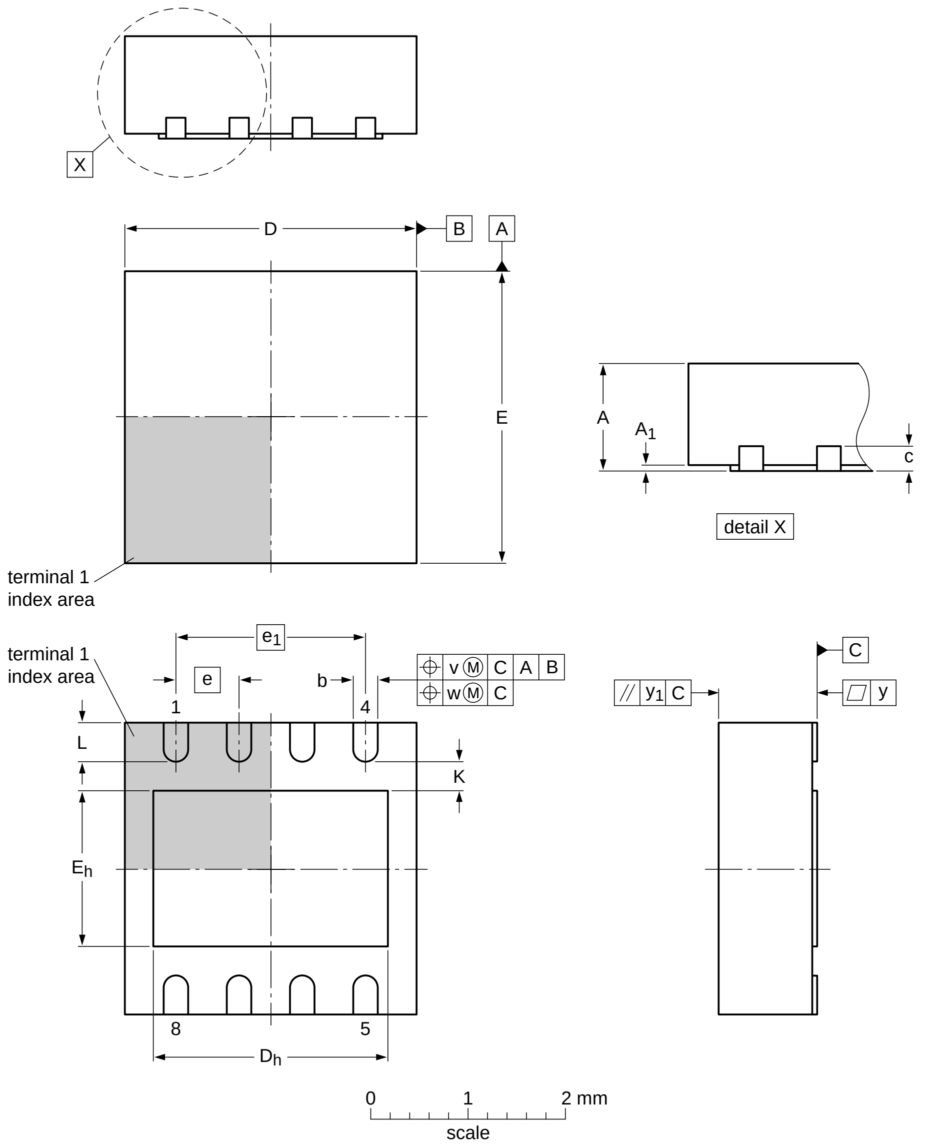
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 7. Package outline SOT96-1 (SO8)

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm **SOT782-1**



Dimensions

Unit(1)		A	A_1	b	c	D	D_h	E	E_h	e	e_1	K	L	v	w	y	y_1
	max	1.00	0.05	0.35		3.10	2.45	3.10	1.65			0.35	0.45				
mm	nom	0.85	0.03	0.30	0.2	3.00	2.40	3.00	1.60	0.65	1.95	0.30	0.40	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.25		2.90	2.35	2.90	1.55			0.25	0.35				

Note

1. Plastic or metal protrusions of 0.075 maximum per side are not included.

sot782-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT782-1	- - -	MO-229	- - -			~~09-08-25~~ 09-08-28

Fig 8. Package outline SOT782-1 (HVSON8)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 10 and 11

Table 10. SnPb eutectic process (from J-STD-020C)

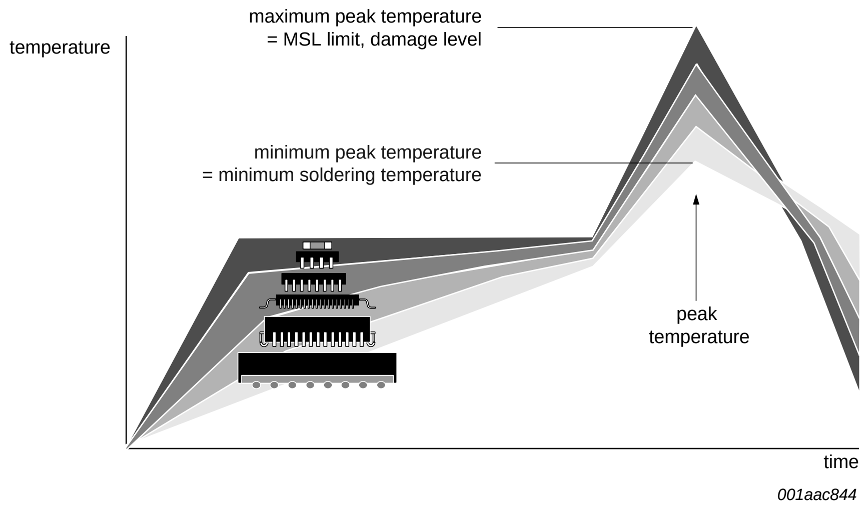
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 11. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

17. Soldering of HVSON packages

Section 16 contains a brief introduction to the techniques most commonly used to solder Surface Mounted Devices (SMD). A more detailed discussion on soldering HVSON leadless package ICs can be found in the following application notes:

- *AN10365 ‘Surface mount reflow soldering description”*
- *AN10366 “HVQFN application information”*

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1029 v.1	20130108	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

Date of release: 8 January 2013
Document identifier: TJA1029