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SL1711
Quadrature Downconverter
Preliminary Information

DS4032 ISSUE 4.0 October 1997

The SL1711 is a quadrature downconverter, intended primarily for application in professional and consumer digital satellite tuners.

The device contains all elements necessary, with the exception of external local oscillator tank to form a complete system operating at standard satellite receiver intermediate frequencies. It is intended for use with external carrier recovery.

The device includes a low noise RF input amplifier, a reference VCO with prescaler output buffer and In-phase and Quadrature mixers with baseband buffer amplifiers containing AGC gain control.

The SL1711 is optimised to drive a dual ADC converter such as the VP216.

The SL1711 utilises a power MP package, whereas the SL1711B variant uses a standard MP16 plastic package and features a revised operating temperature.

FEATURES

- Single chip system for wideband quadrature downconversion
- Compatible with all standard high IF frequencies
- Excellent gain and phase match up to 30MHz baseband
- High output referred linearity for low distortion and multi channel application
- Simple low component application
- Fully balanced low radiation design with fully integrated quadrature generation
- High operating input sensitivity
- On-board AGC facility
- On chip oscillator for varactor tuning or SAW resonator operation
- ESD protection (Normal ESD handling procedures should be observed)

APPLICATIONS

- Satellite receiver systems
- Data communications systems
- Cable systems

Ordering Information

SL1711/KG/MH1P (Sticks)

SL1711/KG/MH1Q (Tape and Reel)

SL1711B/KG/MP1S (Sticks)

SL1711B/KG/MP1T (Tape and Reel)

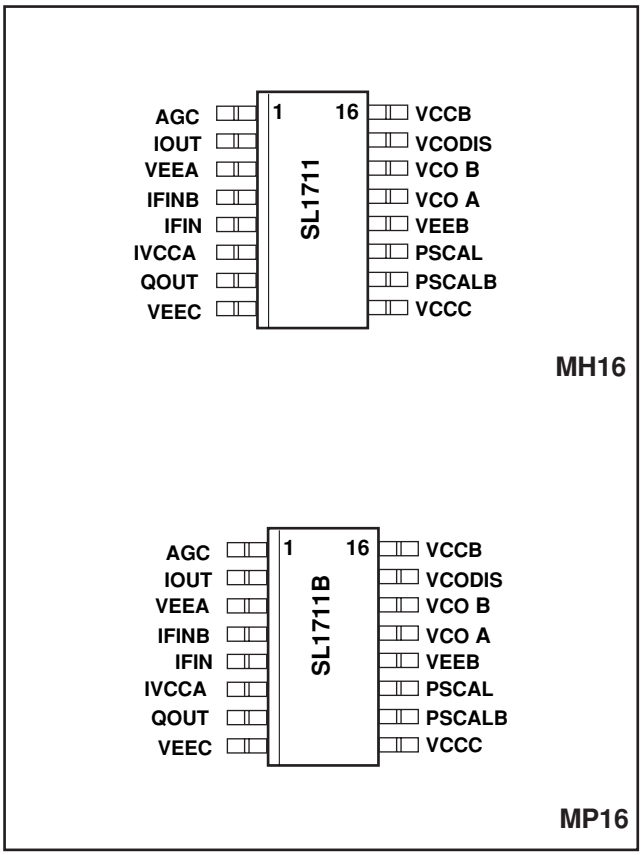


Fig. 1 Pin allocation

QUICK REFERENCE DATA

Characteristic	Value	Units
Input noise figure, DSB	17	dB
Maximum conversion gain	44	dB
Minimum conversion gain	28	dB
$IP3_{2T}$ output referred	+8	dBV
Output clip voltage	1.5	Vp-p
Gain match up to 22MHz	± 0.3	dB
Gain match up to 30MHz	± 0.5	dB
Phase match up to 30MHz	± 1.5	deg
Gain flatness up to 30MHz	± 0.5	dB
VCO phase noise, SSB @ 10kHz offset	- 96	dBc/Hz
Prescaler division ratio	32	
Prescaler output swing	1.6	Vp-p

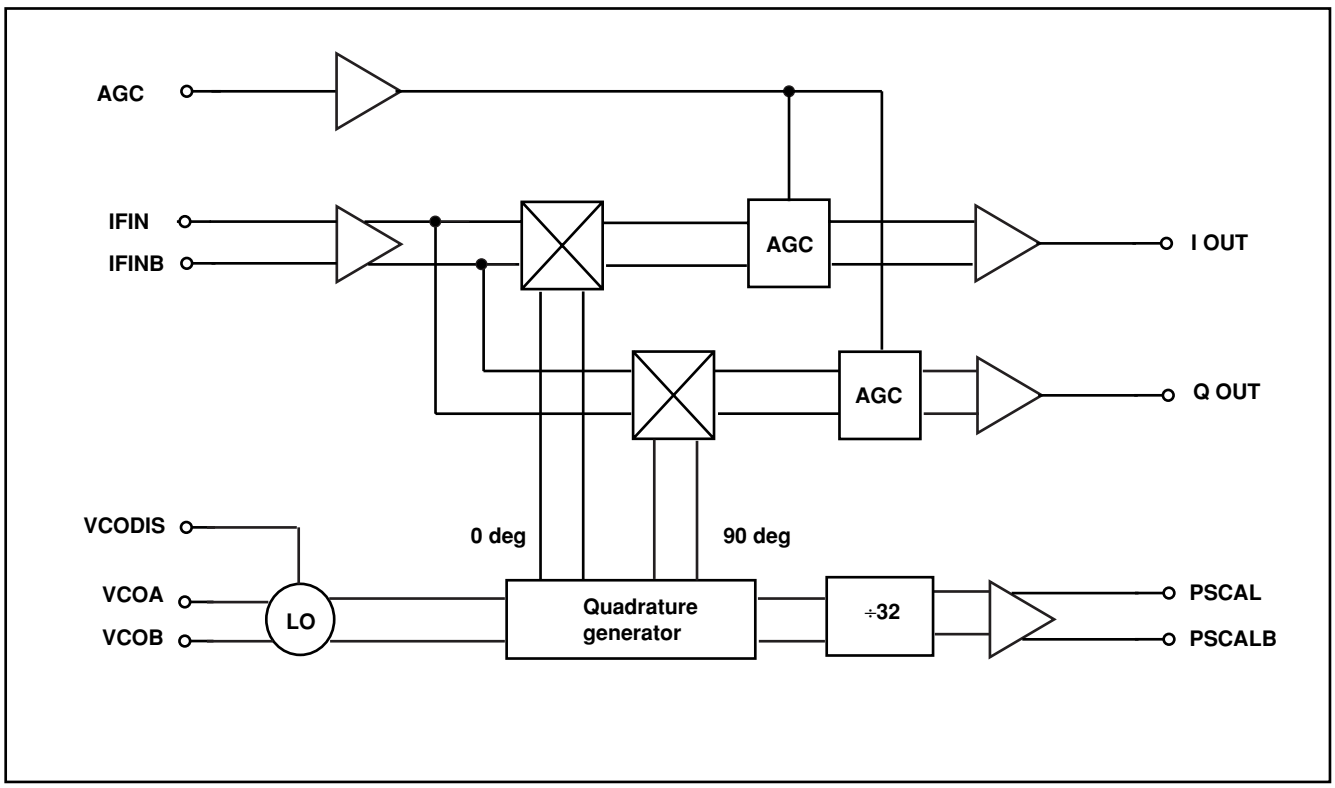


Fig. 2 SL1711 block diagram

FUNCTIONAL DESCRIPTION

The SL1711 is a wideband quadrature downconverter, optimised for application in both professional and consumer digital satellite receiver systems and requiring a minimum external component count. It contains all the elements required for construction of a quadrature demodulator, with the exception of tank circuit for the local oscillator.

A block diagram is shown in Fig. 2.

The SL1711 oscillator can be used with either a varator tuned tank circuit or with a SAW resonator. Both configurations are described in the Application Notes section of this Data Sheet.

A typical digital satellite tuner application from tuner input to data transport stream is shown in Fig. 13

In normal application the second satellite IF frequency of typically 402.75 or 479.5 MHz is fed from the tuner SAW filter to the RF preamplifier, which is optimised for impedance match and signal handling. The amplifier output signal is then split into two balanced channels to drive the In-phase and Quadrature mixers. The typical RF input impedance is shown in Fig. 3

In-phase and Quadrature LO signals for the mixers are derived from the on board local oscillator, which uses an external varactor tuned resonant network and is optimised for low phase noise. The VCO also drives an on board divide by 32 prescaler whose outputs can be used for driving an external PLL control loop for the VCO, where the PLL loop is contained within the QPSK demodulator, for example the VP305. For optimum performance in the varactor tuned application the VCO should be fully symmetric. The VCO has a disable facility by grounding pin 15, VCODIS; in normal applications this pin is pulled to Vcc via a 4K7 resistor.

The mixer outputs are fed to balanced baseband AGC amplifier stages, which provide for a minimum of 16 dB of AGC control. The typical AGC characteristic is shown in Fig. 4.

These amplifiers then feed a low output impedance true differential to single-ended converter output stage. In normal application the output can be either directly AC coupled to the ADC converter such as the VP216, which will generally have a high input impedance, or to drive an anti alias filter. In this later case the maximum load presented to the SL1711 must not exceed a parallel combination of 1KΩ and 20pF. The typical baseband output impedance is contained in Fig. 5.

It is recommended that the device is operated with an output amplitude of 760mV under lock conditions.

Under transient conditions the output should not exceed the clipping voltage.

Input and output interface circuitry is contained in Fig. 6.

The typical key performance figures at 480 MHz IF, 5V Vcc, 1 kΩ load and 25 deg C ambient are contained in table headed 'QUICK REFERENCE DATA'. With SAWR oscillator application the gain and phase match performance will typically exceed these numbers.

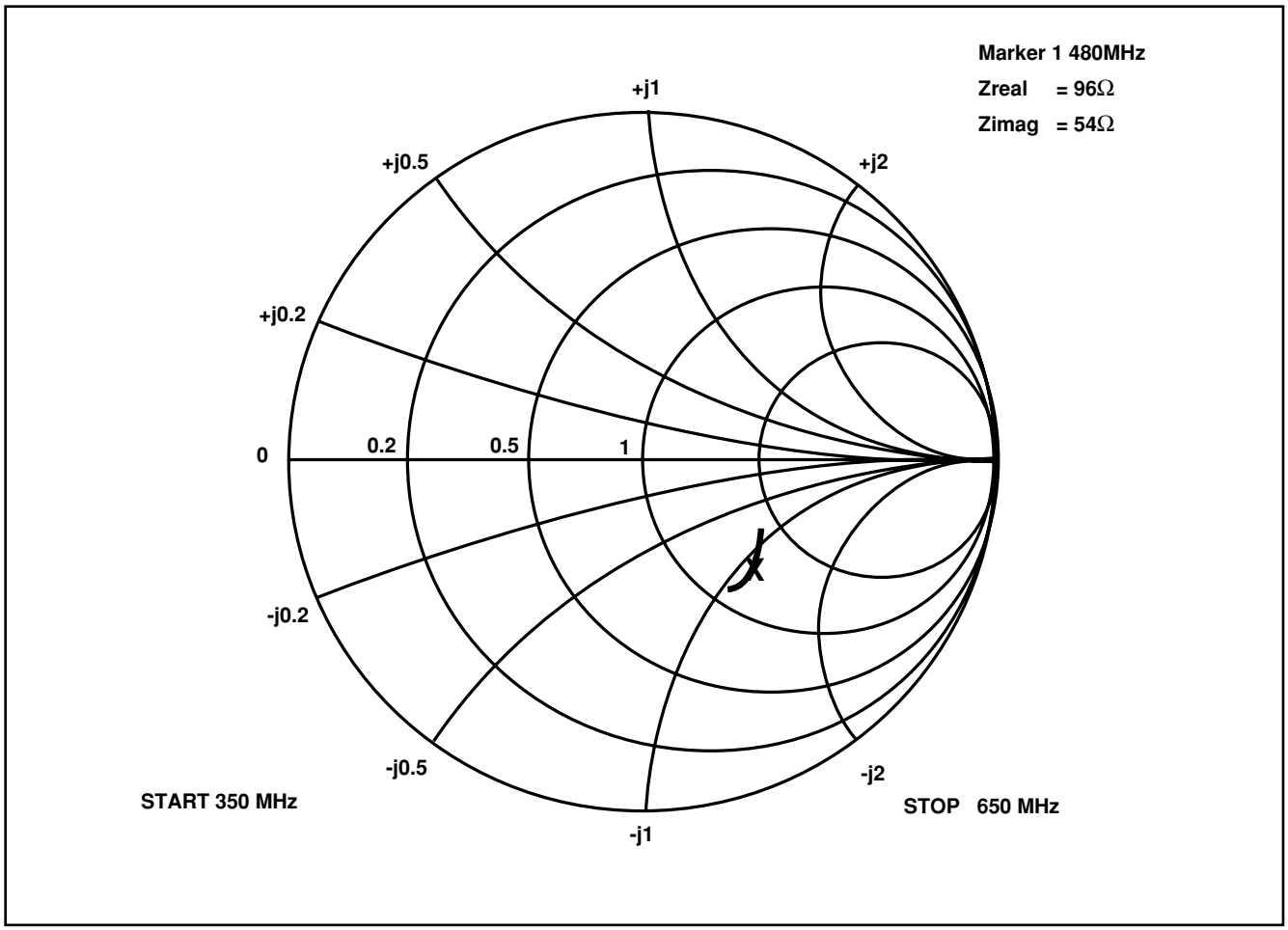


Fig.3 Typical RF input impedance

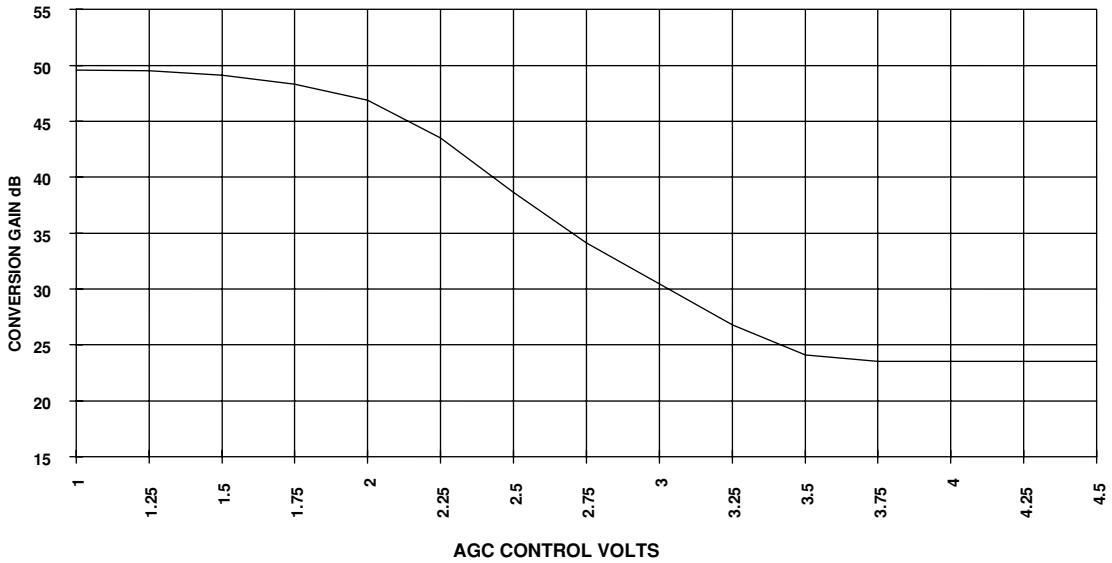


Fig.4 Typical AGC characteristic

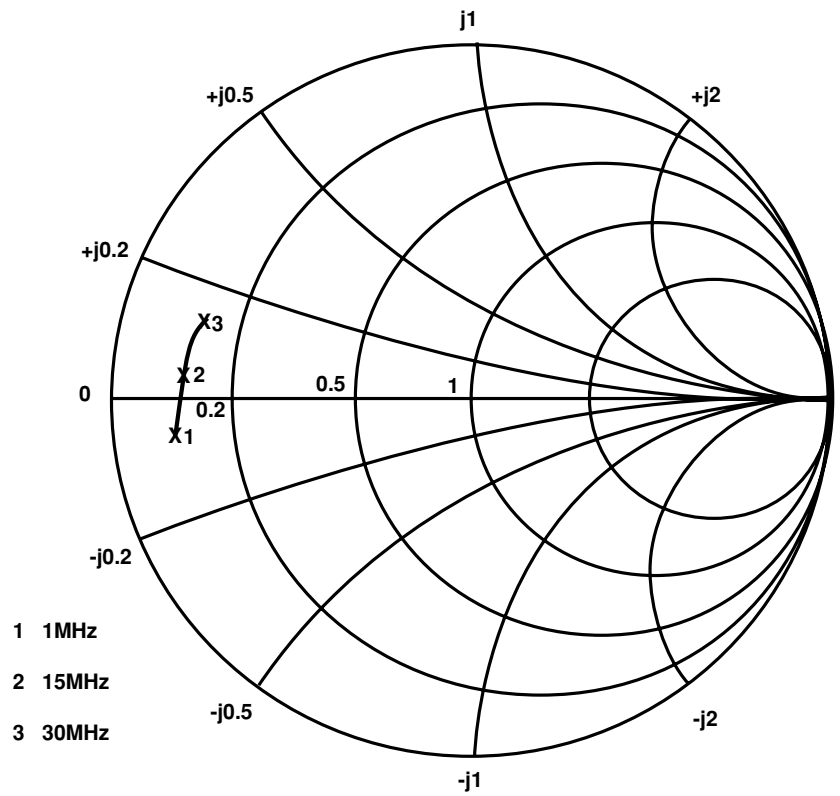
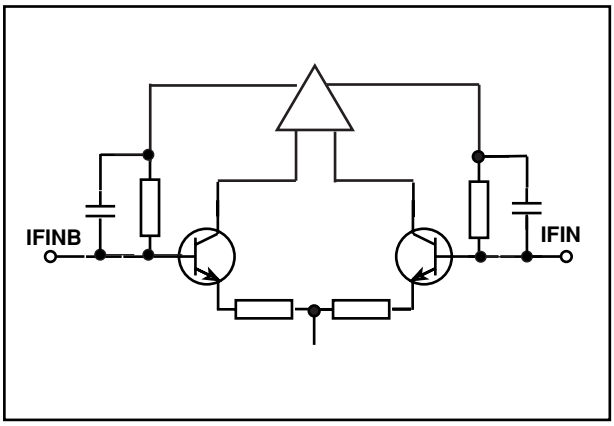
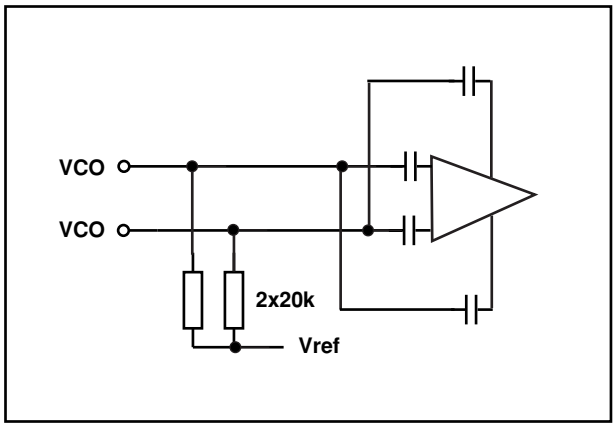


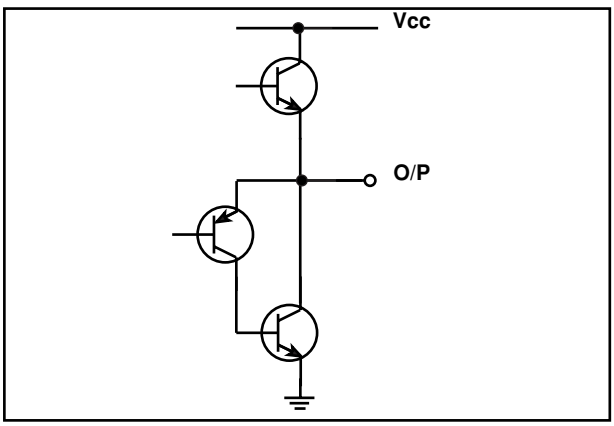
Fig. 5 Typical baseband output impedance



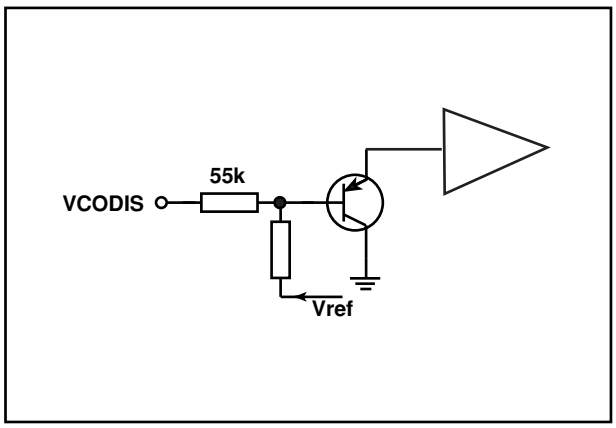
IF Input



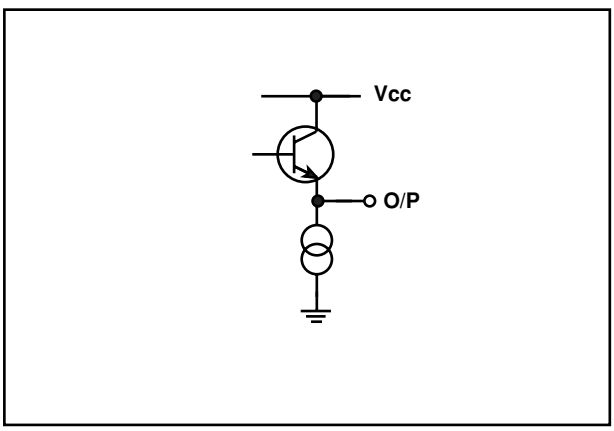
VCO



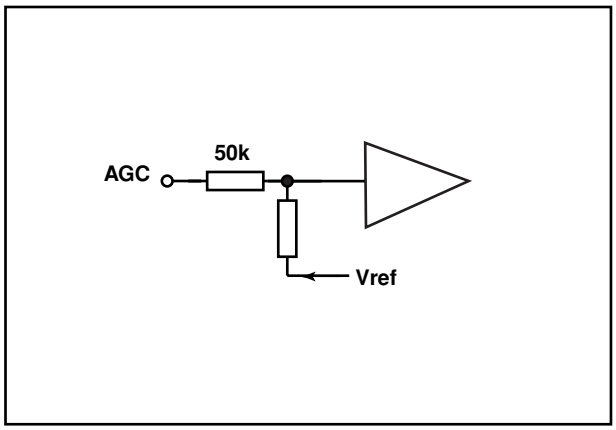
I & Q baseband output



VCO disable input



Prescaler outputs



AGC input

Fig. 6 I/O port peripheral circuitry

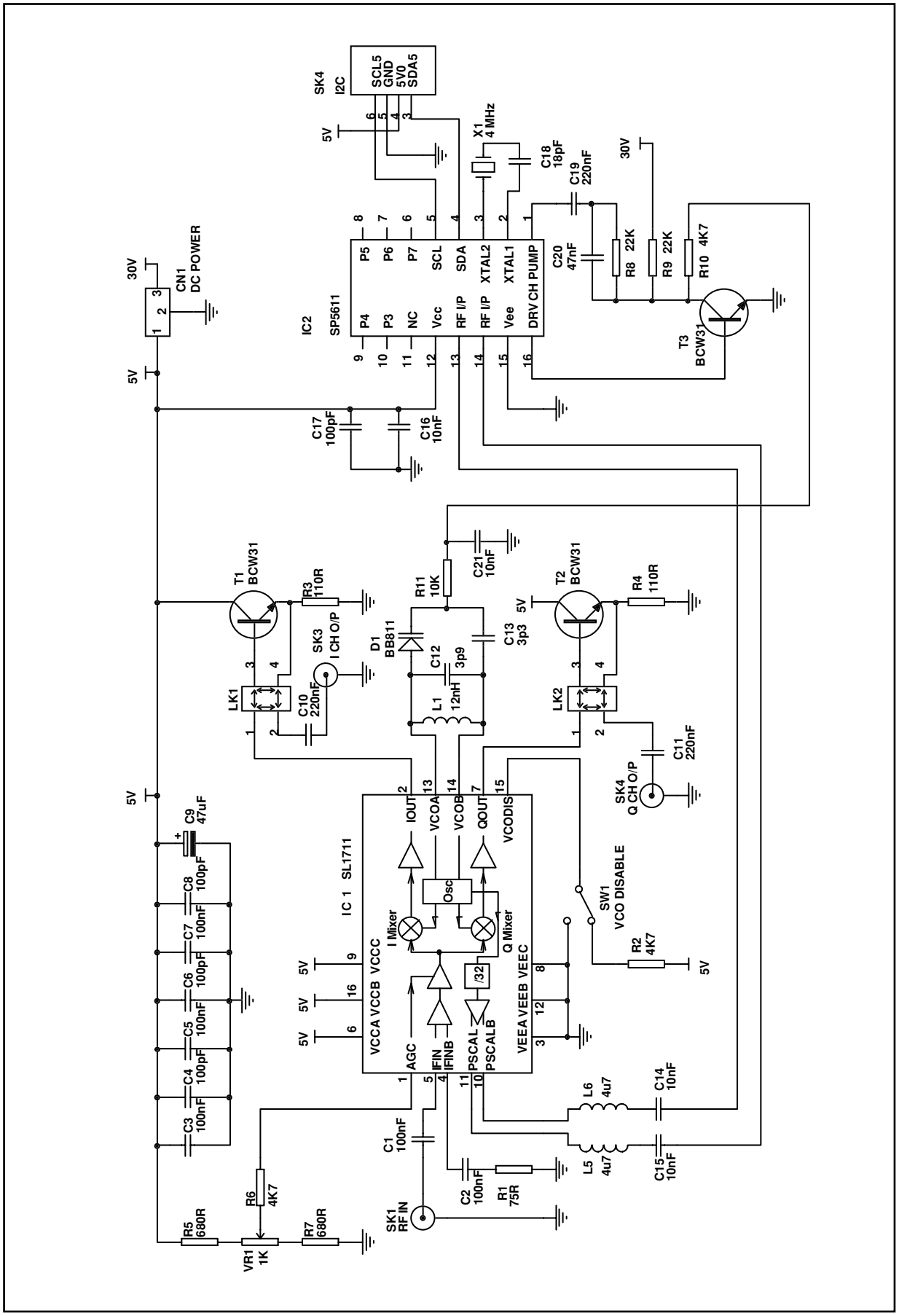


Fig.7 SL1711 standard evaluation board

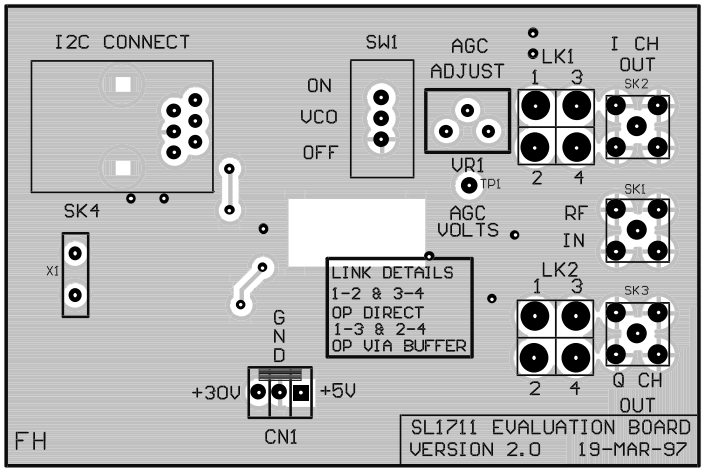

I2C CONNECT
SW1
ON
VCO
OFF
AGC
ADJUST
VR1
TP1
LK1
1 3
2 4
I CH
OUT
SK2
SK1
RF
IN
SK4
X1
AGC
VOLTS
LINK DETAILS
1-2 & 3-4
OP DIRECT
1-3 & 2-4
OP VIA BUFFER
LK2
1 3
2 4
SK3
Q CH
OUT
G
N
D
+30V
+5V
CN1
FH
SL1711 EVALUATION BOARD
VERSION 2.0 19-MAR-97

Fig.8

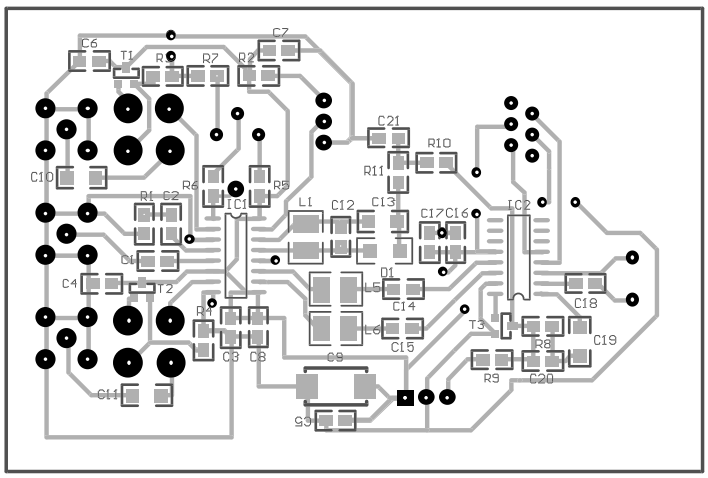

C6
T1
R7
R2
C7
C21
R10
R11
C10
R6
R5
R1
C2
IC1
L1
C12
C13
C17
C16
IC2
C1
C4
T2
D1
L5
C14
C18
R4
L6
C15
T3
R8
C19
C3
C8
C9
R9
C20
C11
C5

Fig.9

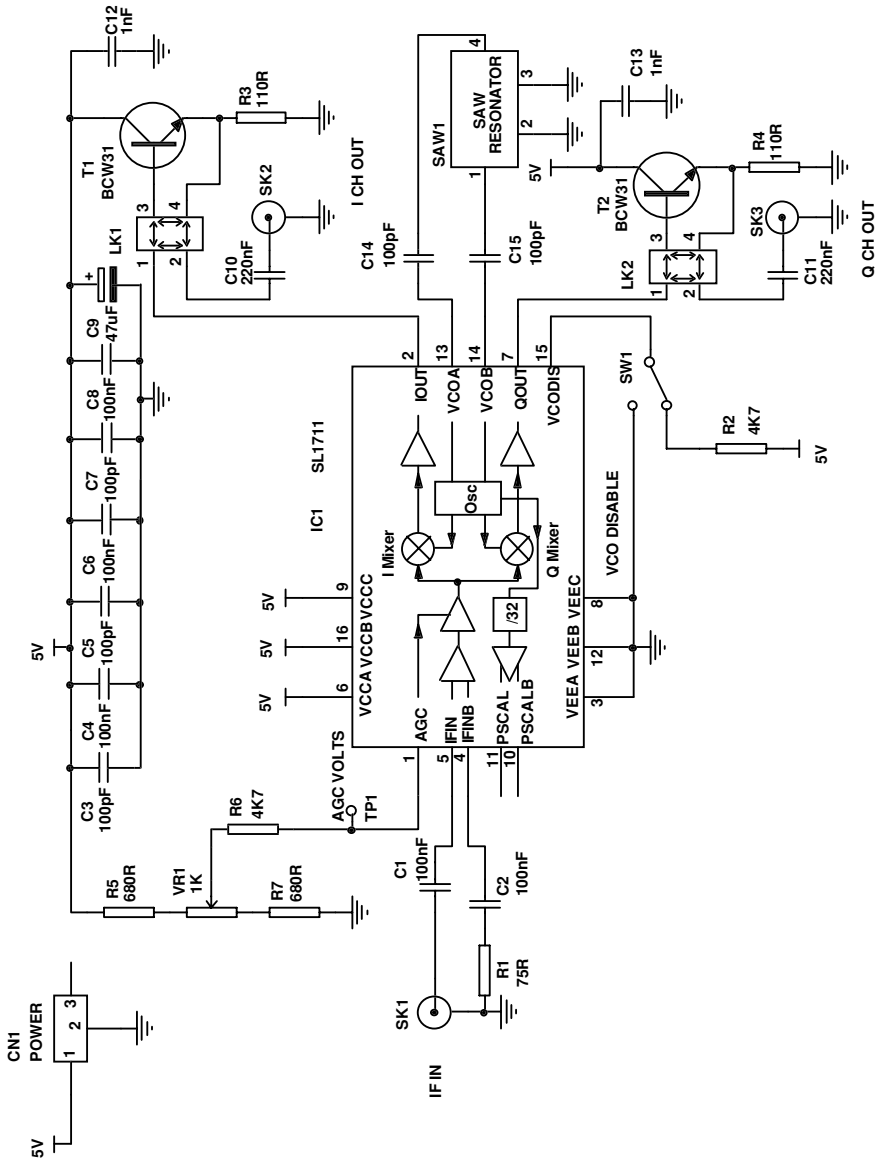


Fig.10. SL1711 I & Q downconverter with SAW resonator

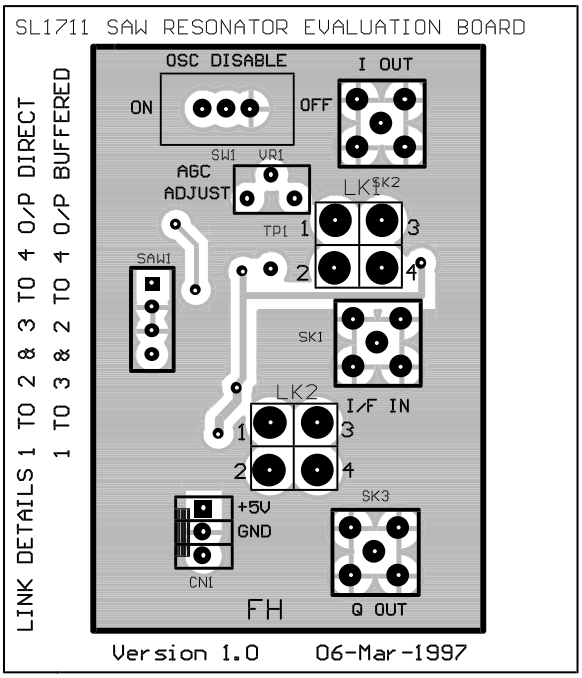

SL1711 SAW RESONATOR EVALUATION BOARD
OSC DISABLE
ON
OFF
I OUT
SW1
VR1
AGC
ADJUST
LK1
SK2
TP1
1
2
3
4
SAW1
SK1
LK2
I/F IN
+5V
GND
SK3
CN1
FH
Q OUT
Version 1.0
06-Mar-1997
LINK DETAILS 1 TO 2 & 3 TO 4 O/P DIRECT
1 TO 3 & 2 TO 4 O/P BUFFERED

Fig. 11

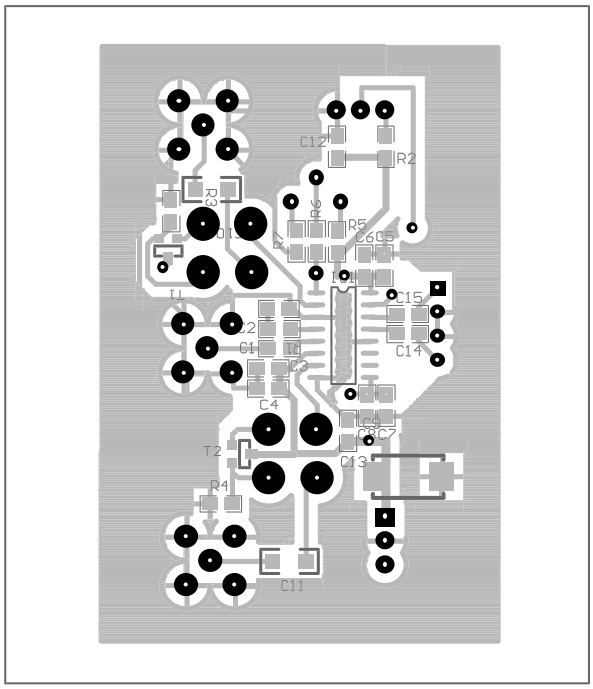


Fig. 12

APPLICATION NOTES

These application notes should be read in conjunction with circuit diagrams contained in Fig. 7 and 10, and a recommended front end tuner solution contained in Fig. 13. These boards have been designed to demonstrate performance and to allow for initial evaluation of the SL1711.

Varator Tuned Oscillator

Refer to Fig. 7 circuit diagram and Figs. 11 and 12 PCB layout.

This application uses a synthesised VCO with a tuning range of 460 MHz to 500 MHz. The surface mount inductor L1 is 12 nH. The VCO frequency is controlled by the SP5611 synthesiser which is programmed via an I^2C bus. The RF input to the synthesiser is from the SL1711 prescaler outputs coupled via RF inductors L3 and L4.

For functional checking the VCO can be tuned by physically shorting the base of transistor T3 to ground and then adjusting the +30 volt supply to tune the VCO. Under these conditions, due to the unlocked state of the LO, the board WILL NOT BE representative of locked gain and phase match or phase noise performance.

In real applications such the VCO control voltage will be provided by the QPSK demodulator circuit, such as the VP305. This circuit provides a line voltage to align the reference LO in the 1711 in both frequency and phase to the centre of the modulation bandwidth, normally 402.75 or 479.5 MHz.

As in all feedback loops the bandwidth of the varactor line must be optimised for the symbol rate of the received modulation.

It is recommended for optimum performance that the VCO application is implemented symmetrically, in presented drive and impedance to the VCO ports, as demonstrated in the evaluation schematic and PCB.

In the recommended application the varactor diodes are referenced to the VCO port DC bias voltages. This limits the minimum tuning voltage on the varactor line to 3V. If lower tuning voltage is required the tank can be AC coupled to the VCO ports by 390pF capacitor and a DC reference voltage for the varactor diodes applied by centre tapping the tank inductors. NB the varactor diodes require a minimum of 1V reverse bias for correct operation.

In real applications the maximum tuning range required for the VCO will be determined by the required lock range of the tuner and the manufacturing tolerance of the tank, assuming the quadrature downconverter section will be alignment free. This tuning range will be typically be much smaller than the demonstration board, which will consequently improve the VCO phase noise performance.

This application can be ported direct to real system implementations. Normal good RF practice must be applied to the layout implementation.

Prescaler Outputs (varactor tuned VCO)

The VCO frequency divided by 32 is available at the differential prescaler outputs, pins 10 and 11. These enable the VCO frequency to be synthesised by a PLL frequency synthesiser; on the demo board an SP5611 is used for this function however in a real application this function will be provided by the QPSK demodulator function contained in for example the VP305

It is recommended that the prescaler outputs are loaded symmetrically to balance radiation effects.

Saw Resonator Oscillator

Refer to Fig. 10 circuit diagram and Figs 11 and 12 PCB layout.

In the standard application the oscillator uses a varactor diode tuned tank circuit which allows fine tuning of the oscillator frequency via a voltage control line. This control voltage is usually derived from the QPSK/FEC decoder VP305/VP306

Certain applications do not require this fine tune facility so a fixed frequency application using a SAW resonator has been developed. In this application the frequency of the oscillator is determined by the SAW resonator. The SAW is AC coupled into the VCO pins of the device pins 13 and 14 via 100pF coupling capacitors.

The SAW resonator used in this application is a ;

Murata Part No SAR479.45MB10X200

Prescaler Outputs (SAWR tuned VCO)

The VCO frequency divided by 32 is available at the differential prescaler outputs, pins 10 and 11. Normally these outputs will not be required since the derotation and fine tuning required will be processed by the QPSK demodulator. However these frequencies could be used if required for other system reference frequencies or clocks.

If used it is recommended that the prescaler outputs are loaded symmetrically to balance radiation effects.

VCO Disable

The on-chip oscillator can be disabled by connecting VCODIS, pin 15, to ground and enabled by connecting to Vcc via a 4k7 Ω pull up resistor.

AGC

The AGC facility can be used to control the conversion gain of the SL1711.

On the demonstration boards the conversion gain is adjusted by means of a potentiometer, which is set to 2.5V so giving a conversion gain of 38 dB. The voltage adjustment range for the AGC is approximately 1.5 to 3.5 V.

It is important that the AGC voltage minimum does not give a conversion gain of greater than 44dBs otherwise the channel amplitude match may be degraded. In real applications the AGC can be either set at a fixed control voltage or controlled by means of the AGC control signal from the QPSK demodulator dependant on the overall dynamic range requirement of the tuner and it's gain distribution.

I & Q baseband outputs

The SL1711 offers a greatly improved drive capability over the SL1710 and as such is much less sensitive to the load conditions.

It is still important however to carefully balance the loads presented to the SL1711 to ensure no differential gain or phase degradation is introduced by the load circuits, which will also include effects due to track striplines etc.

For demonstration purposes the output is unsuitable for connection via co-axial cables to standard test equipment, where such equipment is normally 50 Ω or highly capacitive.

To overcome this problem the outputs of the SL1711 are therefore buffered through emitter followers which are optimised to drive 50 Ω loads without appreciable degradation in the SL1711 performance. These buffer stages are selectable so enabling the outputs to be loaded directly for interfacing direct with an ADC via a low capacitive link.

In most applications the SL1711 will normally interface direct into the ADC converter such as the VP216, which will present a >1 kΩ low capacitive load, though it can interface with lower impedances if desired.

The output is optimised for typical drive levels of 760 mVp-p and the onset of clipping is typically > 1.5V.

Care must be taken with system design to ensure that the I and Q baseband output signals never exceed 1.2V pk-pk. Any gross distortion in the output waveform caused by overdriving the output stages will compromise the system performance.

Device performance characteristics can only be guaranteed if the device is operated below the onset of clipping.

SL1711 Evaluation Board

This board has been created to show the operation of the SL1711 I/Q downconverter.

It does not attempt to simulate a real system, since in practice the 479.5MHz IF oscillator on the SL1711and the 60MHz clock on the subsequent ADC would be controlled via the baseband IQ demodulator chip such as the VP305 which follows the dual channel ADC. For simplicity, the VCO is locked using Zarlink Semiconductor SP5611 synthesiser, controlled via an I2C bus.

For full evaluation, 30V and 5V supplies are necessary.

Supplies

The board must be provided with the following supplies:

A) 5V for the SL1711 and SP5611 and 30V for the varactor line.

The supply connector is a 3 pin 0.1" pitch pin header. The centre pin of the connector is GND.

Outputs driven into hard clipping can exhibit amplitude decline. AGC loops should be designed to take account of this.

I^2C Bus connections

The board is provided with an RJ11 I^2C bus connector which feeds directly to the SP5611 synthesiser.

This connects to a standard 6-way connector cable which is supplied with the I^2C/3-wire bus interface box.

Input and Output connections

The board is provided with the following connectors:

A) IF I/P SMA connector SK1 which is AC coupled to the RF input of the SL1711.

B) I CH OUT SK2 and Q CH OUT (SK3) which provide either a buffered or direct baseband output signal from the SL1711 (depending on which way the links LK1 and LK2 are set). The output buffers should be used when driving 50Ω test equipment or co-axial lines.

Links and Switches

The board is provided with the following:

VCO DISABLE switch

This disables the VCO of the SL1711. It does NOT power down the chip.

AGC ADJUST potentiometer

The potentiometer sets the AGC input voltage of the SL1711 which controls the gain of the chip. TP1 is provided as a means of monitoring the AGC voltage.

LK1 and LK2

These are links which may be placed either vertically or horizontally to connect the outputs of the SL1711 either directly or via buffers to the SMA output connectors of the board.

If the links are placed vertically 1-2 and 3- the outputs are connected directly.

If the links are placed horizontally 1-3 and 2- the ouputs are connected via buffers.

Programming of Synthesisers

A SP5611 synthesiser is used to set the frequency of the SL1711 VCO 480MHz. Since the SL1711 incorporates a divide by 32 the synthesised frequency that the SP5611 must be programmed to is 480/32=15MHz.

Example
a) To program the SL1711 to 480MHz.

I2C Byte	Hex Code
Byte 1 (address)	C2
Byte 2 (programmable divider 8 MSBs)	00
Byte 3 (programmable divider 8 LSBs)	F0
Byte 4 (control data)	CE
Byte 5 (port data)	00

C2 is the address byte byte 1.

0F00 is the programmable divider information bytes 2 and 3.

CE is the control data information byte 4.

**Note - the programmable divider information should be set to program 480MHz /32 = 15MHz since the SL1711 provides a divide by 32 prescaler output rather than the VCO carrier frequency.

It is not possible to program the VCO to 479.5MHz when using a 7.8125kHz phase comparator frequency. The minimum step size is 7.8125kHz x 8 (RF prescaler inside SP5611) x 32 (SL1711 output prescaler) = 2MHz.

If the reference divider is set to 1024 mode3.90625kHz phase comparator frequency, the minimum step size will be 1MHz.

This may be achieved by programming the control byte to CC and modifying the programmable divider information for the new step size.

SL1711 Operation

The SL1711 will mix an IF input with its own local oscillator. This is controlled as above via a SP5611 synthesiser.

Normally the VCO will be set to the same frequency as the IF input, and the signal mixed directly down to baseband.

Alternatively, a CW RF source may be fed into the input of the SL1711 which is deliberately offset from the VCO. By varying the offset from 0-20MHz and monitoring the I and Q channel baseband outputs, the flatness response of the chip/output filter can be measured.

The SL1711 oscillator may also be disabled by setting the ON-VCO-OFF switch to the OFF position.

An AGC voltage adjust pot marked AGC ADJUST is provided, together with a test point.

Measurement of Gain and Phase Match.

a) Synthesise the required frequency 480MHz is used in the example above.

b) Connect an RF signal generator to the input.

c) Input a signal which should give an output of approx 0dBm (0.707V p-p), in combination with the appropriate AGC setting.

d) Connect a vector voltmeter to the BUFFERED outputs when using 50Ω inputs. When using high impedance probes, the direct outputs may be used. Selection of outputs is via the on board U links.

e) CALIBRATE the vector voltmeter and the leads to be used.

The calibration should be performed at the chosen baseband frequency and level for maximum accuracy.

f) Vary the RF input frequency either side of the LO and note the relative I and Q gain and phase reading.

If you experience any difficulties with this board, or require further help, please contact *Robert Marsh* on 01793 518234 or *Fred Herman* on 01793 518423

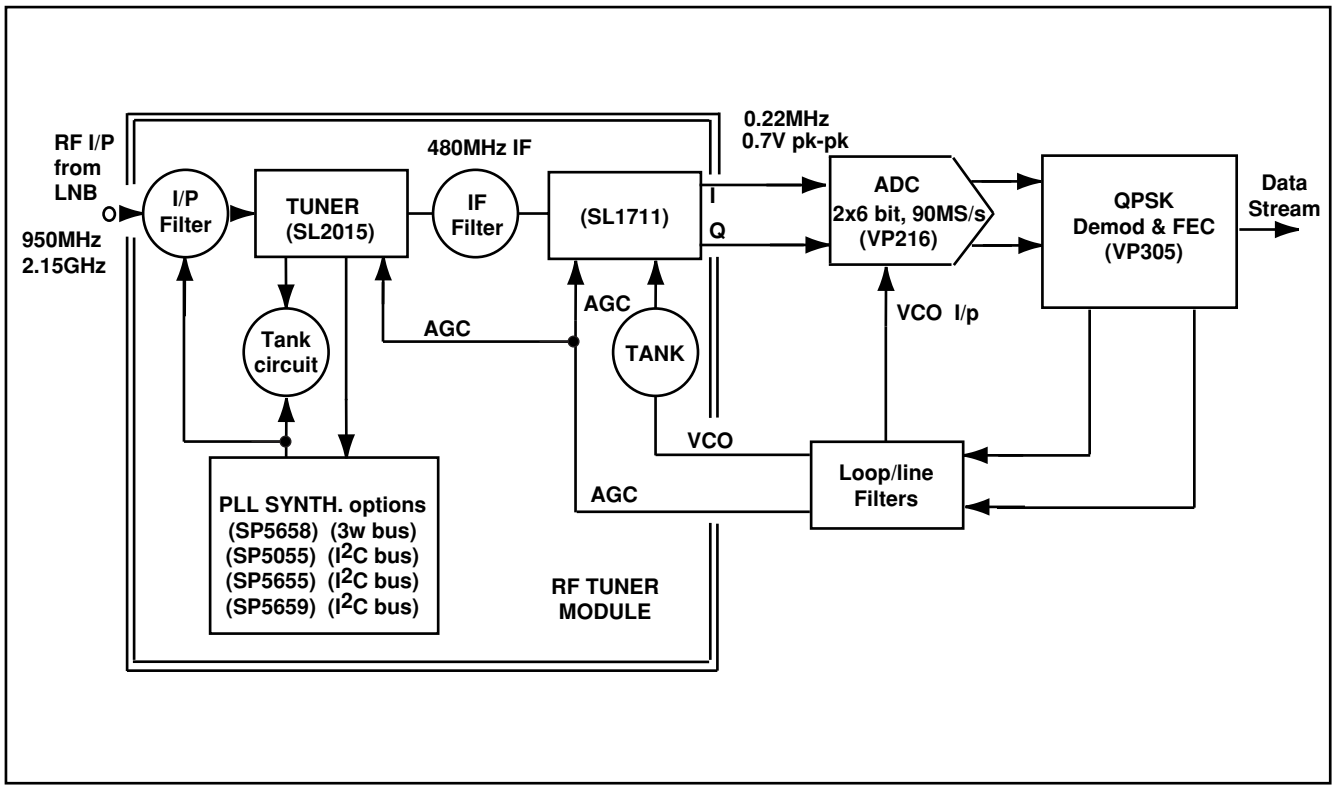


Fig.13 Example digital front end architecture

Note: All ICs shown in Fig. 13 are available from Zarlink Semiconductor.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb}= 0°C to 85°C,* V_{ee}= 0V, Vcc = 4.75 to 5.25 V, Fif = 479.5 MHz, IF bandwidth ± 22 MHz, output amplitude -11dBV

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Min	Typ	Max	Units	Conditions
Supply voltage	6,9,16	4.75		5.25	V	
Supply current	6,9,16		109	125	mA	
IF input operating frequency (1)	4, 5	350		550	MHz	
IF input impedance	4, 5		75		Ω	Over specified frequency operating range, see Fig. 6.
Input return loss	4, 5	12			dB	Over specified frequency operating range, see Fig. 6.
Input noise figure, DSB	4, 5		17	19	dB	Maximum gain setting
Variation in NF with gain setting				1	dB/dB	
VCO operation range		350		550	MHz	Centre frequency and tuning range determined by application.
VCO phase noise, SSB @ 10kHz offset			96	-85	dBc/Hz	Varactor tuned, determined by application.
VCO Vcc sensitivity				2E3	ppm/V	Free running
VCO temperature stability				100	ppm/°C	Uncompensated
Prescaler output swing	10, 11	1.2	1.6		Vp-p	
Prescaler output duty cycle	10, 11	40	50	60	%	
Conversion gain for AGC setting of;						See Fig. 4
1.5V		44			dB	Terminated voltage conversion gain from 50Ω source to 1kΩ load
2.5V			38		dB	
3.5V				28	dB	
AGC input current	1			100	µA	All AGC settings
I Q gain match			±0.3	±1	dB	See Note 3.
I Q gain match			±0.5	±1	dB	See Note 4.
I Q phase match			±1.5	±3	deg	See Note 4.
I & Q channel in band ripple			±0.3	±1	dB	see Note 3.
I & Q channel in band ripple			±0.5	±1	dB	See Note 4.
I Q crosstalk			-29	-20	dB	See Note 4 and Note 2 for derivation of cross modulation

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise stated)

T_{amb}= 0°C to 85°C,* V_{ee}= 0V, Vcc = 4.75 to 5.25 V, Fif = 479.5 MHz, IF bandwidth +- 22 MHz

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

Characteristic	Pin	Min	Typ	Max	Units	Conditions
I & Q baseband output impedance	2,7		8	20	Ω	See note (5), and Fig. 5.
I & Q baseband output clipping level	2, 7	1.2	1.5		Vp-p	See note(6), into 1KΩ load up to 22MHz baseband
$IP3_{2T}$, output referred		+3	+9		dBV	2 input carriers at -39 dBV within IF bandwidth of ±22MHz AGC set to give composite output of -11 dBV, IM3 tone within baseband bandwidth
$IM3_{2T}$ output referred				-40	dBc	2 input carriers within IF bandwidth of ±22MHz, AGC set to give composite output of -11 dBV, IM3 tone within baseband bandwidth
All prescaler and other spurs in I & Q baseband output.				-30	dBc	0.1 - 100MHz, referred to output amplitude of - 11 dBV.
Power supply rejection		20			dBc	Attenuation Vcc to I & Q outputs, over 0-500kHz

Notes:
1. Performance not guaranteed over full specified IF input operating range
2. I Q crosstalk is determined from the gain and phase match by the following formula
   Crosstalk = 20* Log (tan(phase error + Atan (1+amplitude imbalance) -45°))
3. Over specified gain dynamic, 1kΩ load up to 22MHz baseband
4. Over specified gain dynamic range, 1kΩ load up to 30MHz baseband
5. Baseband bandwidth 0.1 to 22MHz
6. The device should not be operated beyond the point of output clipping. The quality and amplitude of the baseband output signals cannot be guaranteed once this level has been exceeded.
7. * Operating temperature range for the SL1711B is 0°C to 70°C. This applies to applications featuring a double sided copper board. For other applications not using such a board, the maximum operating temperature may be reduced.
8. The above device characteristics are guaranteed provided the output is maintained below the onset of clipping.

ABSOLUTE MAXIMUM RATINGS

All voltages are reffered to Vee at 0V

Characteristics	Min	Max	Units	Conditions
Supply voltage, Vcc	-0.3	7	V	
IFFIN &IFINB input voltage		2.5	Vp-p	
IFIN & IFINB input DC offset	-0.3	Vcc+0.3	V	
IOUT & QOUT DC offset	-0.3	Vcc+0.3	V	
AGC DC offset	-0.3	Vcc+0.3	V	
VCO1 & 2 DC offset	-0.3	Vcc+0.3	V	
VCODDIS DC offset	-0.3	Vcc+0.3	V	
PSCAL & PSCALB DC offset	-0.3	Vcc+0.3		
Storage temperature	-55	125	°C	
Junction temperature		150	°C	
PSOP16 package thermal resistance, chip to ambient		TBA	°C/W	
PSOP16 package thermal resitance, chip to case		TBA	°C/W	
MP16 package thermal resistance chip to Ambient		81	°C/W	
MP16 package thermal resistance chip to case		28	°C/W	
Power consumption at 5.25V		657	mW	
ESD protection	2		kV	Mil std 883B method 3015 cat 1

ADDITIONAL INFORMATION REGARDING THE PSOP PACKAGE.

The following information should be noted when using the PSOP package fitted to the SL1711.

(a) This package uses the standard SOIC 16 footprint.

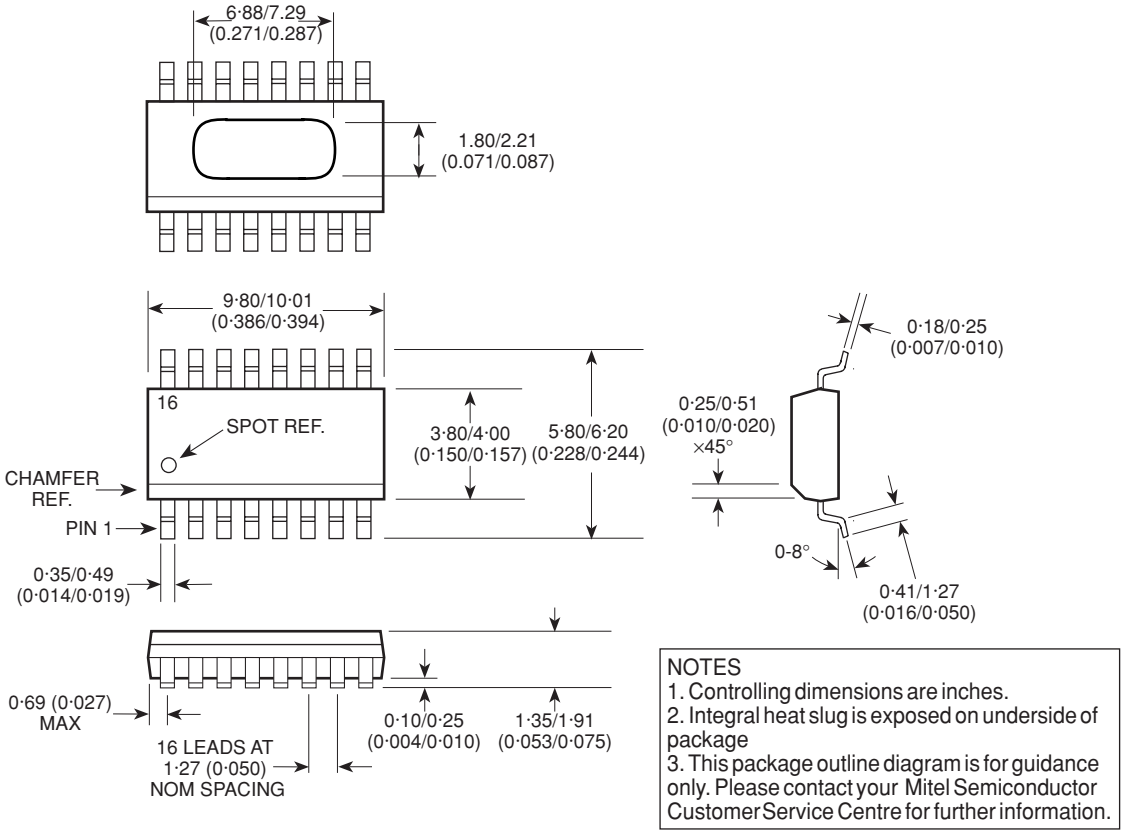
(b) There is no need to make a thermal connection between the package and the board. If such a connection is made using a thermal adhesive this will enhance the long term reliability of the product by reducing the junction temperature.

(c) The heatsink that is evident on the base of the package is solderable.

(d) There is no direct electrical connection between any of the device pins and the metal heatsinkslug. However if the heatsink is to be electrically connected to the PCB these connections should be confined to the ground plane.

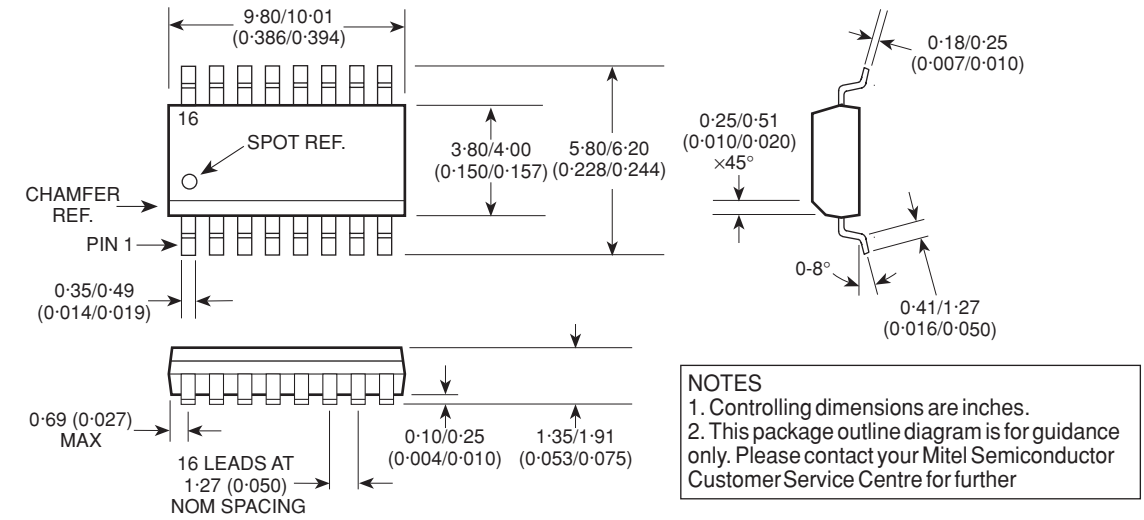
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. Integral heat slug is exposed on underside of package
3. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

16-LEAD MINIATURE HEAT SUNK PLASTIC DIL - MH16



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further

16-LEAD MINIATURE PLASTIC DIL - MP16

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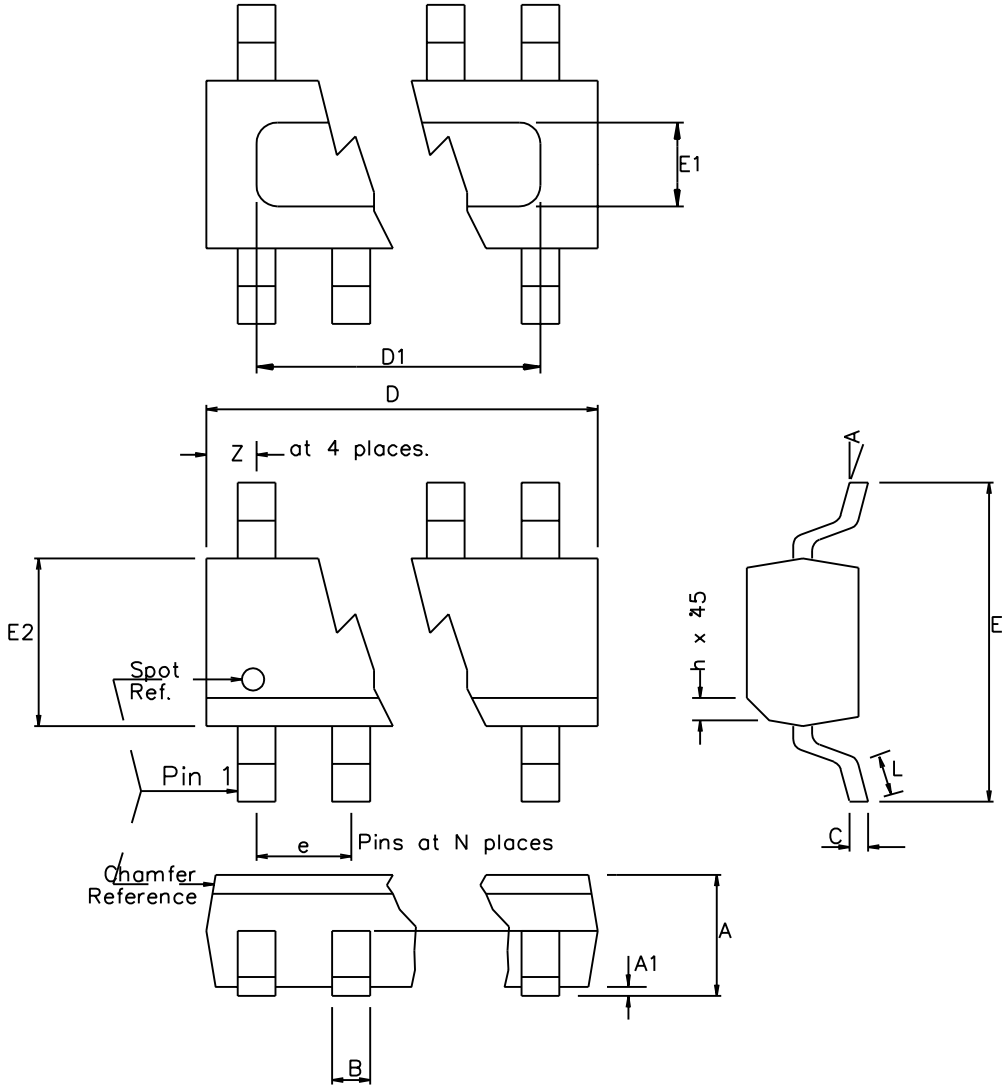


	Min mm	Max mm	Min Inches	Max Inches
A	1.35	1.91	0.053	0.075
A1	0.10	0.25	0.004	0.010
B	0.35	0.49	0.014	0.019
C	0.18	0.25	0.007	0.010
D	9.80	10.01	0.386	0.394
D1	6.88	7.29	0.271	0.287
E	5.80	6.20	0.228	0.244
E1	1.80	2.21	0.071	0.087
E2	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.51	0.010	0.020
L	0.41	1.27	0.016	0.050
Z		0.69		0.027
N	16		16	
A	0°	8°	0°	8°

Note: –
1. Dimensions D & E2 do not include mould flash or protrusions which shall not exceed 0.25mm (0.010") per side.
2. Heat sink to be flush with underside of package.
3. Maximum die thickness allowable is 0.015".
4. Formed leads shall be planar with respect to one another within 0.003 inches at seating plane.
5. Controlling dimension in inches.

ISSUE	1	2	3	
ACN	179387	201328	212433	
DATE	23Jun95	24Oct96	25Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

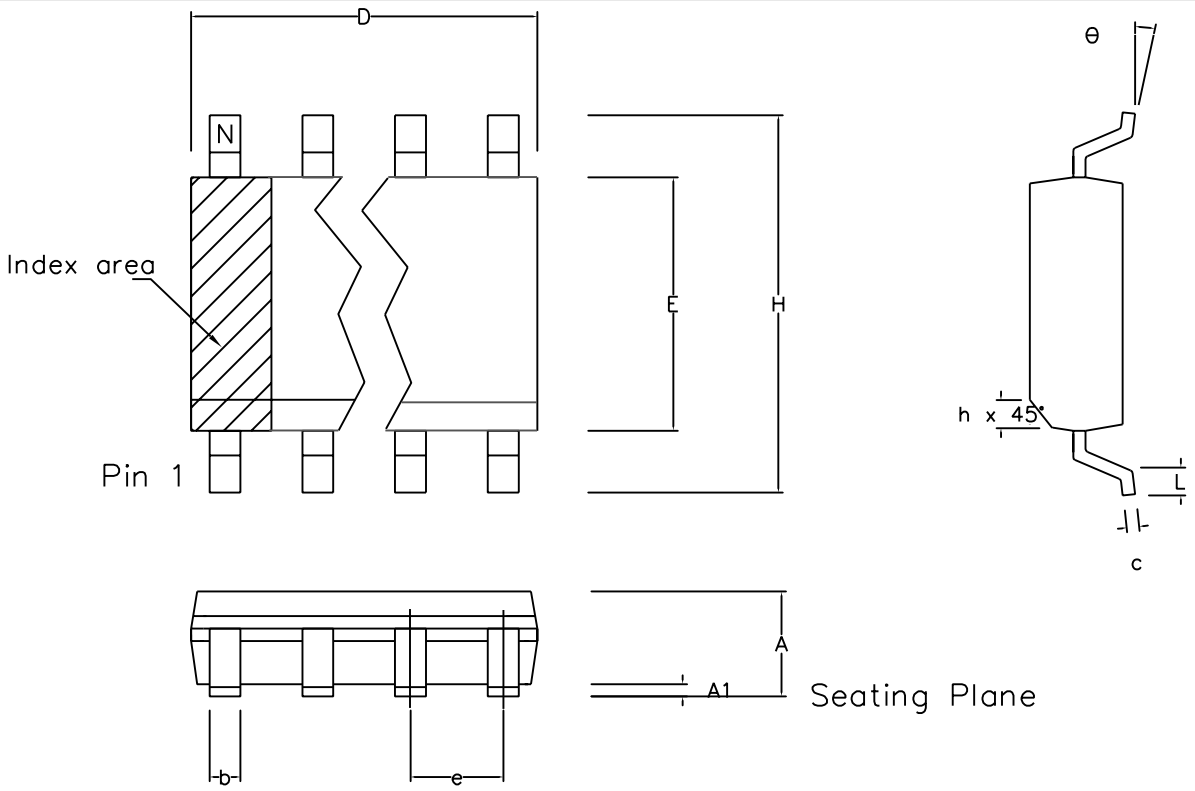
Previous package codes

MH / S

Package Code DC

Package Outline for
16 lead PSOP 11
(0.150" Body Width)

GPD00124



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201938	202597	203706	212431
DATE	7Apr95	27Feb97	12Jun97	9Dec97	25Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes
MP / S

Package Code DC

Package Outline for
16 lead SOIC
(0.150" Body Width)

GPD00012

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