LINEAR SYSTEMS

LS3550C
MONOLITHIC DUAL
PNP TRANSISTOR

micross

Linear Systems Monolithic Dual PNP Transistor

The LS3550C is a monolithic pair of PNP transistors mounted in a single SOIC package. The monolithic dual chip design reduces parasitics and gives better performance while ensuring extremely tight matching.

The 8 Pin SOIC provides ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS3550C Features:

- Tight matching
- Low Output Capacitance

FEATURES	
EXCELLENT THERMAL TRACKING	≤ 15µV/°C
TIGHT V_{BE} MATCHING	$\lvert V_{BE1} - V_{BE2} \rvert$ ≤10mV

ABSOLUTE MAXIMUM RATINGS [1]
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	-55°C to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	TBD
Maximum Currents	
Collector Current	10mA
Maximum Voltages	
Collector to Collector Voltage	80V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$\lvert V_{BE1} - V_{BE2} \rvert$	Base Emitter Voltage Differential	--	--	10	mV	I_C = -10mA, V_{CE} = -5V
$\Delta\lvert(V_{BE1} - V_{BE2})\rvert$ / ΔT	Base Emitter Voltage Differential Change with Temperature	--	--	15	µV/°C	I_C = -10mA, V_{CE} = -5V T_A = -40°C to +85°C
$\lvert I_{B1} - I_{B2} \rvert$	Base Current Differential	--	--	10	nA	I_C = -10µA, V_{CE} = -5V
$\lvert\Delta (I_{B1} - I_{B2})\rvert/\Delta T$	Base Current Differential Change with Temperature	--	--	1.0	nA/°C	I_C = -10µA, V_{CE} = -5V T_A = -40°C to +85°C
h_{FE1}/h_{FE2}	DC Current Gain Differential	--	--	15	%	I_C = 10µA, V_{CE} = 5V

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{CBO}	Collector to Base Voltage	-20	--	--	V	I_C = 10µA, I_E = 0
BV_{CEO}	Collector to Emitter Voltage	-20	--	--	V	I_C = 10µA, I_B = 0
BV_{EBO}	Emitter-Base Breakdown Voltage	-6.2	--	--	V	I_E = 10µA, I_C = 0 [2]
BV_{CCO}	Collector to Collector Voltage	-80	--	--	V	I_C = 10µA, I_E = 0
h_{FE}	DC Current Gain	50	--	--		I_C = -1mA, V_{CE} = -5V
		40	--	--		I_C = -10mA, V_{CE} = -5V
		40	--	--		I_C = -100mA, V_{CE} = -5V
V_{CE}(SAT)	Collector Saturation Voltage	--	--	-1.2	V	I_C = -100mA, I_B = -10mA
I_{EBO}	Emitter Cutoff Current	--	--	-0.2	nA	I_E = 0, V_{CB} = -3V
I_{CBO}	Collector Cutoff Current	--	--	-0.2	nA	I_E = 0, V_{CB} = -20V
C_{OBO}	Output Capacitance	--	--	2	pF	I_E = 0, V_{CB} = -10V
C_{C1C2}	Collector to Collector Capacitance	--	--	2	pF	V_{CC} = 0V
I_{C1C2}	Collector to Collector Leakage Current	--	--	-1	nA	V_{CC} = ±80V
f_T	Current Gain Bandwidth Product(Current)	--	--	600	MHz	I_C = -1mA, V_{CE} = -5V
NF	Narrow Band Noise Figure	--	--	3	dB	I_C = -100µA, V_{CE} = -5V, BW=200Hz, R_G= 10Ω, f = 1KHz

Notes:
1. Absolute Maximum ratings are limiting values above which serviceability may be impaired
2. The reverse base-to-emitter voltage must never exceed 6.2 volts; the reverse base-to-emitter current must never exceed 10µA.

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Available Packages:

LS3550C in SOIC
LS3550C available as bare die

Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx

SOIC (Top View)