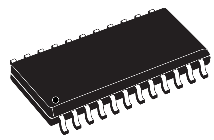
LIS3L02DS

INERTIAL SENSOR: 3Axis - 2g/6g DIGITAL OUTPUT LINEAR ACCELEROMETER

PRODUCT PREVIEW

- 2.7V TO 3.6V SINGLE SUPPLY OPERATION
- I2C/SPI DIGITAL OUTPUT INTERFACES
- MOTION ACTIVATED INTERRUPT SOURCE
- FACTORY TRIMMED DEVICE SENSITIVITY AND OFFSET
- EMBEDDED SELF TEST
- HIGH SHOCK SURVIVABILITY



SO-24
ORDERING NUMBER: LIS3L02DS

DESCRIPTION

The LIS3L02DS is a tri-axis digital output linear accelerometer that includes a sensing element and an IC interface able to take the information from the sensing element and to provide the measured acceleration signals to the external world through an I2C/SPI serial interface.

The sensing element, capable to detect the acceleration, is manufactured using a dedicated process called THELMA (Thick Epi-Poly Layer for Microactuators and Accelerometers) developed by ST to produce inertial sensors and actuators in silicon.

The IC interface instead is manufactured using a CMOS process that allows high level of integration to design a dedicated circuit which is factory trimmed to better match the sensing element characteristics.

The LIS3L02DS has a user selectable full scale of 2g, 6g and it is capable of measuring accelerations over a maximum bandwidth of 2.0 KHz for the X, Y axis and Z axis. The device bandwidth may be programmed accordingly to the application requirements. A self-test capability allows the user to check the functioning of the system.

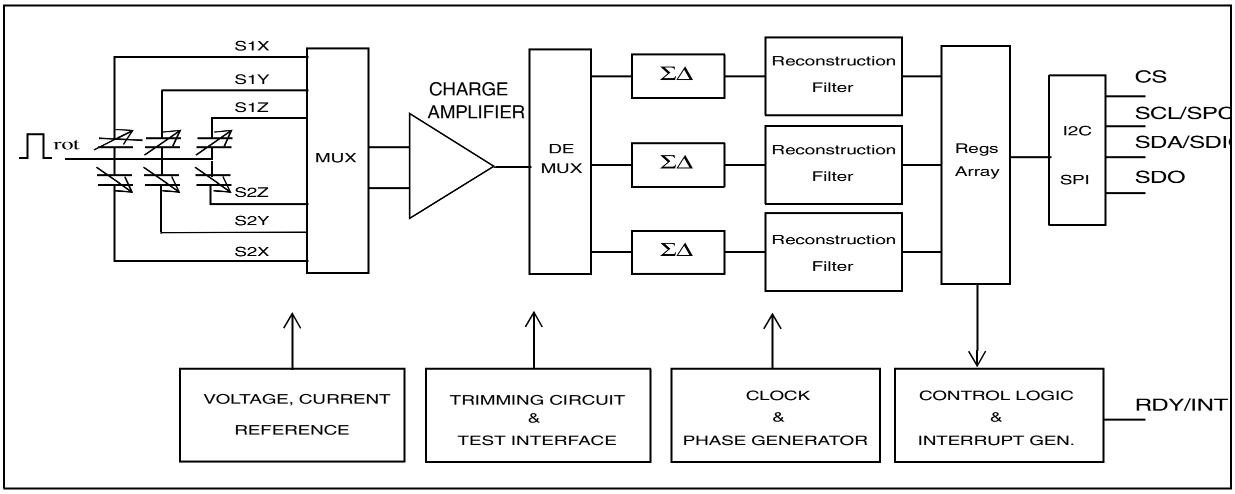
The device may be configured to generate an inertial wake-up/interrupt signal when a programmable acceleration threshold is exceeded along one of the three axis.

The LIS3L02DS is available in plastic SMD package and it is specified over a temperature range extending from -40°C to +85°C.

The LIS3L02DS belongs to a family of products suitable for a variety of applications:

– Antitheft systems and Inertial navigation
– Virtual reality input devices
– Vibration Monitoring, recording and compensation
– Robotics and Appliance control

BLOCK DIAGRAM

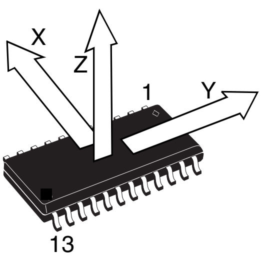


This is preliminary information on a new product now in development. Details are subject to change without notice.

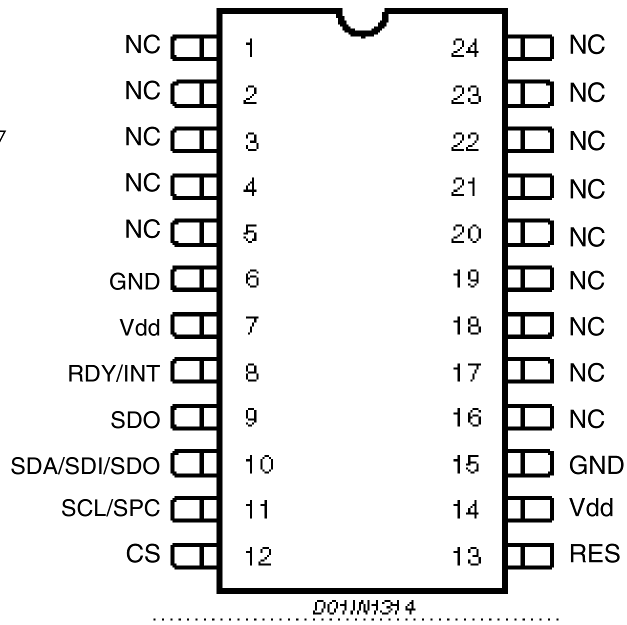
PIN DESCRIPTION

N°	Pin	Function
1 to 5	NC	Internally not connected
6	GND	0V supply
7	Vdd	Power supply
8	RDY/INT	Data ready/inertial wake-up interrupt
9	SDO	SPI Serial Data Output
10	SDA/ SDI/ SDO	I2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
11	SCL/SPC	I2C Serial Clock (SCL) SPI Serial Port Slock (SPC)
12	CS	SPI enable I2C/SPI mode selection (1: I2C mode; 0: SPI enabled)
13	RES	Reserved. Either leave unconnected or connect to Vdd
14	Vdd	Power supply
15	GND	0V supply
16 to 24	NC	Internally not connected

PIN CONNECTION (Top view)



DIRECTION OF THE DETECTABLE ACCELERATIONS



ELECTRICAL CHARACTERISTCS (Temperature range -40°C to +85°C)

All the parameters are specified @ Vdd=3.3V and T=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.7		3.6	V
Idd	Supply current	T = 25°C		1	1.5	mA
IddPdn	Current consumption in power-down mode	T = 25°C			10	µA
BW	Digital Filter Cut-Off frequency (-3dB)			70	1150	Hz
FS	Measurement range[2]	FS bit set to 0		±2.0		g
		FS bit set to 1		±6.0		g
FSAcc	Full-scale accuracy	T = 25°C Full-scale = 2g	FS-10%	FS	FS+10%	g
		T = 25°C Full-scale = 6g	FS-15%	FS	FS+15%	g
So	Device Resolution	T = 25°C Full-scale = 2g BW=56Hz		1		mg
0g-Offset	Zero g level	T = 25°C Full-scale = 2g	-50		50	mg
NL	Non Linearity	Best fit straight line X, Y axis Full-scale = 2g BW=56Hz		±1		% FS
		Best fit straight line Z axis Full-scale = 2g BW=56Hz		±3		% FS
DR1	Output data rate	Dec factor = 128		280		Hz
DR2	Output data rate	Dec factor = 64		560		Hz
DR3	Output data rate	Dec factor = 32		1120		Hz
DR4	Output data rate	Dec factor = 8		4480		Hz
Ton	Turn-on time			50		ms

Notes

[1] Typical specifications are not guaranteed

[2] Guaranteed by wafer level test and measurement of initial offset and sensitivity

ABSOLUTE MAXIMUM RATING

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Maximum Value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO, RDY/INT)	Vss -0.3 to Vdd +0.3	V
A_{POW}	Acceleration (Any axis, Powered, Vdd=3.3V)	3000g for 0.5 ms	
A_{UNP}	Acceleration (Any axis, Unpowered)	3000g for 0.5 ms	
T_{OP}	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-40 to +105	°C

1 FUNCTIONALITY

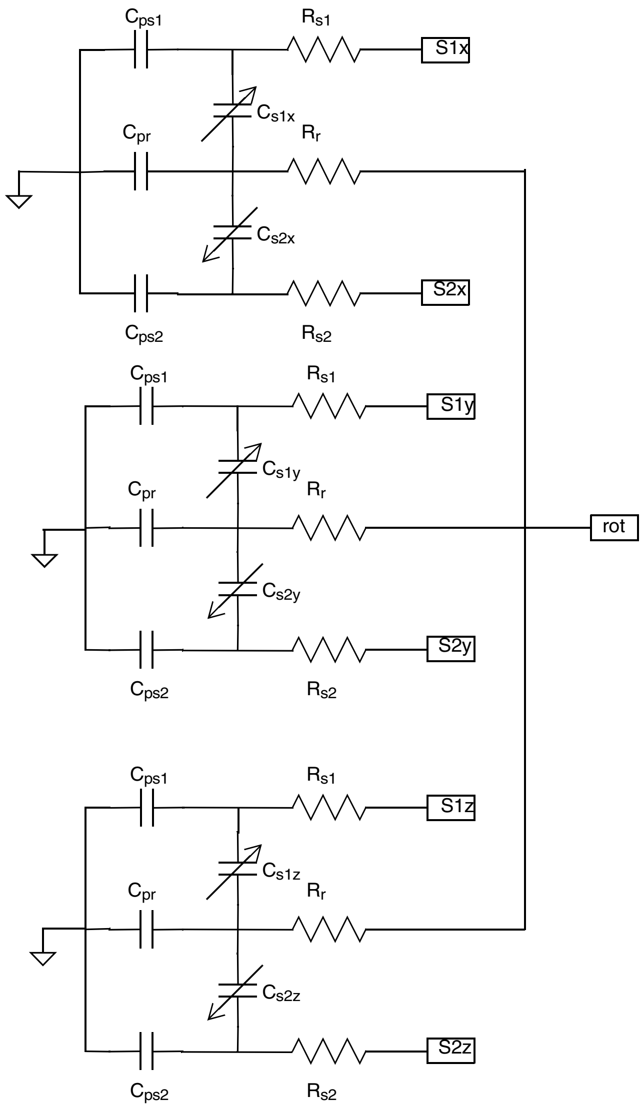
1.1 Sensing element

The THELMA process is utilized to create a surface micro-machined accelerometer. The technology allows to carry out suspended silicon structures which are attached to the substrate in a few points called anchors and free to move on a plane parallel to the substrate itself. To be compatible with the traditional packaging techniques a cap is placed on top of the sensing element to avoid blocking the moving parts during the molding phase.

The equivalent circuit for the sensing element is shown in the below figure; when a linear acceleration is applied, the proof mass displaces from its nominal position, causing an imbalance in the capacitive half-bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the sense capacitor.

The nominal value of the capacitors, at steady state, is few pF and when an acceleration is applied the maximum variation of the capacitive load is few tenth of pF.

Figure 1. Equivalent electrical circuit



1.2 IC Interface

The complete measurement chain is composed by a low-noise capacitive amplifier which converts into an analog voltage the capacitive unbalancing of the MEMS sensor and by three ΣΔ analog-to-digital converters, one for each axis, that translates the produced signal into a digital bitstream.

The ΣΔ converters are tigthly coupled with dedicated reconstruction filters which removes the high frequency components of the quantization noise and provides low rate and high resolution digital words.

The charge amplifier and the ΣΔ converters are operated respectively at 107.5 KHz and 35.8 KHz.

The data rate at the output of the reconstruction depends on the user selected Decimation Factor (DF) and span from 280 Hz to 4.48 KHz.

The acceleration data may be accessed through an I2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The LIS3L02DS features a Data-Ready signal (DRY) which indicated when a new set of measured acceleration data is available thus simplifying data synchronization in digital system employing the device itself.

The LIS3L02DS may also be configured to generate an inertial wake-up/interrupt signal when a programmable acceleration threshold is exceeded along one of the three axis.

1.3 Factory calibration

The IC interface is factory calibrated to provide to the final user a device ready to operate. The parameters which are trimmed are: gain, offset, common mode and internal clock frequency.

The trimming values are stored inside the device by a non volatile structure. Any time the device is turned on, the trimming parameters are downloaded into the registers to be employed during the normal operation thus allowing the final user to employ the device without any need for further calibration

2 DIGITAL INTERFACES

The registes embedded inside the LIS3L02DS may be accessed through both the 2C and SPI serial interfaces. The latter may be SW configured to operate either in SPI mode or in 3-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I2C interface, CS line must be tied high (i.e connected to Vdd).

Table 1. Serial Interface Pin Description

PIN Name	PIN Description
CS	SPI enable I2C/SPI mode selection (1: I2C mode; 0: SPI enabled)
SCL/SPC	I2C Serial Clock (SCL) SPI Serial Port Slock (SPC)
SDA/SDI/SDO	I2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO	SPI Serial Data Output (SDO)

2.1 I2C Serial Interface

The LIS3L02DS I2C is a bus slave. The I2C is employed to write the data into the registers whose content can also be read back.

The relevant I^2C terminology is given in the table below

Table 2. Serial Interface Pin Description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the Serial Clock Line (SCL) and the Serial DAta liine (SDA). The latter is a bidirectional line used for sending and receiving the data to/form the interface. Both the lines are connected to Vdd through a pull-up resistor embedded inside the LIS3L02DS. When the bus is free both the lines are high.

2.1.1 I^2C Operation

The transaction on the bus is started through a START signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with it's address. If they match, the device considers itself addressed by the Master. The address can be made up of a programmable part and a fixed part, thus allowing more than one device of the same type to be connected to the I^2C bus.

The Slave ADdress (SAD) associated to the LIS3L02DS is 0011101.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received.

The I^2C embedded inside the Gengine ASIC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a salve address is sent, once a slave acknowledge has been returned, a 8-bit sub-address will be transmitted: the 7 LSB represent the actual register address while the MSB enables address autoincrement. If the MSB of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

If the LSB of the slave address was '1' (read), a repeated START condition will have to be issued after the two sub-address bytes; if the LSB is '0' (write) the Master will transmit to the slave with direction unchanged.

Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Transfer when Master is writing multiple bytes to slave:

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Transfer when Master is receiving (reading) one byte of data from slave:

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			MAK
Slave			SAK		SAK			SAK	DATA	

Master	SR		MAK		NMAK	SP
Slave		DATA		DATA		

Data are transmitted in byte format. Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant Bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to read.

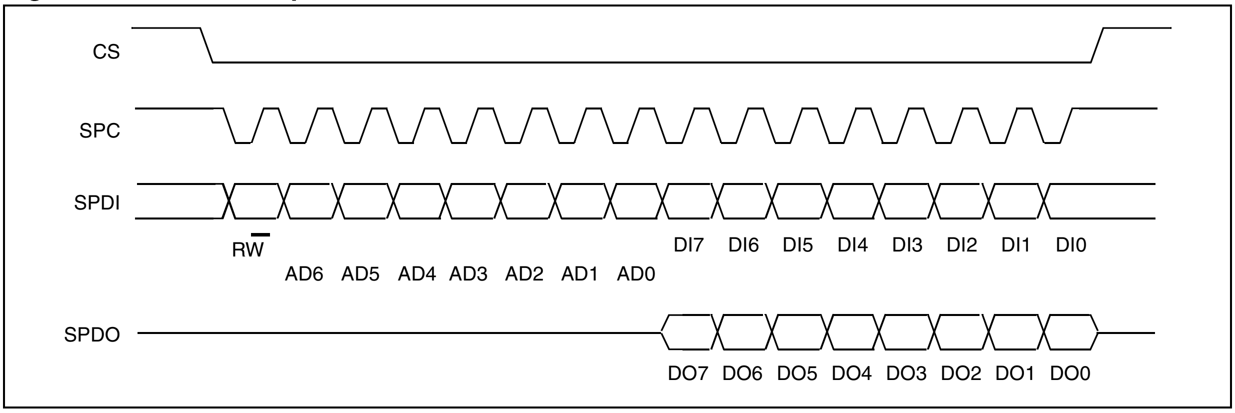
2.2 SPI Bus Interface

The Gengine SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: CS, SPC, SPDI and SPDO.

2.2.1 Read & Write registers

Figure 2. Read & write protocol



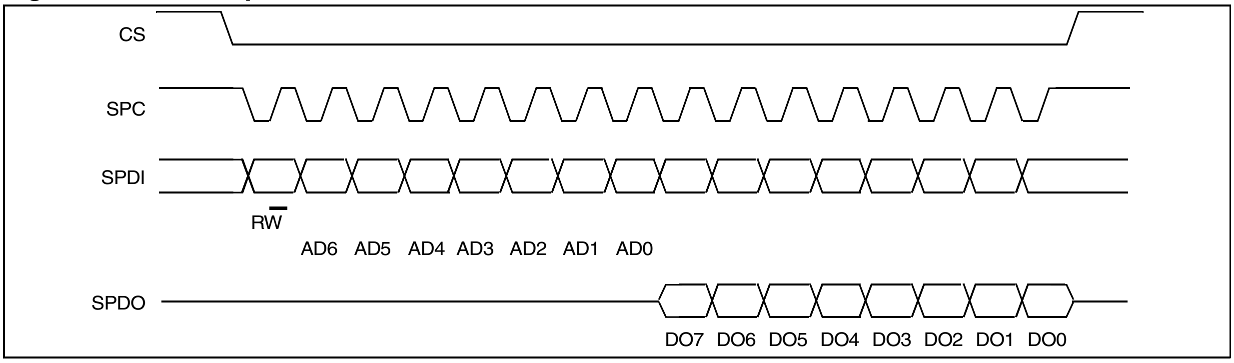
CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. SPC is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when CS is high (no transmission). SPDI and SPDO are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of SPC and should be captured at the rising edge of SPC.

Both the Read Register and Write Register commands are completed in 16 clocks pulses. Bit duration is the time between two falling edges of SPC. The first bit (bit 0) starts at the first falling edge of SPC after the falling edge of CS while the last bit (bit 15) starts at the last falling edge of SPC just before the rising edge of CS.

- bit 0: RW bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive SPDO at the start of bit 8.
- bit 1-7: address AD(6:0). This is the address field of the indexed register.
- bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).
- bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

2.2.2 SPI Read

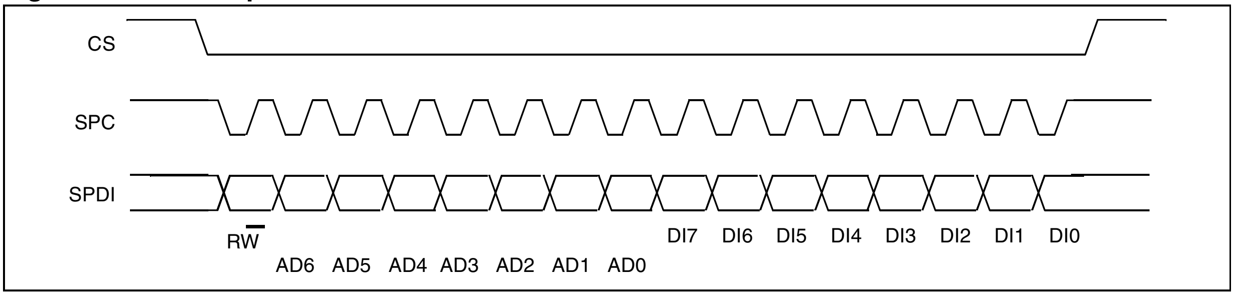
Figure 3. SPI Read protocol



The SPI Read command consists is performed with 16 clocks pulses:
- bit 0: READ bit. The value is 1.
- bit 1-7: address AD(6:0). This is the address field of the indexed register.
- bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

2.2.3 SPI Write

Figure 4. SPI Write protocol

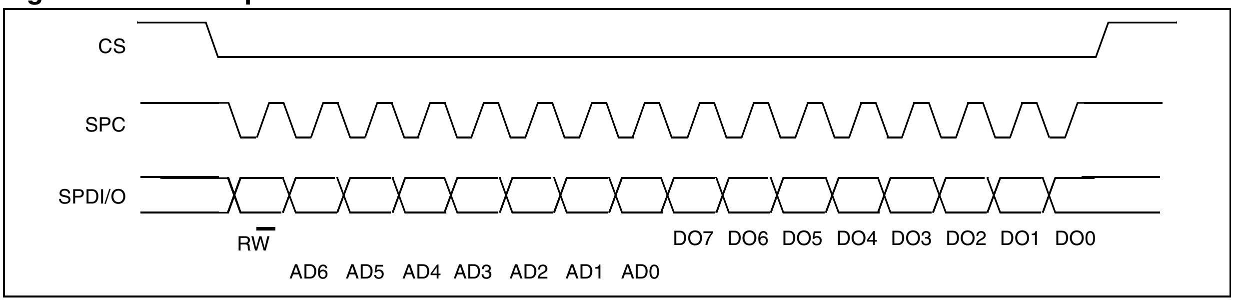


The SPI Write command consists is performed with 16 clocks pulses.
- bit 0: WRITE bit. The value is 0.
- bit 1-7: address AD(3:0). This is the address field of the indexed register.
- bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

2.2.4 SPI Read in 3-wires mode

3-wires mode is entered by setting to 1 bit SIM (SPI Serial Interface Mode selection) in A_IF_CTRL2.

Figure 5. SPI Read protocol in 3-wires model



The SPI Read command consists is performed with 16 clocks pulses:
- bit 0: READ bit. The value is 1.
- bit 1-7: address AD(6:0). This is the address field of the indexed register.
- bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

3 REGISTERS MAPPING

The table given below provides a listing of the registers embedded in the device and the related address.

All the “application related” registers (i.e. control, status, data) are mapped into Bank2 so to simplify their access when running through the SPI interface.

Table 3. Registers address map

Reg. Name	Type	Register Address		Size (Bit)	Comment
		Binary	Hex		
		0000000 - 0010101	00 - 15		Reserved
OFFSET_X	rw	0010110	16	8	Loaded at boot
OFFSET_Y	rw	0010111	17	8	Loaded at boot
OFFSET_Z	rw	0011000	18	8	Loaded at boot
GAIN_X	rw	0011001	19	8	Loaded at boot
GAIN_Y	rw	0011010	1A	8	Loaded at boot
GAIN_Z	rw	0011011	1B	8	Loaded at boot
		0011100 - 0011111	1C - 1F		Reserved
CTRL_REG1	rw	0100000	20	8	
CTRL_REG2	rw	0100001	21	8	
		0100010	22		Reserved
WAKE_UP_CFG	rw	0100011	23	8	
WAKE_UP_SRC	r	0100100	24	8	
WAKE_UP_ACK	r	0100101	25	8	
		0100110	26		Reserved
STATUS_REG	rw	0100111	27	8	
OUTX_L	r	0101000	28	8	
OUTX_H	r	0101001	29	8	
OUTY_L	r	0101010	2A	8	
OUTY_H	r	0101011	2B	8	
OUTZ_L	r	0101100	2C	8	
OUTZ_H	r	0101101	2D	8	
THS_L	rw	0101110	2E	8	
THS_H	rw	0101111	2F	8	
		0110000 - 1111111	30 - 3F		Reserved

4 REGISTERS DESCRIPTION

The device contains a set of registers which are used to control its behavior and to retrieve acceleration data.

4.1 OFFSET_X (16h)

OX7	OX6	OX5	OX4	OX3	OX2	OX1	OX0

OX7, OX0	Digital Offset Trimming for X-Axis

4.2 OFFSET_Y (17h)

OY7	OY6	OY5	OY4	OY3	OY2	OY1	OY0

DOY7, DOY0	Digital Offset Trimming for Y-Axis

4.3 OFFSET_Z (18h)

OZ7	OZ6	OZ5	OZ4	OZ3	OZ2	OZ1	OZ0

OZ7, OZ0	Digital Offset Trimming for Z-Axis

4.4 GAIN_X (19h)

GX7	GX6	GX5	GX4	GX3	GX2	GX1	GX0

GX7, GX0	Digital Gain Trimming for X-Axis

4.5 GAIN_Y (1Ah)

GY7	GY6	GY5	GY4	GY3	GY2	GY1	GY0

GY7, GY0	Digital Gain Trimming for Y-Axis

4.6 GAIN_Z (1Bh)

GZ7	GZ6	GZ5	GZ4	GZ3	GZ2	GZ1	GZ0

GZ7, GZ0	Digital Gain Trimming for Z-Axis

4.7 A_IF_CTRL1 (20h)

PD1	PD0	DF1	DF0	ST	Zen	Yen	Xen

PD1, PD0	Power Down Control (00: power-down mode; 01: device on)
DF1, DF0	Decimation Factor Control (00: decimate by 128; 01: decimate by 64; 10: decimate by 32; 11: decimate by 8)
ST	Self Test Enable (0: normal mode; 1: self-test active)
Zen	Z-axis enable (0: axis off; 1: axis on)
Yen	Y-axis enable (0: axis off; 1: axis on)
Xen	X-axis enable (0: axis off; 1: axis on)

4.8 A_IF_CTRL2 (21h)

FS	x	x	BOOT	IEN	DRDY	SIM	DAS

FS	Full Scale selection (0: +/- 2g; 1: +/- 6g)
BOOT	Reboot memory content
IEN	Interrupt ENable (0: data ready on RDY pad; 1: int req on RDY pad)
DRDY	Enable Data-Ready generation
SIM	SPI Serial Interface Mode selection (0: 4-wire interface; 1: 3-wire interface)
DAS	Data Alignement Selection (0: 12 bit right justified; 1: 16 bit left justified)

4.9 WAKE_UP_CFG (23h)

x	LIR	MZH	MZL	MYH	MYL	MXH	MXL

LIR	Latch interrupt request (1: interrupt request latched)
MZH	Mask Z High Interrupt (1: enable int req on measured accel. value higher than preset threshold)
MZL	Mask Z Low Interrupt (1: enable int req on measured accel. value lower than preset threshold)
MYH	Mask Y High Interrupt (1: enable int req on measured accel. value higher than preset threshold)
MYL	Mask Y Low Interrupt (1: enable int req on measured accel. value lower than preset threshold)
MXH	Mask X High Interrupt (1: enable int req on measured accel. value higher than preset threshold)
MXL	Mask X Low Interrupt (1: enable int req on measured accel. value lower than preset threshold)

4.10 WAKE_UP_SOURCE (24h)

x	IA	ZH	ZL	YH	YL	XH	XL

IA	Interrupt Active
MZH	Z High
MZL	Z Low
MYH	Y High
MYL	Y Low
MXH	X High
MXL	X Low

4.11 WAKE_UP_ACK (25h)

Reading at this address resets the **WAKE_UP_SOURCE** register.

4.12 A_IF_STATUS (27h)

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

ZYXOR	X, Y and Z axis Data Overrun
ZOR	Z axis Data Overrun
YOR	Y axis Data Overrun
XOR	Y axis Data Overrun
ZYXDA	X, Y and Z axis new Data Available
ZDA	Z axis new Data Available
YDA	Y axis new Data Available
XDA	X axis new Data Available

4.13 OUTX_L (28h)

XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0

XD7, XD0	X axis acceleration data LSb

4.14 OUTX_H (29h)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. XD15-XD12=XD11, XD11, XD11, XD11).

XD15	XD14	XD13	XD12	XD11	XD10	XD9	XD8

XD15, XD8	X axis acceleration data MSb

4.15 OUTY_L (2Ah)

YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0

YD7, YD0	Y axis acceleration data LSb

4.16 OUTY_H (2Bh)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. YD15-YD12=YD11, YD11, YD11, YD11).

YD15	YD14	YD13	YD12	YD11	YD10	YD9	YD8

YD15, YD8	Y axis acceleration data MSb

4.17 OUTZ_L (2Ch)

ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0

ZD7, ZD0	Z axis acceleration data LSb

4.18 OUTZ_H (2Dh)

When reading the register in “12 bit right justified” mode the most significant bits (7:4) are replaced with bit 3 (i.e. ZD15-ZD12=ZD11, ZD11, ZD11, ZD11).

ZD15	ZD14	ZD13	ZD12	ZD11	ZD10	ZD9	ZD8

ZD15, ZD8	Z axis acceleration data MSb

4.19 THS_L (2Eh)

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS15, THS8	Inertial Wake Up Acceleration Threshold Lsb

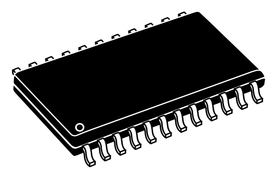
4.20 THS_H (2Fh)

THS15	THS14	THS13	THS12	THS11	THS10	THS9	THS8

THS15, THS8	Inertial Wake Up Acceleration Threshold Msb

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
A2			2.55			0.100
B	0.33		0.51	0.013		0.0200
C	0.23		0.32	0.009		0.013
D	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0,050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
k	0° (min.), 8° (max.)					
L	0.40		1.27	0.016		0.050

OUTLINE AND MECHANICAL DATA



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