Preliminary

Notice: This is not a final specification.
Some parametric limits are subject to change.

M6MGB/T641S8BKT

67,108,864-BIT (4,194,304-WORD BY 16-BIT / 8,388,608-WORD BY 8-BIT) CMOS FLASH MEMORY &

8,388,608-BIT (524,288-WORD BY 16-BIT / 1,048,576-WORD BY 8BIT) CMOS SRAM

Stacked- mMCP (micro Multi Chip Package)

DESCRIPTION

The M6MGB/T641S8BKT is a Stacked micro Multi Chip Package (S- μ MCP) that contents 64M-bit Flash memory and 8M-bit Static RAM and are available in a 52-pin TSOP for lead free use.

64M-bit Flash memory is a 4,194,304 words / 8,388,608 bytes single power supply and high performance non-volatile memory fabricated by CMOS technology for the peripheral circuit and DINOR IV (Divided bit-line NOR IV) architecture for the memory cell. All memory blocks are locked and can not be programmed or erased, when F-WP# is Low. Using Software Lock Release function, program or erase operation can be executed.

8M-bit SRAM is a 524,288 words / 1,048576 bytes asynchronous SRAM fabricated by CMOS technology for the peripheral circuit and CMOS type transistor for the memory cell.

The M6MGB/T641S8BKT is suitable for a high performance cellular phone and a mobile PC that are required to be small mounting area, weight and small power dissipation.

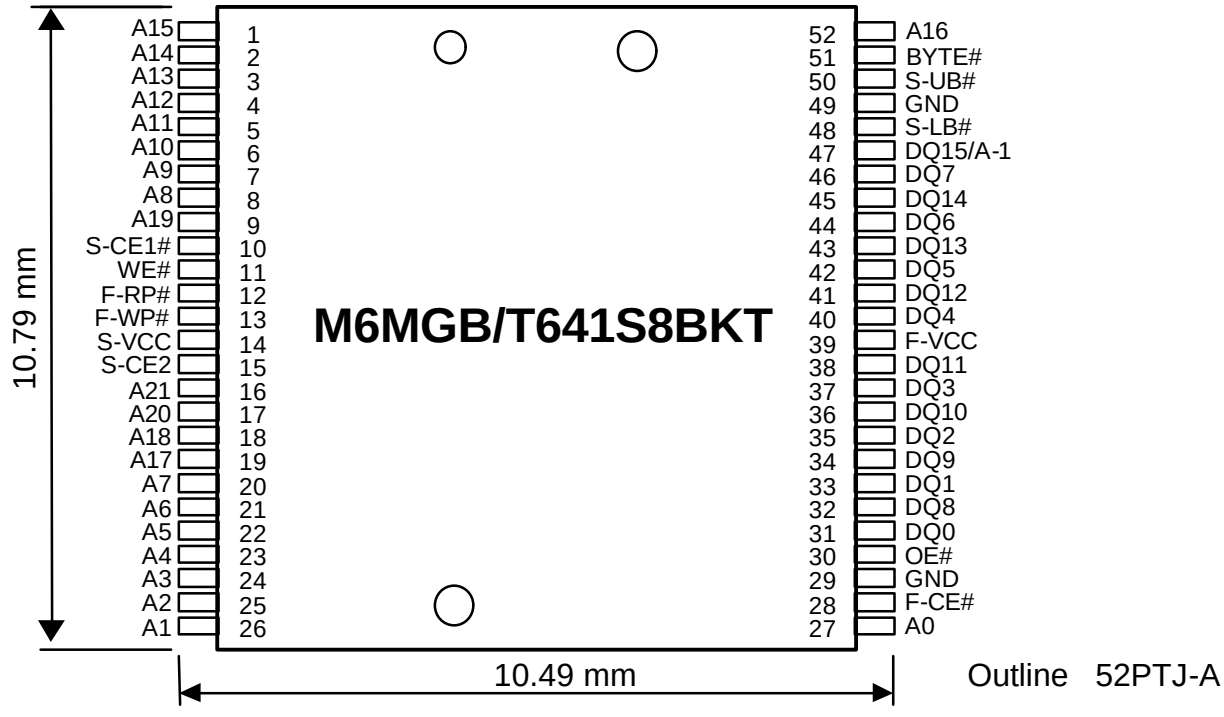
FEATURES

Access time	Flash	70ns (Max.)
	SRAM	85ns (Max.)
Supply voltage		VCC = 2.7 ~ 3.0V
Ambient temperature		Ta=-40 ~ 85 °C
Package		52pin TSOP(Type-II), Lead pitch 0.4mm
		Outer-lead finishing : Sn-Cu

APPLICATION

Mobile communication products

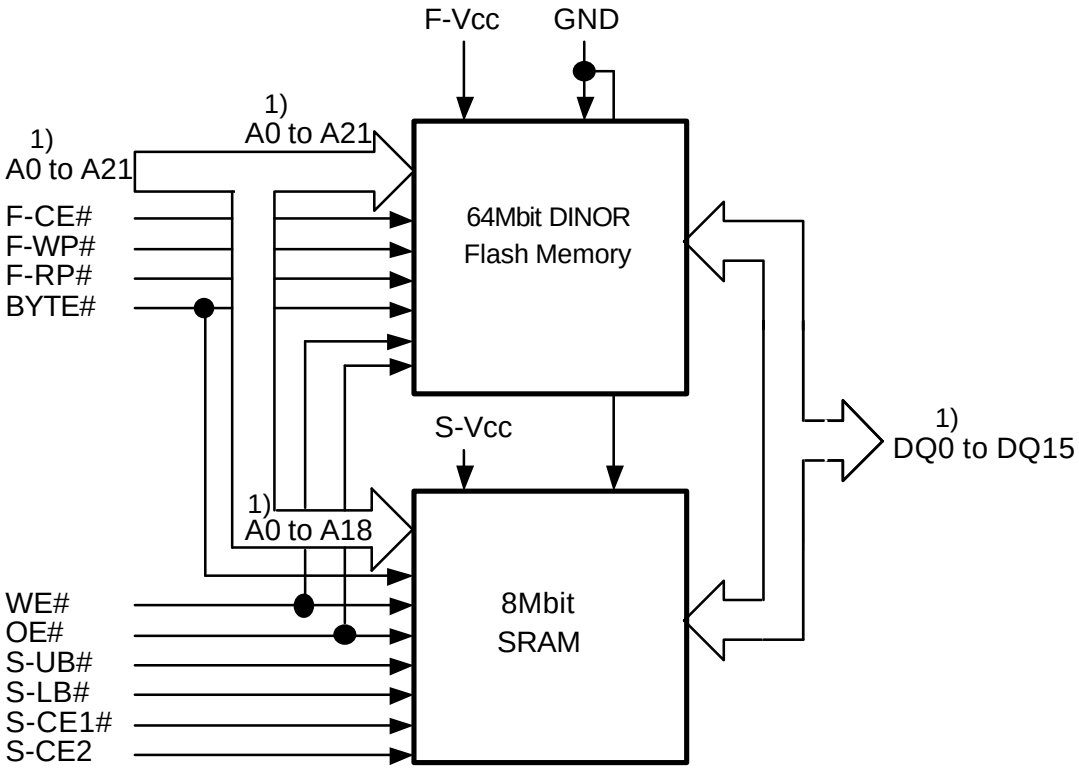
PIN CONFIGURATION (TOP VIEW)



Outline 52PTJ-A

F-VCC	:Vcc for Flash
S-VCC	:Vcc for SRAM
GND	:GND for Flash/SRAM
A-1-A18	:Flash/SRAM common Address
A19-A21	:Address for Flash
DQ0-DQ15	:Data I/O
F-CE#	:Flash Chip Enable
S-CE#,S-CE2	:SRAM Chip Enable
OE#	:Flash/SRAM Output Enable
WE#	:Flash/SRAM Write Enable
F-WP#	:Flash Write Protect
F-RP#	:Flash Reset Power Down
BYTE#	:Flash/SRAM Byte Enable
S-LB#	:SRAM Lower Byte
S-UB#	:SRAM Upper Byte

MCP Block Diagram



Note 1): In case of x8 organization, A-1 is added, and only Lower Byte data(DQ0 to DQ7) are assigned to I/O and Upper Byte data(DQ8 to DQ15) are High-Z.
Note 2): In the data sheet there are "VCC"s which mean "F-VCC" or "S-VCC". In the SRAM part there are "UB#" and "LB#" which mean "S-UB#" and "S-UB#", respectively.

Capacitance

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
CIN	Input capacitance	A21-A0, OE#, WE#, F-CE#, BYTE#, F-RP#, F-WP#, S-CE1#, S-CE2, S-UB#, S-LB#	Ta=25°C, f=1MHz, Vin=Vout=0V			18	pF
COUT	Output Capacitance	DQ15-DQ0				22	pF

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Renesas LSIs

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