EL711DI
1A Fast Transient DC-DC Buck Converter With Integrated Silicon Magnetics

Description

The EL711DI is the first of a brand new Linear Direct Replacement (LDR™) buck regulator family designed for the economical replacement of Low Drop-Out (LDO) linear voltage regulators. The EL711DI is a 1000mA Power System-on-Chip, (PowerSoC) switch-mode DC-DC regulator with integrates MOSFETs, controller, compensation circuit and a proprietary on-chip silicon inductor. Utilizing a 3x4.5x0.9mm DFN package, the EL711DI offers high efficiency at an excellent solution size and is a cost-effective alternative to LDOs. With an 18MHz switching frequency, the EL711DI is the fastest in-class buck regulator with the lowest output ripple. Due to its all-silicon PowerSoC construction, the EL711DI also offers superior reliability over standard discrete DCDC solutions.

The EL711DI showcases Enpirion's proprietary monolithic magnetics-on-silicon inductor technology and is designed to meet the demand of high performance digital ASICs, DSPs, and FPGAs found in servers, routers, switches, and base stations. Enpirion's PowerSoC solution improves system design and productivity by offering simple board layout, small solution size, low cost, high efficiency, ultra-fast transient response and high performance.

Features

- Output Current up to 1000mA
- High Efficiency
- 3 x 4.5 x 0.9 mm DFN package
- Ultra-Fast Transient Response
- 2% Initial Output Voltage Accuracy
- Input Voltage Range: 2.7V to 5.5V
- Output Voltage Range 0.6V to $V_{IN} – V_{DO}$
- 18MHz Switching Frequency for Ultra Low Ripple (8mVpp)
- 100% IC-level Reliability in a PowerSoC Solution
- Short-Circuit, UVLO and Thermal Protection
- RoHS compliant, MSL level 3, 260 °C reflow

Applications

- Voltage Rails Using LDO with Thermal Issues
- Cost-Effective Compliance Energy Star Initiative
- High Density Applications with Limited LDO Footprint
- Very Low Noise and Noise Sensitive Applications
- CPU, GPU, DSP, FPGA or Memory Core Voltage

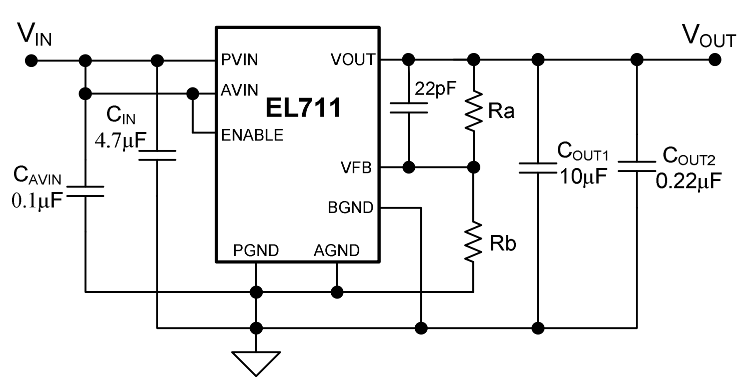


Figure 1. Simplified Applications Circuit

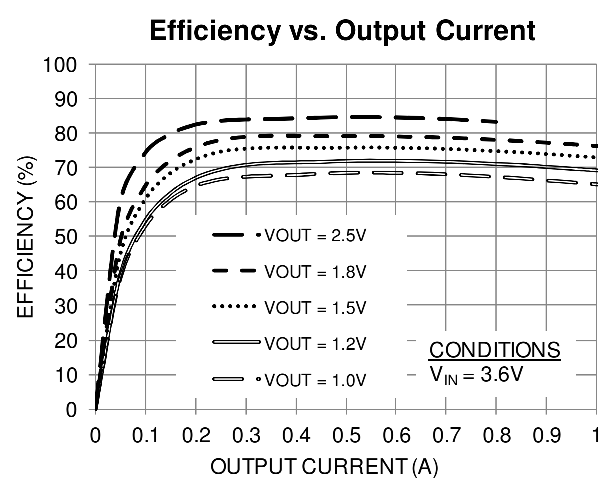


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (℃)	Package Description
EL711DI	L711	-40 to +85	16-pin (3.0mm x 4.5mm x 0.9mm) DFN T&R
EL711DI-E	L711	DFN Evaluation Board	

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

Pin Assignments (Top View)

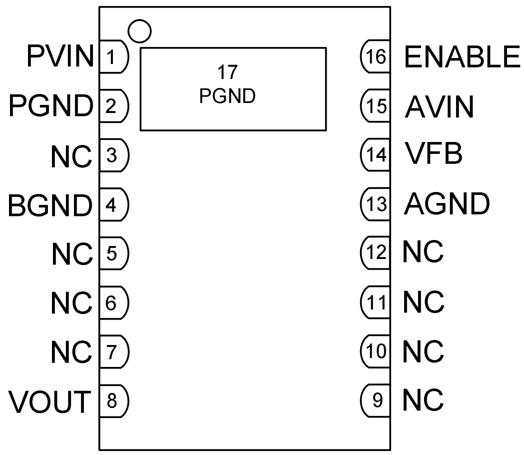


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White ‘dot’ on top left is pin 1 indicator on top of the device package.

Pin Description

PIN	NAME	FUNCTION
1	PVIN	Input power supply. Connect to input power supply and place input filter capacitor(s) between this pin and the PGND pin. Refer to Layout Recommendations section for details.
2	PGND	Power ground. Connect this pin to the ground electrode of the output filter capacitor(s).
4	BGND	Connect to GND plane at all times.
8	VOUT	Regulated converter output. Connect to the load and place output filter capacitor(s) between this pin and the PGND pin. Refer to Layout Recommendations section for details.
13	AGND	Analog ground. This is the quiet ground for the internal control circuits and the ground return for external feedback voltage divider.
14	VFB	This is the external feedback input pin. A resistor divider connects from the output to AGND. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) is required parallel to the upper feedback resistor (R_A). The output voltage regulation is based on the VFB node voltage equal to 0.6V.
15	AVIN	Analog input voltage for the control circuits. Connect this pin to the input power supply (PVIN) at a quiet point.
16	ENABLE	Device enable pin. A high level or floating this pin enables the device while a low level disables the device. A voltage ramp from another power converter may be applied for precision enable. Refer to Power Up Sequencing.
3, 5, 6,7, 9, 10, 11, 12	NC	NO CONNECT: These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
17	PGND	Not a perimeter pin. Device thermal pad to be connected to the ground electrode of the input filter capacitor(s) with a wide trace. From that point, vias conduct heat to the system GND plane. Refer to Layout Recommendation section.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage: PVIN, AVIN, VOUT	V_{IN}	-0.3	6.0	V
Voltages on: ENABLE		-0.3	V_{IN}+ 0.3	V
Voltages on: V_{FB}		-0.3	2.7	V
Maximum Operating Junction Temperature	T_{J-ABS}		150	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020C			260	℃
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (Charge Device Model)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.7	5.5	V
Output Voltage Range (Note 1)	V_{OUT}	0.6	V_{IN}-V_{DO}	V
Operating Ambient Temperature	T_A	-40	+85	℃
Operating Junction Temperature	T_J	-40	+125	℃

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (Note 2)	θ_{JA}	60	℃/W
Thermal Overload Trip Point	T_{J-TP}	+155	℃
Thermal Overload Trip Point Hysteresis		15	℃

Note 1: V_{DO} (dropout voltage) is defined as (I_{LOAD} x Max Dropout Resistance) / 0.375. Maximum V_{OUT} = V_{IN} - V_{DO}. Low V_{IN} operation beyond the dropout region is not guaranteed. Please refer to Electrical Characteristics Table and Typical Performance Curves.

Note 2: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

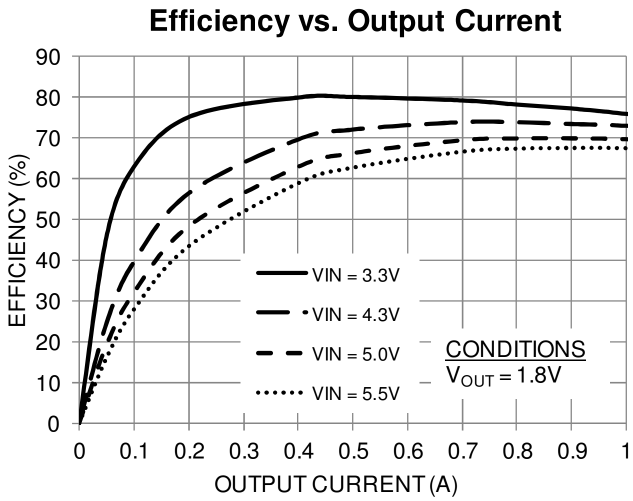
NOTE: V_{IN}=5.5V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

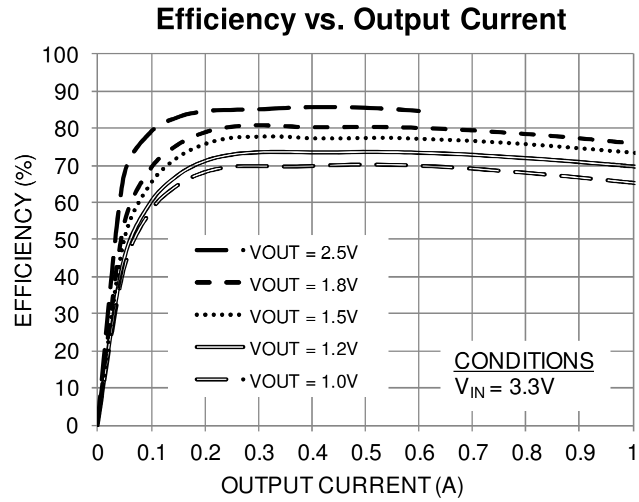
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage Range	V_{IN}		2.7		5.5	V
Under Voltage Lock-out – V_{IN} Rising	V_{UVLO_R}		2.35	2.5	2.65	V
Under Voltage Lock-out – V_{IN} Falling	V_{UVLO_F}		2.2	2.35	2.5	V
Drop Out Resistance	R_{DO}	Input to Output Resistance		340	500	mΩ
VFB Voltage Initial Accuracy	V_{FB}	T_A = 25°C	0.588	0.600	0.612	V
Operating Output Voltage Range	V_{OUT}	Note 1	0.6		V_{IN}-V_{DO}	V
Line Regulation	ΔV_{OUT_LINE}	2.7V ≤ V_{IN} ≤ 5.5V		0.2		%/V
Load Regulation	ΔV_{OUT_LOAD}	0A ≤ I_{LOAD} ≤ 1A		0.2		%/A
Temperature Variation	ΔV_{OUT_TEMPL}	-40°C ≤ T_A ≤ +85°C		24		ppm/°C
Output Current	I_{OUT}	Note 1 Subject to Dropout Voltage Limit	0		1.0	A
Shut-down Current	I_{SD}	ENABLE = Low		1.5		µA
Over Current Protection (OCP) Threshold	I_{LIM}	2.7V ≤ V_{IN} ≤ 5.5V 0.6V ≤ V_{OUT} ≤ 3.3V	1.5	2.2		A
Feedback Pin Input Current	I_{FB}	Note 3		<100		nA
Enable Pin Logic Low	V_{ENLO}		0		0.3	V
Enable Pin Logic High	V_{ENHI}		1.4		AVIN	V
Enable Pin Current	I_{ENABLE}	Note 3		<100		nA
Operating Frequency	F_{OSC}			18.5		MHz
V_{OUT} Rise Time	T_{RISE}	(Note 3 and 4)		850		µs

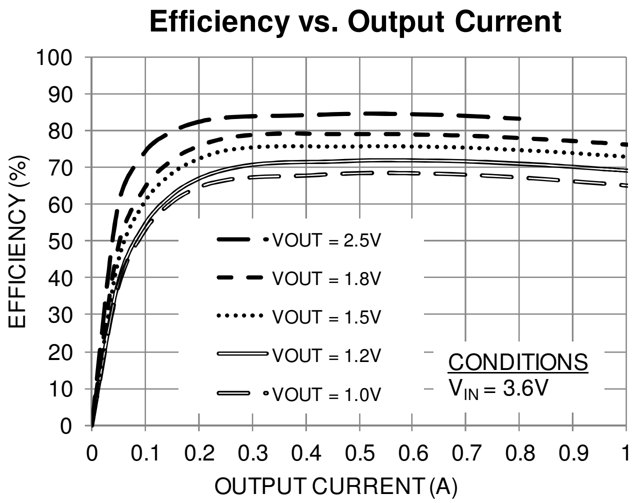
Note 3: Parameter not production tested but is guaranteed by design.

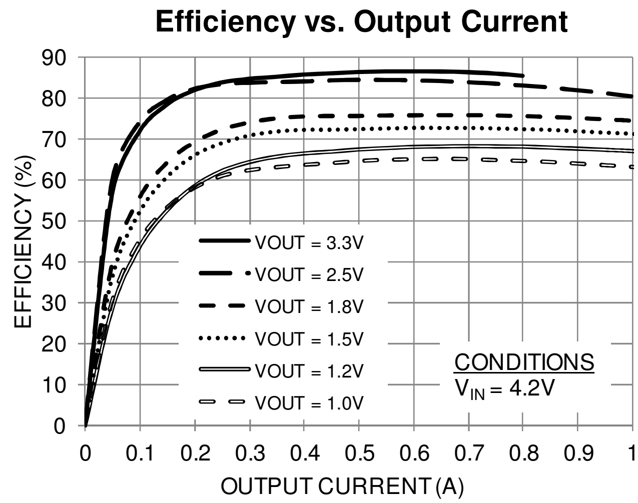
Note 4: Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

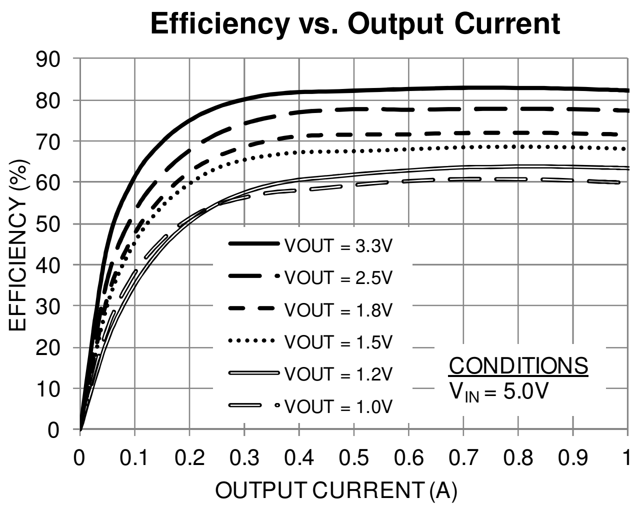
Typical Performance Curves

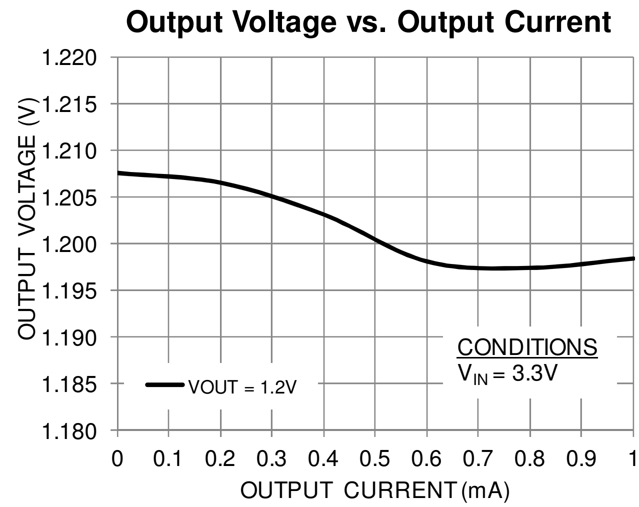












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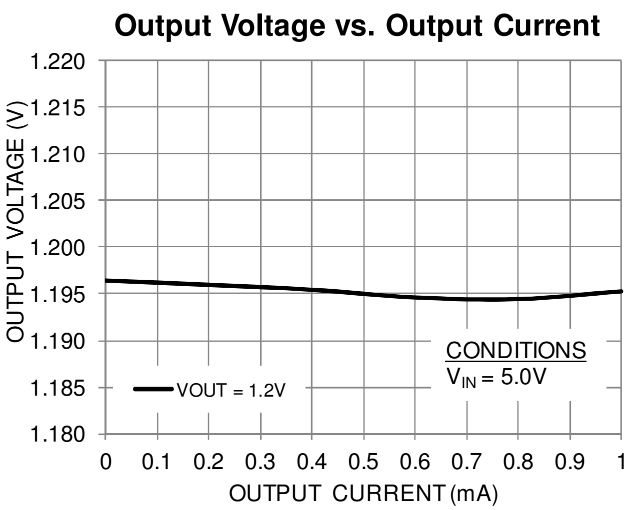

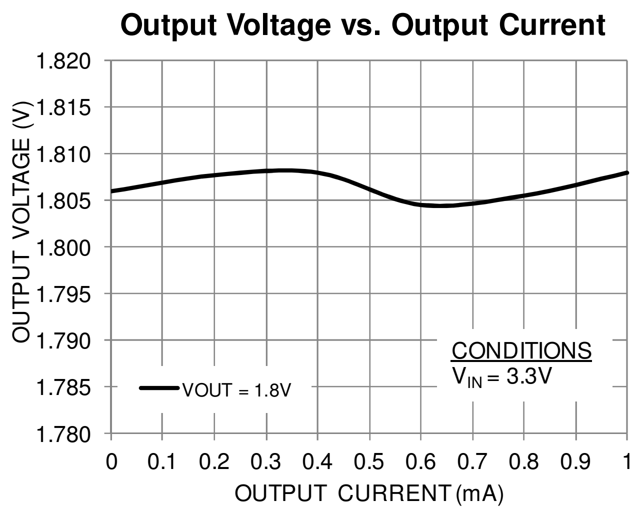

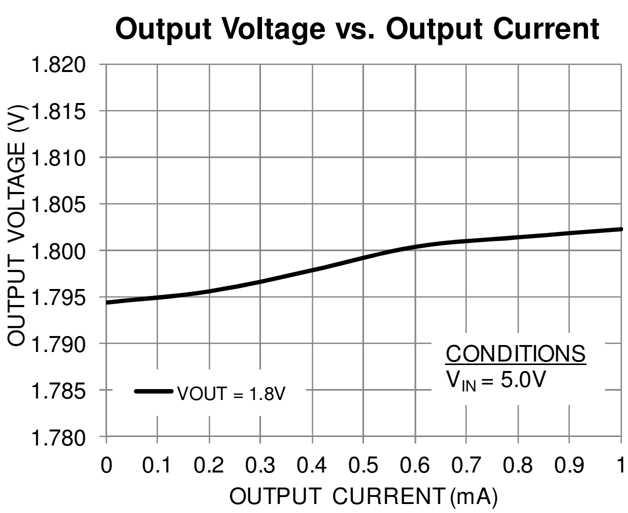

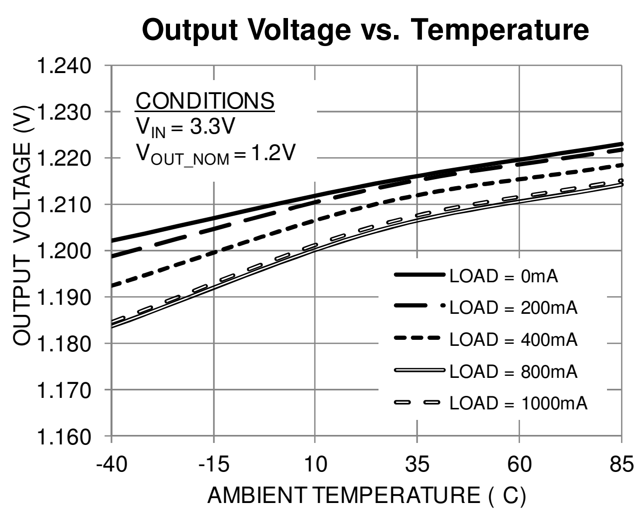

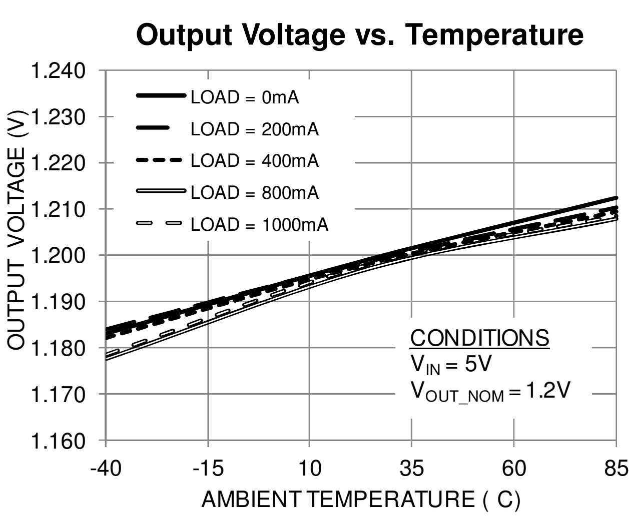

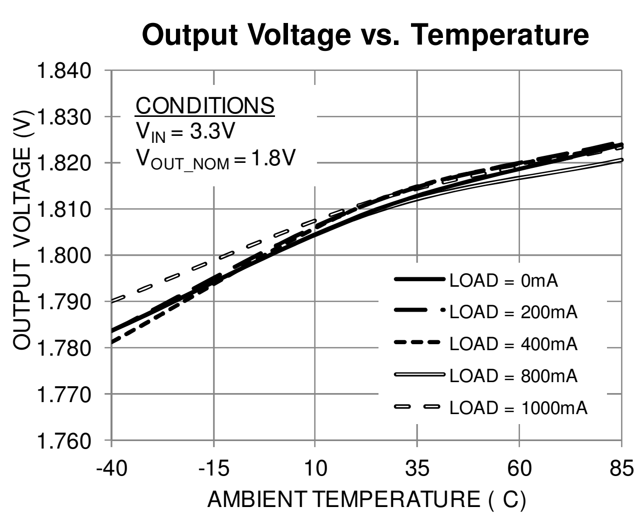

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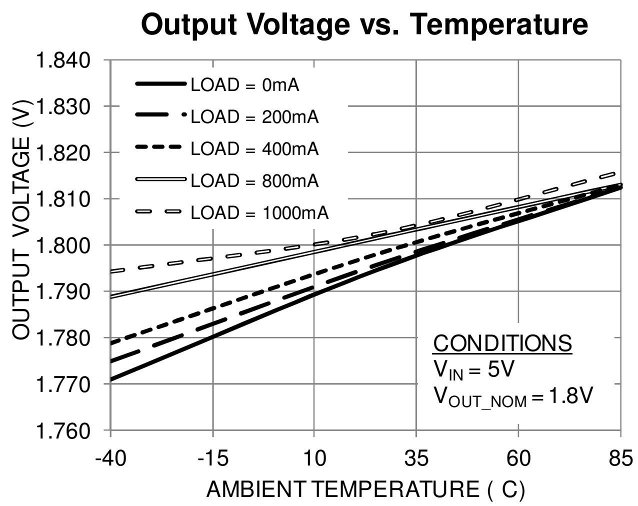

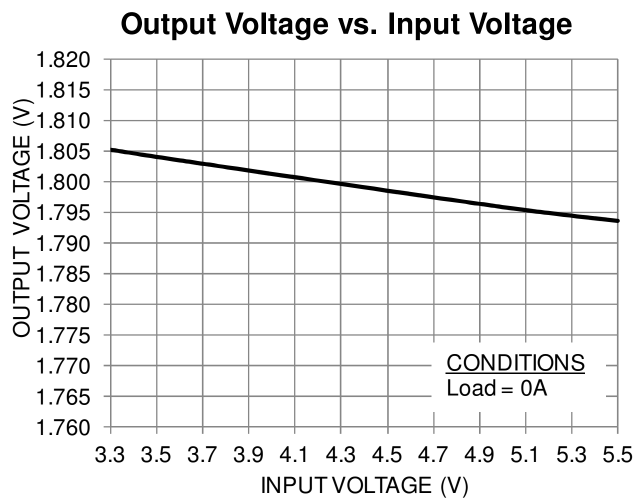

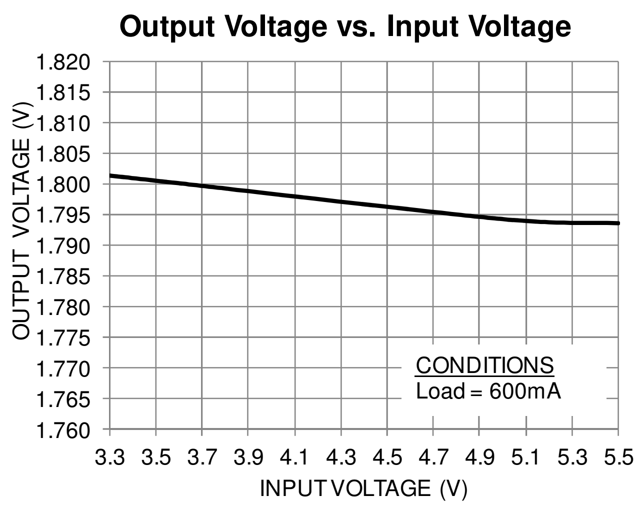

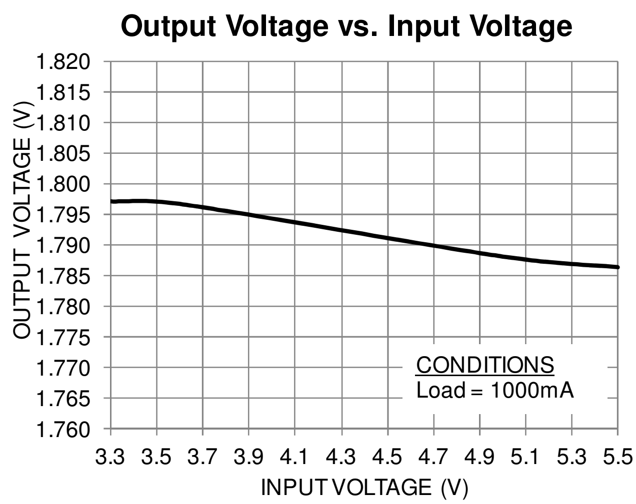

Typical Performance Characteristics

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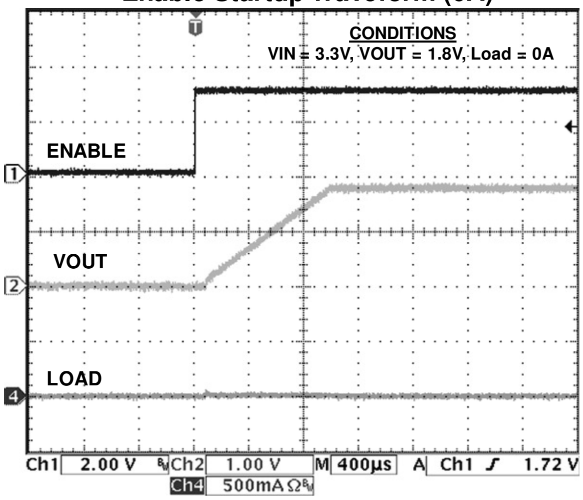
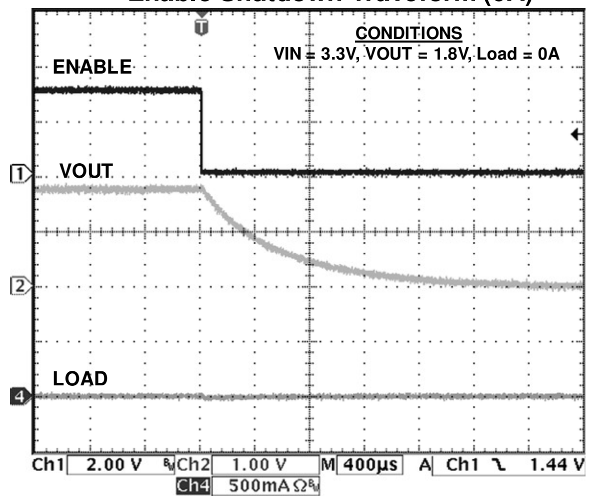
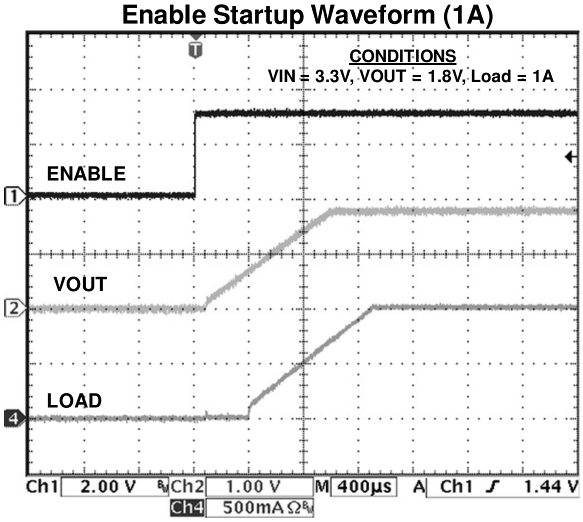


Enable Shutdown Waveform (0A)



Enable Startup Waveform (1A)



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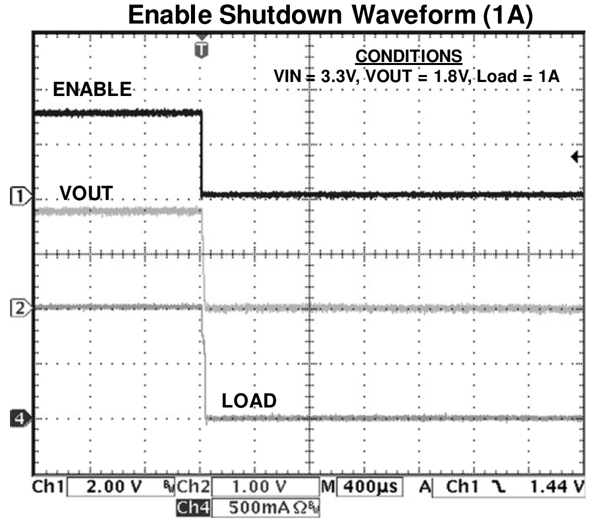

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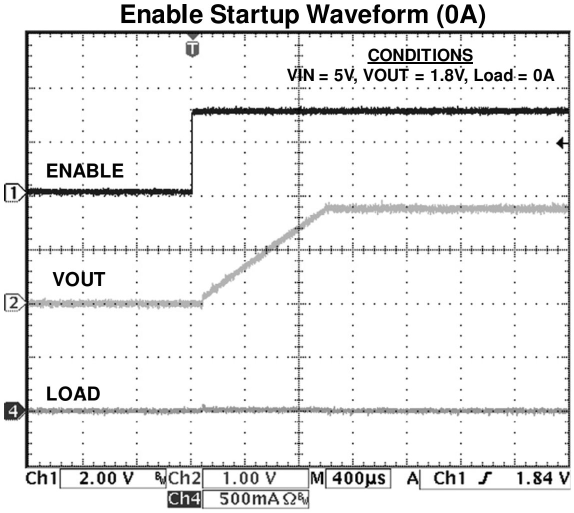

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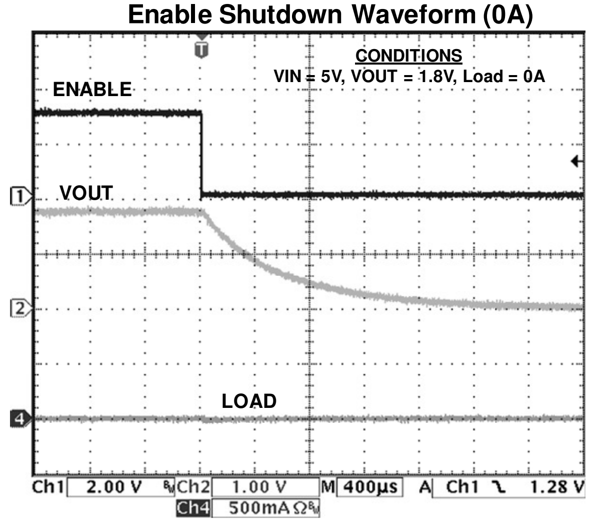

Typical Performance Characteristics (Continued)

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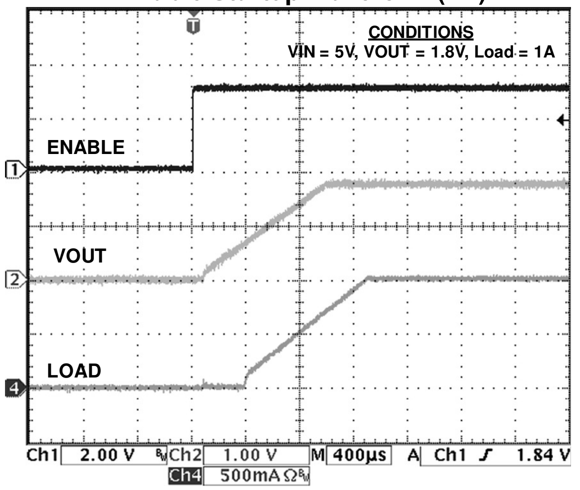
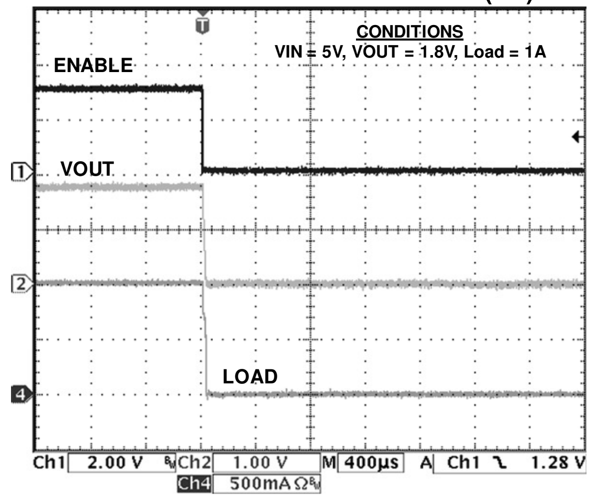
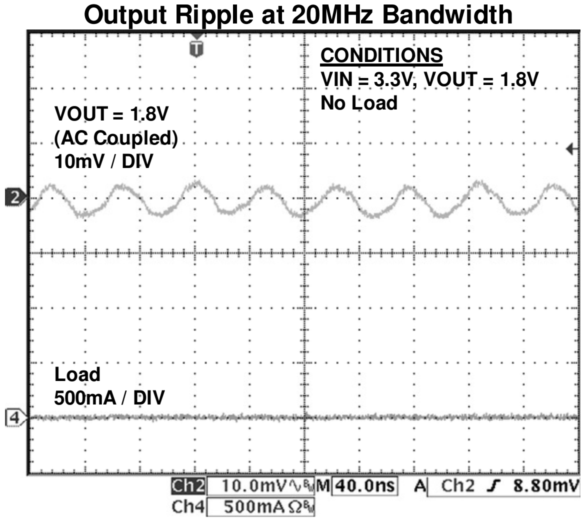


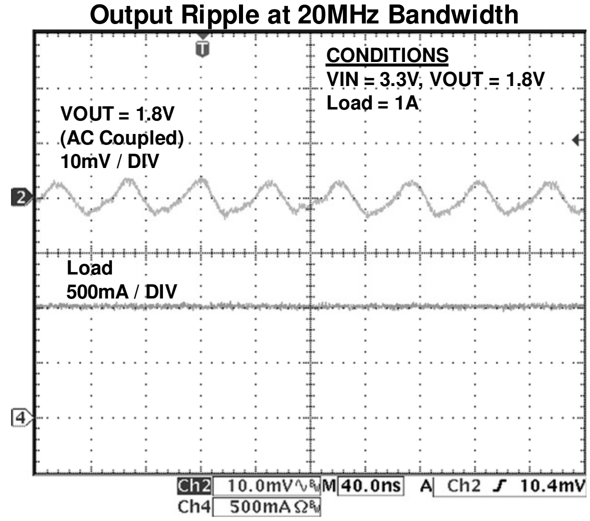
Enable Shutdown Waveform (1A)



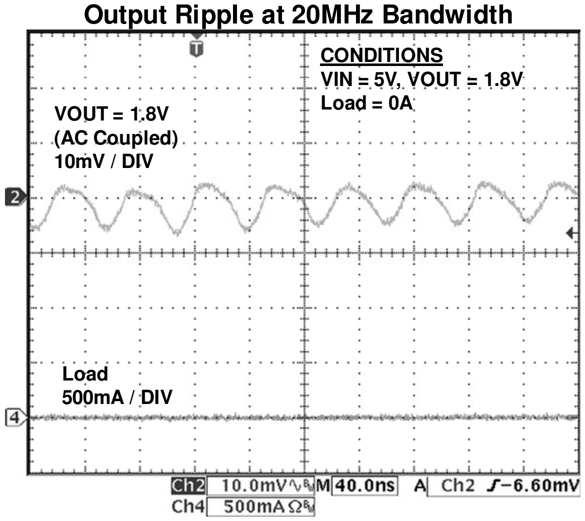
Output Ripple at 20MHz Bandwidth



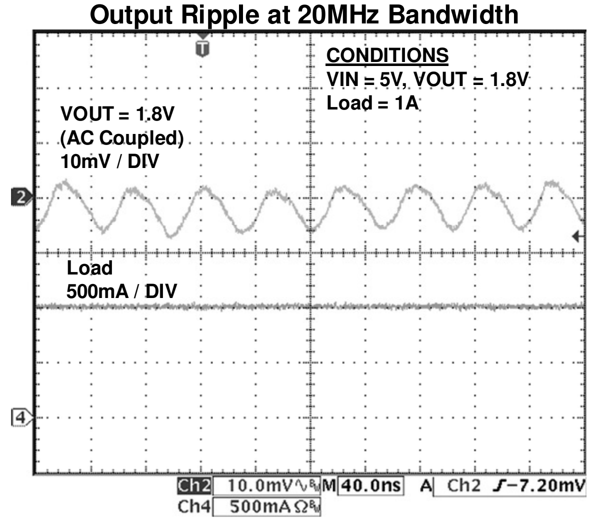
Output Ripple at 20MHz Bandwidth



Output Ripple at 20MHz Bandwidth

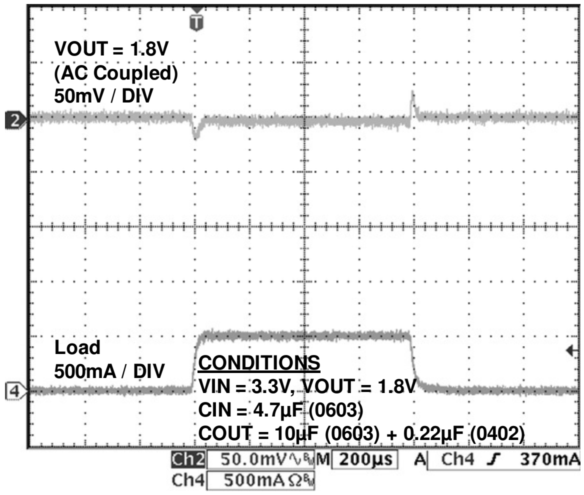


Output Ripple at 20MHz Bandwidth

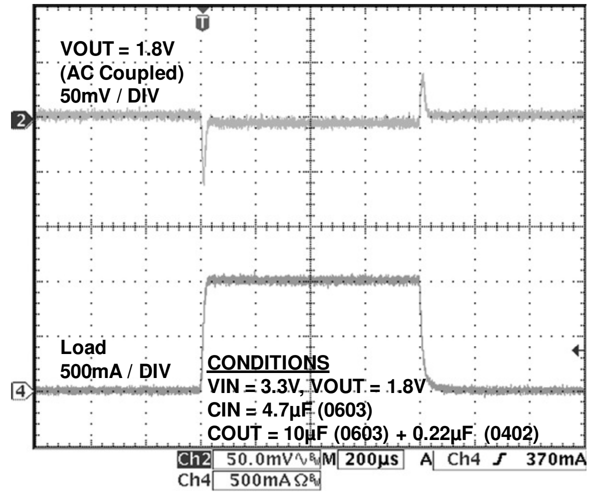


Typical Performance Characteristics (Continued)

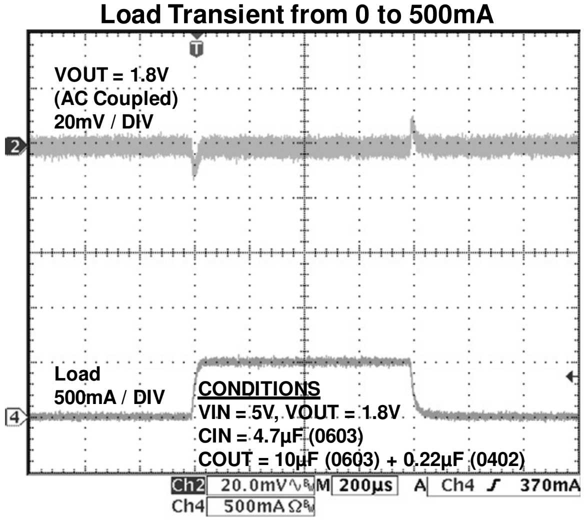
Load Transient from 0 to 500mA



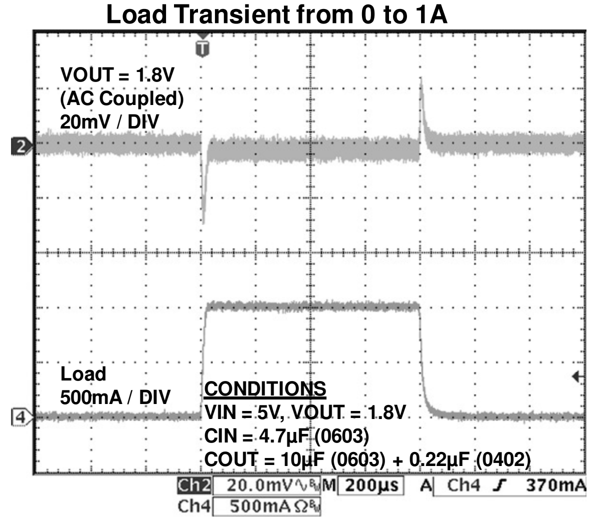
Load Transient from 0 to 1A



Load Transient from 0 to 500mA



Load Transient from 0 to 1A



Functional Block Diagram

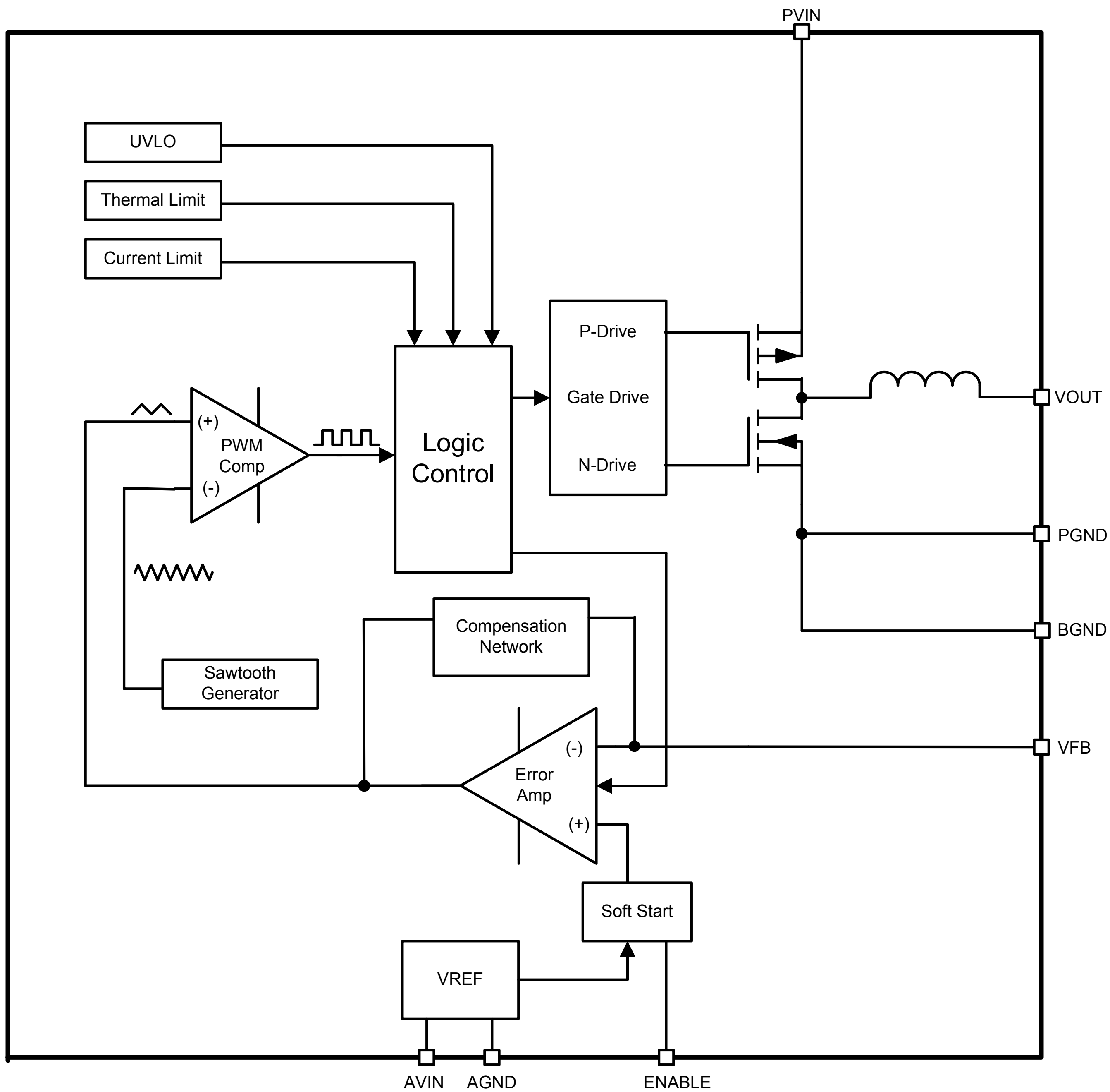


Figure 4: Functional Block Diagram

Functional Description

Functional Overview

The EL711DI integrates MOSFET switches, the PWM controller, gate-drive, controller compensation, and a magnetics-on-silicon inductor into a small 3.0mm x 4.5mm x 0.9mm DFN package. Advanced package design, along with the high level of integration, provides low output ripple and noise. The EL711DI uses voltage mode control for high noise immunity and load matching to advanced sub-90nm digital-chip loads. An external resistor divider is used to set the output voltage over the 0.6V to 5.0V range. The EL711DI provides exceptional power density for a 1000mA DC-DC converter solution.

The key enabler of this revolutionary integration is Enpirion's proprietary high speed power MOSFET technology combined with Enpirion's latest advanced magnetics-on-silicon inductor technology. The advanced MOSFET switches are implemented in deep sub-micron CMOS generating very low switching loss at ultra-high switching frequencies while allowing monolithic integration. The semiconductor process allows seamless integration of all switching, control, and inductive energy storage functions.

The proprietary magnetic-on-silicon technology provides high-density, high-inductance in a very small footprint on a silicon die. Enpirion magnetics are carefully matched to the control and compensation circuits yielding an optimal solution with assured performance over the entire operating range.

Protection features include under-voltage lock-out (UVLO), over-current protection (OCP), short circuit protection, and thermal overload protection.

Integrated Inductor: Low-Loss, Low Noise

The EL711DI utilizes a proprietary low loss integrated inductor technology. The integration of the inductor greatly simplifies the power supply design process. Its inductor on silicon is manufactured with ultra-low loss alloys capable of operating in the 10-20 MHz regime. Alloy shielding and compact die construction of the inductor silicon die reduces the conducted and radiated noise that can couple into the traces of the printed circuit board. Further, the package layout is optimized to reduce the electrical path length for the high *di/dt* currents that are a major source of radiated emissions from DC-DC converters. The unique, leading-edge integrated inductor technology provides the optimal solution to complexity, output ripple, and costs that plague low power DC-DC converter design with a viable LDO alternative.

Controller Topology

The EL711DI utilizes on-chip Type III Voltage-Mode control. Voltage-Mode control is properly impedance matched to digital loads in the sub-90nm process technologies that are used in today's advanced ICs. It also provides a high degree of noise immunity at light load currents so that low ripple and high accuracy are maintained over the entire load range. The very high switching frequency allows for a very wide control loop bandwidth and hence excellent transient performance.

Soft Start

Internal soft start circuits limit in-rush current when the device starts up from a power down condition or when the "ENABLE" pin is asserted "high". Digital control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The EL711DI has a pre-set, fixed V_{OUT} ramp time. Therefore, the ramp rate will vary with the output voltage setting. V_{OUT} ramp time is given in the Electrical Characteristics Table.

Due to this fixed startup ramp time, large and excessive bulk capacitance on the output of the device can cause an over-current trip condition at startup. The maximum total capacitance on the output, including the output filter capacitor and bulk and decoupling capacitances, at the load, is given as:

$$C_{OUT\_TOTAL\_MAX}\ (\mu F) = 718\ /\ V_{OUT}\ (V)$$

The nominal value for C_{OUT} is 10µF. See the applications section for more details.

Over-Current and Short-Circuit Protections (OCP and SCP)

The current limit function is achieved by sensing the current flowing in the high-side switch through a sense P-MOSFET which is compared to a reference current. When this level is exceeded the high-side P-FET is turned off and the low-side N-FET is turned on, pulling V_{OUT} low. This condition is maintained for approximately 0.2 – 0.5 ms followed by a normal soft start procedure. If the over-current condition still persists after soft start, this hiccup cycle will repeat itself indefinitely until the over-current condition is removed.

Hiccup Mode Over-Current Protection

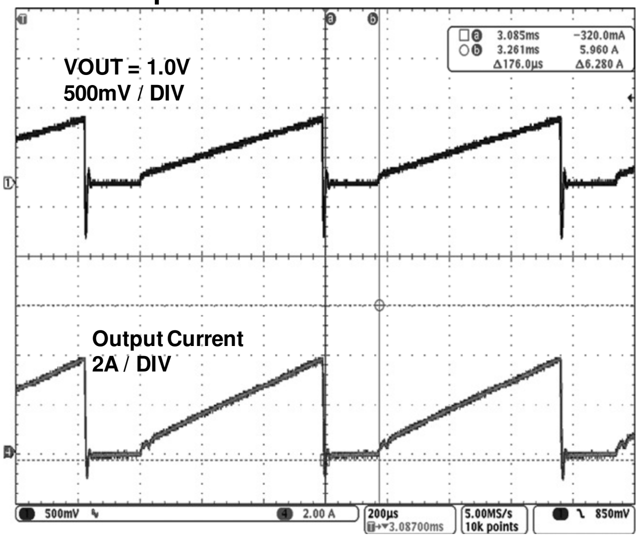


Figure 5. Hiccup Over-Current Protection

Under-Voltage-Lockout (UVLO)

During initial power-up the under-voltage-lockout circuit will hold-off the switching circuitry until the input voltage reaches a sufficient level to insure proper operation. If the voltage drops below the UVLO threshold, the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between states.

Power-Up Sequencing

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. Tying all three pins together meets these requirements.

Pre-Bias Precaution

The EL711DI is not designed to be turned on into a pre-biased output voltage. Be sure the output capacitors are not charged or the output of the EL711DI is not pre-biased when the EL711DI is first enabled.

Enable

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start, allowing the output voltage to rise monotonically into regulation. A logic low will disable the converter and the device will power down in a controlled manner. Floating the ENABLE pin will cause the regulator to be in an indeterminate state. The ENABLE should not be left floating.

Thermal Shutdown

When excessive power is dissipated in the chip, the junction temperature rises. Once the junction temperature exceeds the internal thermal shutdown temperature, the thermal shutdown circuit turns off the converter output voltage thus allowing the device to cool down. When the junction temperature decreases by 15°C, the device will initiate a normal startup process. This process will repeat itself if the thermal overload condition is not removed.

Application Information

Output Voltage Programming

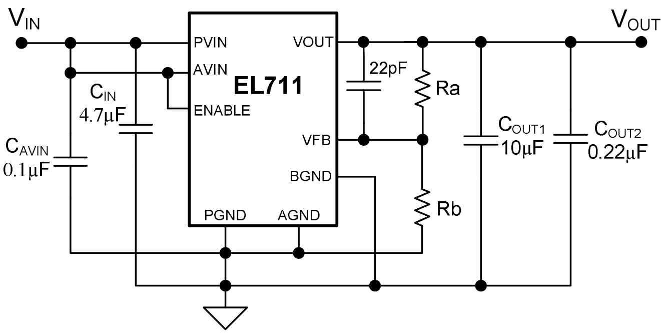
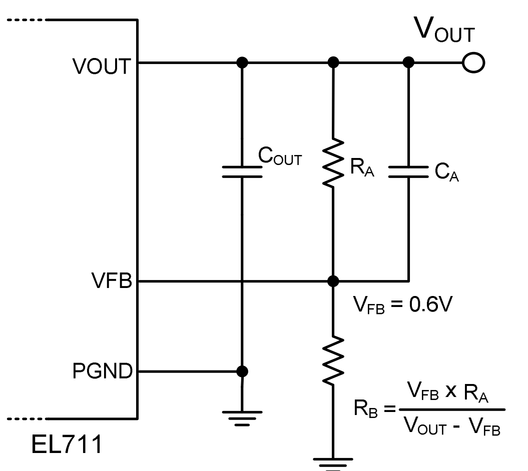


Figure 6: Typical Application Circuit

The EL711DI uses a simple resistor divider to set the output voltage. In Figure 6, use 100kΩ for the upper resistor (R_A). The value of the bottom resistor, R_B in kΩ is then given by:



,

Figure 7: Feedback Resistor Network

where, V_{FB} = 0.6V nominal and V_{OUT} is the desired output voltage. A 22pF MLCC capacitor is required in parallel with R_a for proper control loop compensation.

Input Filter Capacitor Selection

The input capacitor, C_{IN}, should be at least 4.7µF in a 0603 MLCC capacitor case. It must be either X5R or X7R or of an equivalent dielectric formulation. Since Y5V or equivalent dielectric formulations severely lose capacitance with frequency, bias, and temperature, they are NOT suitable for high frequency switch-mode DC-DC converter input filter applications such as the EL711DI.

	MFG	P/N
4.7µF, 10V, X5R, 10%, 0603	Murata	GRM188R61A475KE15D
4.7µF, 10V, X5R, 10%, 0603	Taiyo Yuden	LMK107BBJ475MKLT
4.7µF, 10V, X5R, 10%, 0603	AVX	0603ZD475KAT2A
0.1µF, 10V, X5R, 10%, 0402	Taiyo Yuden	LMK105BJ104KV-F

Table 1. Recommended Input Capacitors

Output Filter Capacitor Selection

The output filter is designed as an impedance network to provide both bulk (low frequency) filtering as well as impedance attenuation (high frequency) switching noise filtering. While only physical capacitors comprise the network, its high frequency equivalent circuit including ESR and ESL are taken into account in the design. For bulk charge and stability requirements, the minimum value of C_{OUT} must be 10µF in a minimum 0603 MLCC capacitor case. Peak-to-peak ripple magnitude can be further reduced as needed by adding additional 10µF 0603 and 0.22µF 0402 MLCC capacitors.

The maximum output filter capacitance permitted directly at the output pins of the device depends on V_{OUT} and is calculated by the equation in the Soft Start section. V_{OUT} must be sensed at the last output filter capacitor at the EL711DI output pins. Wherever the sense location, it should not be at a point where an additional secondary LC filter is inadvertently created for example by placement of capacitors at a distance from one another where the intervening trace forms adequate inductance. Down-stream filtering past the sense point is perfectly acceptable and will not pose any stability concerns. In fact the added benefit of the EL711DI's high operating frequency is that the extra trace inductance will provide further ripple and noise attenuation to exceptionally low levels. Of course proper hardware design practices must be followed to avoid resonances that naturally increase noise levels in ANY switch-mode power supply system.

Additional bulk capacitance for decoupling and bypass can be placed at the point-of-load as long as there is sufficient separation between the V_{OUT} sense point and that bulk capacitance.

Excess total capacitance on the output (Output

Filter + Bulk) will cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

The output capacitor must have an X5R or X7R or equivalent dielectric formulation. Y5V or equivalent dielectric formulations exhibit severe, unacceptable loss of capacitance with frequency, bias, and temperature, as much as 50% or more. They are NOT suitable for high frequency, switch-mode, DC-DC converter output filter applications such as the EL711DI.

	MFG	P/N
10µF, 10V, X5R, 10%, 0603	Murata	GRM188R61A106KE69D
10µF, 10V, X5R, 10%, 0603	Taiyo Yuden	LMK107BBJ106MALT
10µF, 10V, X5R, 20%, 0603	AVX	0603ZD106MAT2A
0.22µF, 10v, X5R, 10%, 0402	Taiyo Yuden	LMK105BJ224KV-F

Table 2. Recommended Output Capacitors

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Enpirion PowerSoC helps alleviate some of those concerns.

The Enpirion EL711DI DC-DC converter is packaged in a 3x4.5x0.9mm 16-pin DFN package. The DFN package is constructed with copper lead frames that have exposed thermal pads. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 155°C.

The following example and calculations illustrate the thermal performance of the EL711DI.

Example:

V_{IN} = 3.3V

V_{OUT} = 1.8V

I_{OUT} = 1000mA

First calculate the output power.

P_{OUT} = 1.8V x 1A = 1.8W

Next, determine the input power based on the efficiency (η) shown in Figure 8.

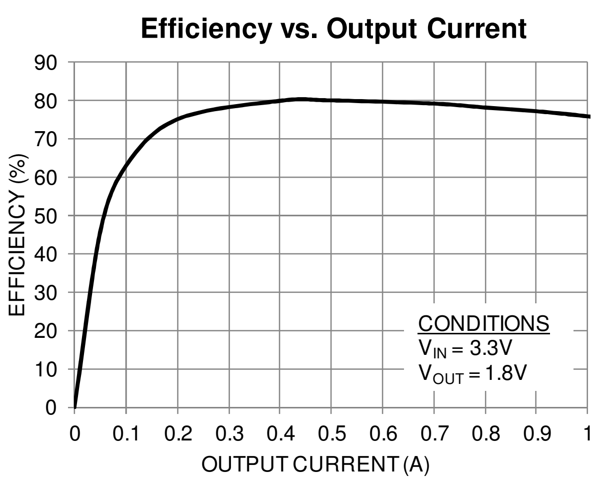


Figure 8: Efficiency vs. Output Current

For V_{IN} = 3.3V, V_{OUT} = 1.8V at 1A, η ≈ 76%

η = P_{OUT} / P_{IN} = 76% = 0.76

P_{IN} = P_{OUT} / η

P_{IN} ≈ 1.8W / 0.76 ≈ 2.37W

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

P_D = P_{IN} – P_{OUT}

≈ 2.37W – 1.8W ≈ 0.57W

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EL711DI has a θ_{JA} value of 60 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

ΔT = P_D x θ_{JA}

ΔT ≈ 0.57W x 60°C/W = 34.2°C ≈ 34°C

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

T_J = T_A + ΔT

T_J ≈ 25°C + 34°C ≈ 59°C

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

T_{AMAX} = T_{JMAX} – P_D x θ_{JA}

≈ 125°C – 34°C ≈ 91°C

The maximum ambient temperature the device can reach is 85°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate.

Engineering Schematic

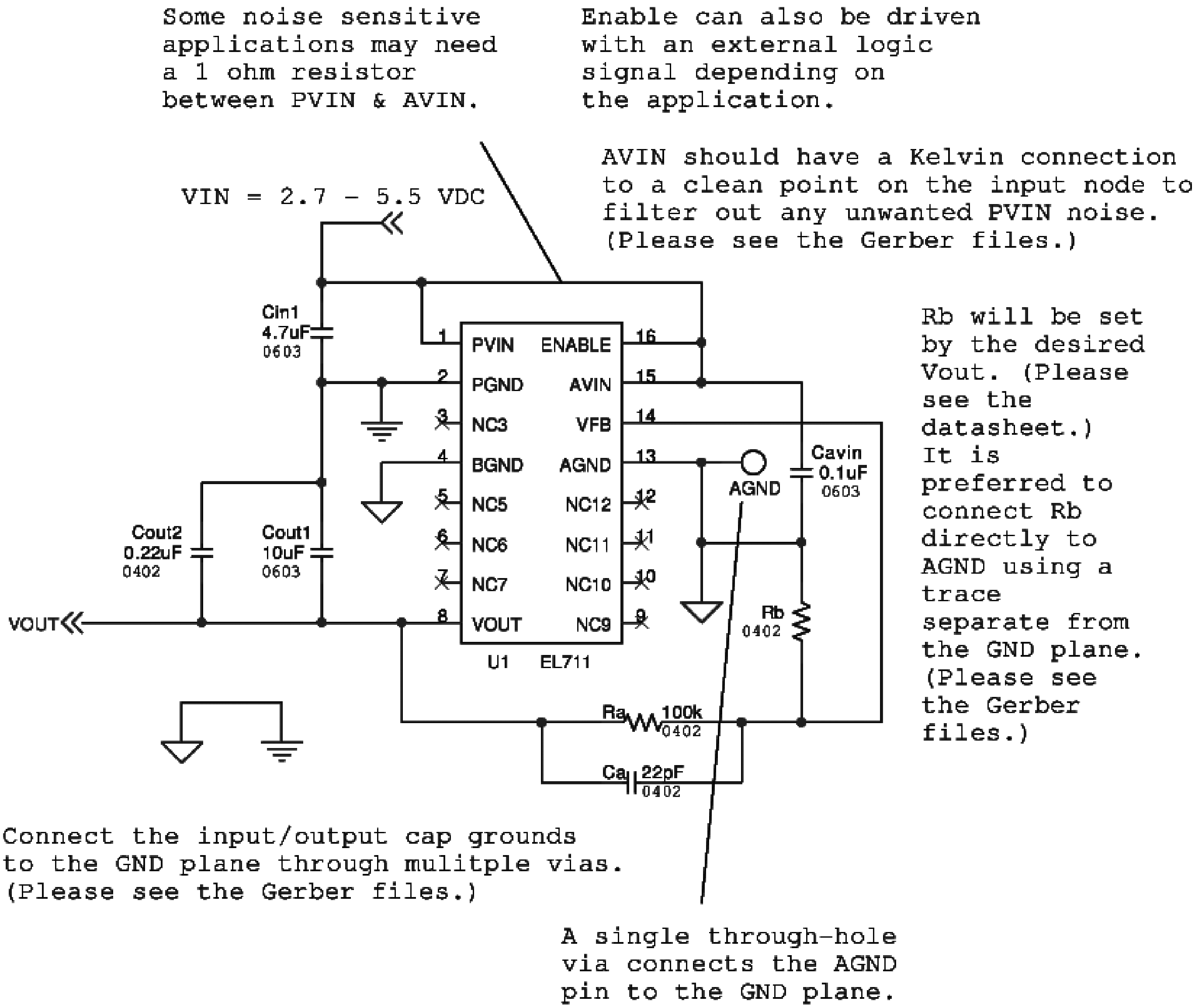


Figure 9: Engineering Schematic for Layout Recommendation Section

Layout Recommendation

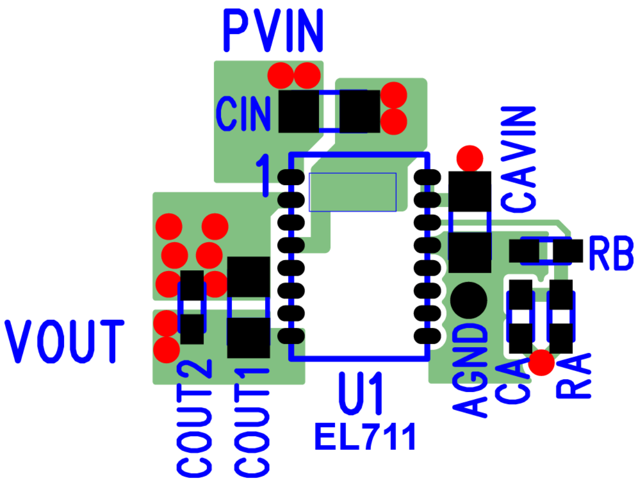


Figure 10: Top Layout with Critical Components Only (Top View). See Figure 9 for corresponding schematic.

This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode with ENABLE tied to AVIN. Alternate ENABLE configurations need to be connected and routed according to customer application. Please see the Gerber files at www.enpirion.com for details on all layers. ***Due to the high switching frequency, the layout for this part is very critical. To ensure success for this product, these layout recommendations and the Enpirion Gerbers must be followed exactly.***

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EL711 package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EL711 should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to be separated with the input ground connected directly to the thermal pad. The output ground should be connected directly to the PGND (pin 2). Both input and output ground should have vias to the system ground planes below. The trace from the thermal pad to the input capacitor also carries heat from the thermal pad to the ground plane through the vias next to CIN.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the input capacitor and the traces leading up to the device. There needs to be a copper void in layers 1, 2, and layer 3 under the inductor portion of the EL711. Please see the Gerber files for exact details.

Recommendation 4: Multiple small vias should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops.

Recommendation 5: AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. In our recommended layout this connection is made on the back side at the input vias just above CIN. See the Gerber files for exact details. There is also a need for a decoupling capacitor CAVIN right next to the AVIN and AGND pins.

Recommendation 6: In order to avoid unnecessary ground loops, the copper from the AGND pin should only connect to CAVIN, R_B, and the via going to the ground plane.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 10. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. In our recommended layout this trace is on the back side. Please see the Gerber files.

Recommendation 9: Keep R_A, C_A, and R_B close to the VFB pin (Refer to Figure 10). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to AGND instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations and the Gerber files exactly to optimize performance. Verify with Enpirion any deviations from our layout recommendations. Contact Enpirion Applications Engineering for detailed support (techsupport@enpirion.com).

Recommended PCB Footprint

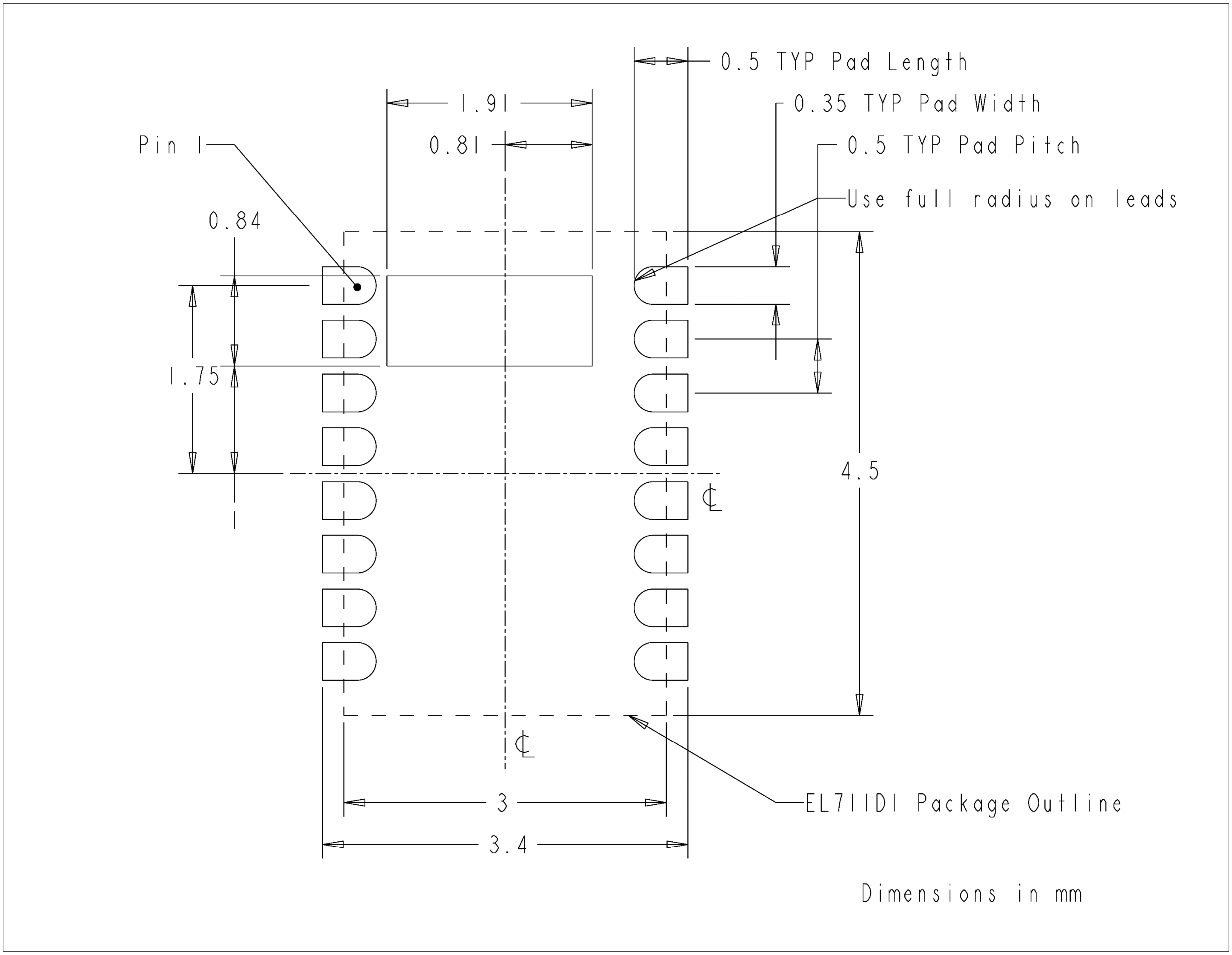


Figure 11: EL711DI PCB Footprint (Top View)

Package and Mechanical

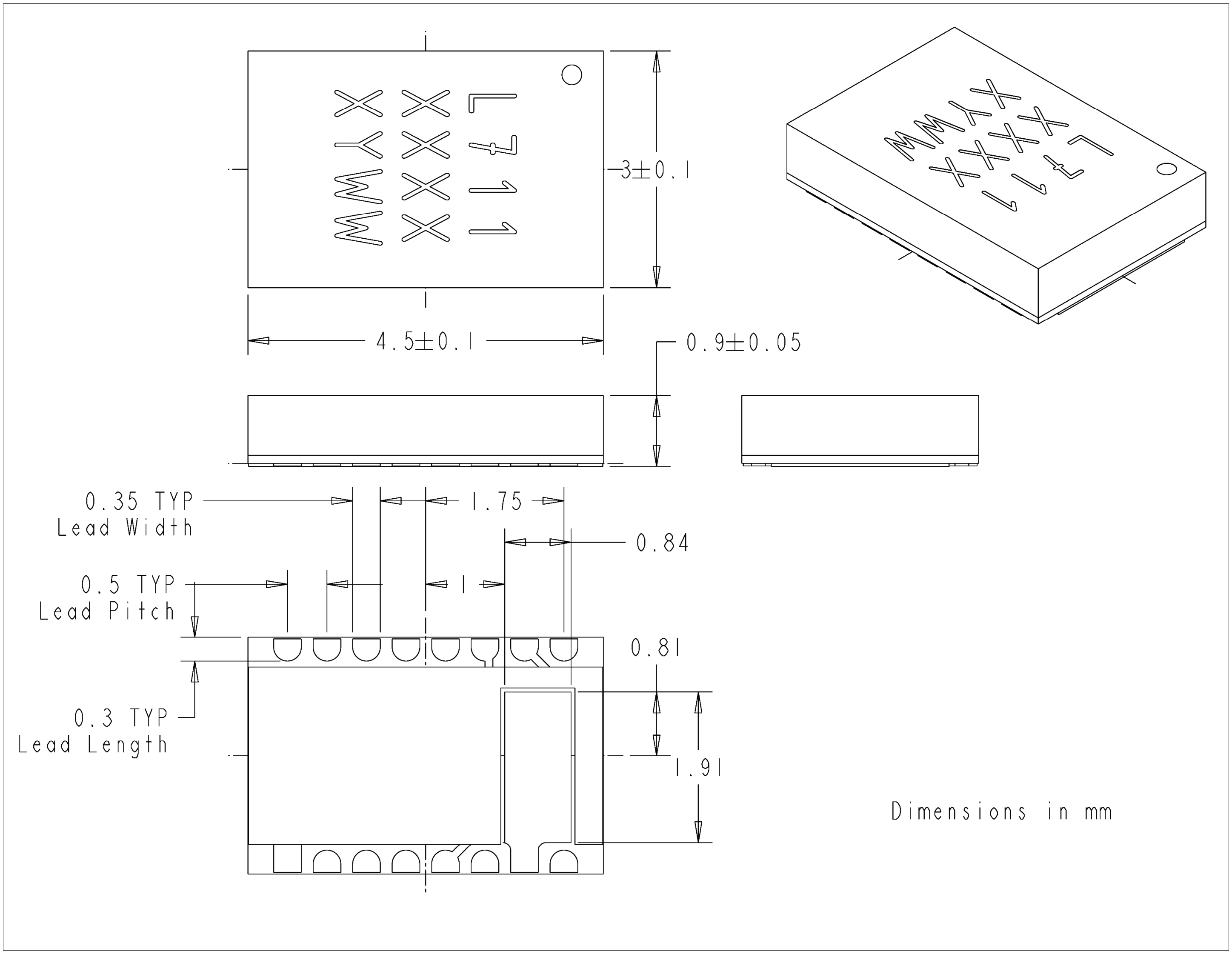


Figure 12: EL711DI Package Dimensions (Bottom View)

Packing and Marking Information: http://www.enpirion.com/resource-center-packing-and-marking-information.htm

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