REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added K package. Added 04 device, two suppliers and 05 device, one supplier. Added vendor CAGE 34335 for devices 01L, 013, and 02L. Editorial changes throughout. Added vendor CAGE 34335 for devices 01K, 023, and 02K. Redrawn.	91 – 04 – 19	M. A. Frye
B	Added vendor CAGE 65786 for devices 01, 02, 03, 04, and 05LX, KX, and 3X. Added vendor CAGE 18324 for devices 01, 02, 04, and 05LX. IAW NOR 5962-R079-93.	93 – 01 – 28	M. A. Frye
C	Added 06 device for one supplier. Added test t_{SU2} to table I. Editorial changes throughout. Redrawn.	93 – 07 – 30	M. A. Frye
D	Added devices 07-14, Added CAGE 1FN41 for devices 13 and 14, added test I_{CCSB} to table I for devices 13 and 14, and updated text to newer boiler plate.	97 – 03 – 04	Raymond Monnin
E	Changes in accordance with NOR 5962-R263-97	97 – 04 – 23	Raymond Monnin
F	Changes in accordance with NOR 5962-R341-97	97 – 06 – 05	Raymond Monnin
G	Added powerup-reset parameters to table I, and the waveform as figure 5. Updated boilerplate. ksr	98 – 07 – 10	Raymond Monnin
H	Changed minimum IOS value for devices 01 thru 06 on table I. Value was changed from -50 mA to -30 mA. ksr	99 – 03 – 19	Raymond Monnin
J	Updated boiler plate. ksr	02 - 10 - 10	Raymond Monnin

REV																			
SHEET																			
REV	J	J	J																
SHEET	15	16	17																

REV STATUS OF SHEETS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89 – 11 – 28

REVISION LEVEL
J

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, PROGRAMMABLE ARRAY LOGIC (EEPLD), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89841**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

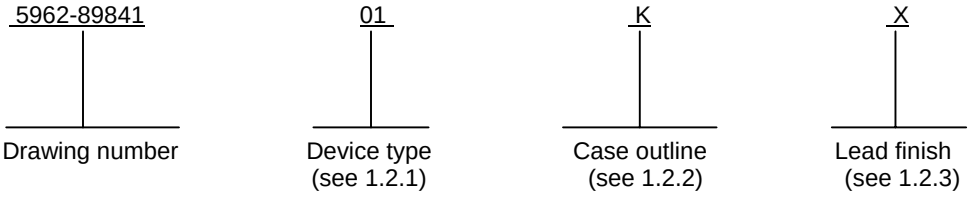
5962-E540-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01, 07	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	30
02, 08	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	20
03, 09	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	15
04, 10	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	25
05, 11	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array (higher tCO, lower fCLK2)	15
06, 12	22V10	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	10
13	22V10L	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	25
14	22V10L	22-input, 10-output, EECMOS, architecturally generic, programmable AND-OR array	20

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
K	GDFP2-F24 or CDFP3-F24	24	flat pack
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
3	CQCC1-N28	28	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage applied	-0.5 V dc to VCC +1.0 V dc 1/
Off-state output voltage applied	-0.5 V dc to VCC +1.0 V dc 1/
Storage temperature range (TSTG)	-65°C to +150°C
Maximum power dissipation (PD) 2/	1.5 W
Lead temperature (soldering, 10 seconds) (TSOL)	+260°C
Thermal resistance, junction-to-case (ΘJC)	See MIL-STD-1835
Junction temperature (TJ)	+175°C
Data retention	10 years (minimum)
Endurance	100 erase/write cycles (minimum)

1/ Minimum voltage is -0.5 V which may undershoot to -2.5 V for pulses of less than 20 ns.
2/ Must withstand the added PD due to short circuit test; e.g., IOS.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	2.0 V dc to V_{CC} +1.0 V dc
Low level input voltage (V_{IL})	V_{SS} -0.5 V dc to +0.8 V dc
High level output current (I_{OH})	-2.0 mA maximum
Low level output current (I_{OL})	12 mA maximum
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1. Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.2.1 Unprogrammed devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.2.3 Case outlines The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Table I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, 4.5 V $\le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input leakage current 1/	I_{LX}	$0.0 \text{ V} \le V_{IN} \le V_{CC}$	1, 2, 3	01-06, 13,14	10	-150	µA
				7-12	-10	10	
Bidirectional pin leakage current 1/	$I_{I/O/Q}$	$0.0 \text{ V} \le V_{I/O/Q} \le V_{CC}$	1, 2, 3	01-06, 13,14	10	-150	µA
				7-12	-40	40	
Output low voltage	V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA, $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All		0.5	V
Output high voltage	V_{OH}	$V_{CC} = 4.5$ V, $I_{OH} = -2$ mA, $V_{IN} = V_{IH}$ or V_{IL}	1, 2, 3	All	2.4		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.0		V
Operating power supply current	I_{CC}	$V_{IL} = 0.5$ V, $V_{IH} = 3.0$ V	1, 2, 3	01-06		150	mA
		$f_{tog} = 15$ MHz		07-12		130	
				13,14		70	
Power supply current standby	I_{CCSB}	V_{IN} 0 V or V_{CC} $f_{tog} = 0$ MHz	1, 2, 3	13,14		15	mA
Output short circuit current 3/	I_{OS}	$V_{CC} = 5.0$ V, $V_{OUT} = 0.5$ V	1, 2, 3	01-06	-30	-135	
		$T_A = 25°C$ see 4.3.1d		07-12	-30	-90	mA
Input capacitance	C_{IN}	$V_{CC} = 5.0$ V, $V_I = 2.0$ V $f = 1.0$ MHz, $T_A = +25°C$, See 4.3.1c	4	All		10	pF
Bidirectioanl pin capacitance	$C_{I/O/Q}$	$V_{CC} = 5.0$ V, $V_{I/O/Q} = 2.0$ V $f = 1.0$ MHz, $T_A = +25°C$, See 4.3.1c	4	All		10	pF
Functional tests		See 4.3.1e	7, 8A,8B	All			
Input or feedback to nonregistered output	t_{PD}	$V_{CC} = 4.5$ V, see figures 3 and 4 4/	9, 10, 11	01		30	ns
				02		20	
				03, 05		15	
				08, 09, 11	3	15	
				04		25	
				06		10	
				12	3	10	
				07,10, 13	3	25	
				14	3	20	

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V, $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock to output delay 5/	t_{CO}	V_{CC} = 4.5 V see figures 3 and 4 4/	9, 10, 11	01,04		20	ns
				02		15	
				07, 10, 14	2	15	
				03		8	
				08, 09, 11	2	8	
				05		12	
				06		7	
				12	2	7	
				13	2	20	
Input to output enable	t_{EA}		9, 10, 11	01,04, 07,10, 13		25	ns
				02, 14		20	
				03, 05, 08,09, 11		15	
				06, 12		10	
Input to output disable 6/	t_{ER}		9, 10, 11	01,04, 07,10, 13,		25	ns
				02, 14		20	
				03, 05,08, 09,11		15	
				06		12	
				12		10	
Asynchronous register reset 5/	t_{RES}		9, 10, 11	01,04, 13		30	ns
				02.07, 10,14		25	
				03.05, 08,09, 11		20	
				06,12		12	
Clock frequency without feedback 5/ 7/ $1/(t_{PWH} + t_{PWL})$	f_{CLK1}		9, 10, 11	01	0	25.0	MHz
				02,14,	0	33.3	
				07,10	0	35.7	
				03, 05	0	62.5	
				08, 09, 11	0	83.3	
				04, 13	0	33.0	
				12	0	142.0	
				06	0	166.0	

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock frequency with feedback 5/ 7/ $1/(t_{CO} + t_{SU1})$	f_{CLK2}	V_{CC} = 4.5 V see figures 3 and 4 4/	9, 10, 11	01	0.0	22.0	MHz
				07,10	0.0	30.3	
				02,14	0.0	31.2	
				03,08, 09,11	0.0	50.0	
				04, 13	0.0	26.3	
				05	0.0	42.0	
				06,12	0.0	76.9	
Input or feedback setup time before rising clock 5/	t_{SU1}		9, 10, 11	01	25		ns
				02, 14	17		
				03,05	12		
				08, 09, 11	10		
				04, 07, 10, 13	18		
				06, 12	6		
Synchronous Preset setup time	t_{SU2}		9, 10, 11	01	25		ns
				02, 14	17		
				08, 09, 11	10		
				03, 05	12		
				04, 07, 10, 13	18		
				06, 12	7		
Input or feedback hold time after rising clock 5/	t_h		9, 10, 11	All	0		ns
Clock pulse width, high 5/	t_{PWH}		9, 10, 11	01	20		ns
				02, 14	15		
				03, 05	8		
				04, 13	15		
				07, 10	14		
				08, 09, 11	6		
				06, 12 7/	3		

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V, 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock pulse width, low 5/	t_{PWL}	V_{CC} = 4.5 V see figures 3 and 4 4/	9, 10, 11	01	20		ns
				02, 14	15		
				03, 05	8		
				04, 13	15		
				07, 10	14		
				08, 09, 11	6		
				06, 12 7/	3		
Asynchronous reset pulse width	t_{PWR}		9, 10, 11	01	30		ns
				02, 14	20		
				03, 05, 08, 09, 11	15		
				04, 07, 10, 13	25		
				06, 12	10		
Asynchronous reset to rising clock recovery time	t_{REC}		9, 10, 11	01	30		ns
				02, 14	20		
				03, 05	15		
				08, 09, 11	12		
				04, 07, 10, 13	25		
				06, 12	6		
Clock pulse width 5/ 7/	t_W	See figure 5	9, 10, 11	01, 07	20		ns
				04, 10, 13	15		
				02, 08, 14	15		
				03, 05, 09, 11	8		
				06, 12	3.5		
Setup time 5/ 7/	t_S		9, 10, 11	01, 07	25		ns
				04, 10, 13	18		
				02, 08, 14	17		
				03, 05, 09, 11	12		
				06, 12	6		
Power up reset time 7/	t_{PR}		9, 10, 11	All		1.0	µs

See footnotes at end of table.

1/ The maximum leakage current is due to the internal pull-up resistor on all pins.
2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3/ Not more than one output at a time should be shorted. Short circuit test duration should not exceed 1 second (see 4.3.1d).
4/ AC tests are performed with input rise and fall times (10 percent to 90 percent) of 3.0 ns, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and the output load of figure 3. Input pulse levels are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
5/ Test applies only to registered outputs.
6/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.
7/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2,3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2,3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point Electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroups 1 and 7
** See 4.3.1c

Device Types	All Devices	
Case outlines	K and L	3
Terminal number	Terminal symbol	
1	I/CLK	NC
2	I	I/CLK
3	I	I
4	I	I
5	I	I
6	I	I
7	I	I
8	I	NC
9	I	I
10	I	I
11	I	I
12	GND	I
13	I	I
14	I/O/Q	GND
15	I/O/Q	NC
16	I/O/Q	I
17	I/O/Q	I/O/Q
18	I/O/Q	I/O/Q
19	I/O/Q	I/O/Q
20	I/O/Q	I/O/Q
21	I/O/Q	I/O/Q
22	I/O/Q	NC
23	I/O/Q	I/O/Q
24	V_{CC}	I/O/Q
25	---	I/O/Q
26	---	I/O/Q
27	---	I/O/Q
28	---	V_{CC}

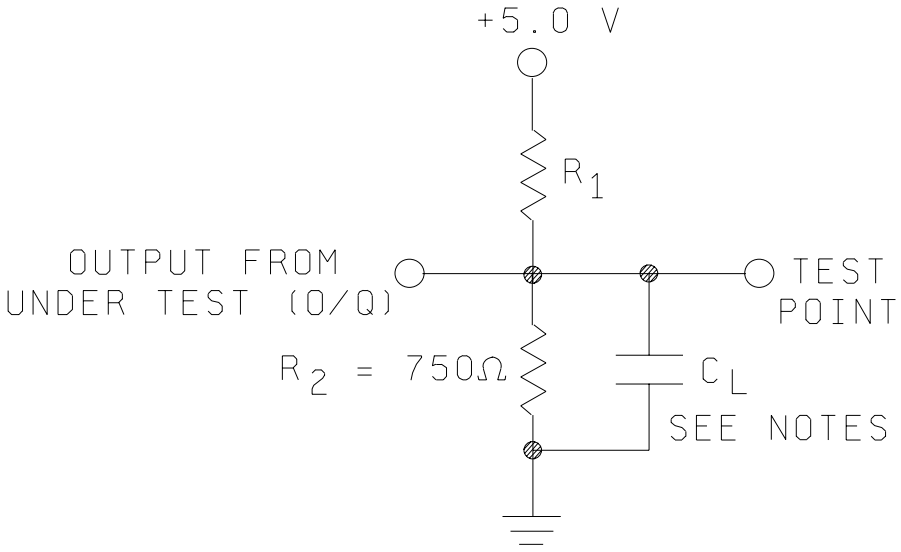
FIGURE 1. Terminal connections.

Inputs											
I/CLK	I	I	I	I	I	I	I	I	I	I	I
X	X	X	X	X	X	X	X	X	X	X	X

Outputs											
I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q	I/O/Q
Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

X = don't care state
Z = high impedance state

FIGURE 2. Truth table (unprogrammed).



Test	R_1	C_L (minimum)
t_{PD}, t_{CO}, t_{RES}, f_{CLK1}, f_{CLK2}	390 Ω	50 pF
t_{EA}	Active high = infinity Active low = 390Ω	50 pF
t_{ER}	Active high = infinity Active low = 390Ω	5 pF

NOTES:
1. CL = load capacitance and includes jig and probe capacitance.
2. A different output load circuit may be utilized, but table I electricals shall be guaranteed with figure 3 output load circuit.

FIGURE 3. Output load circuit.

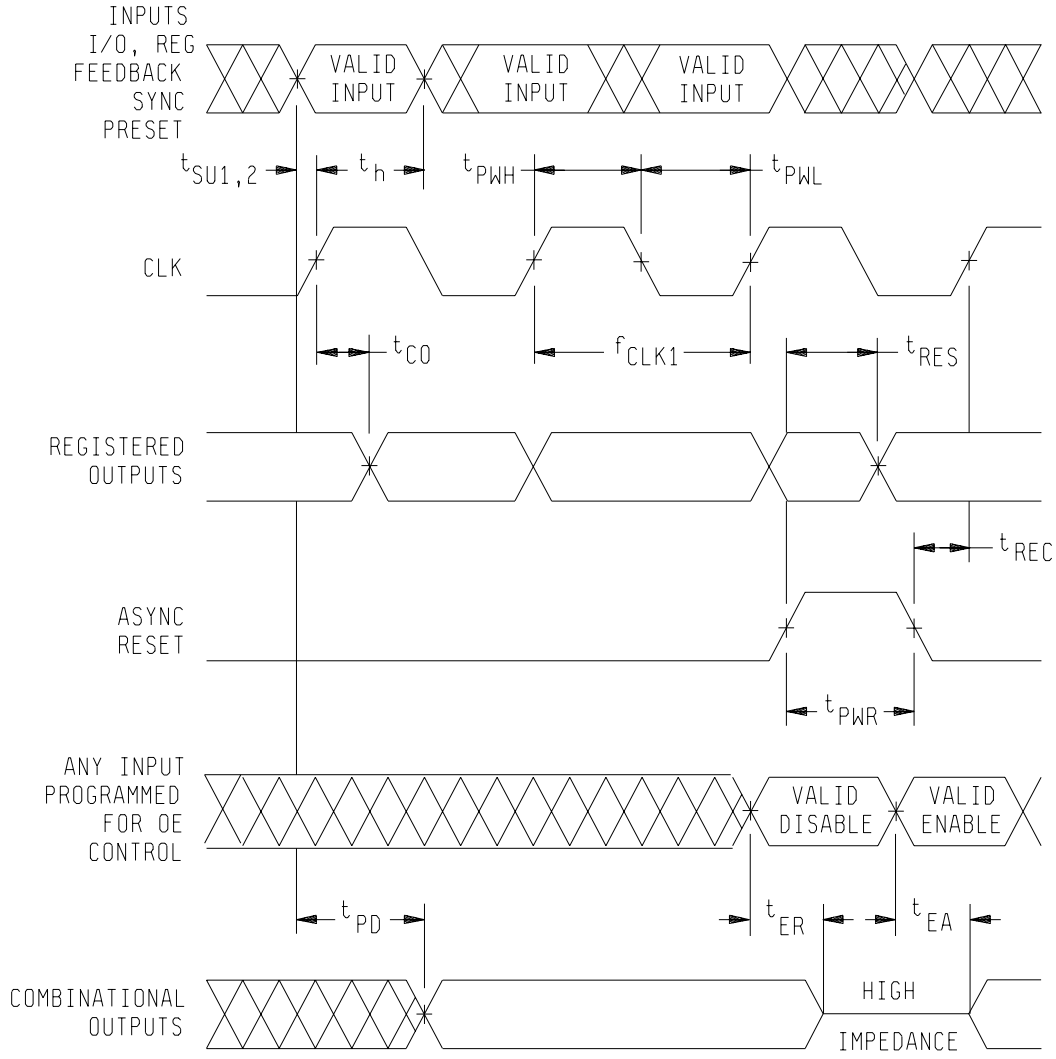
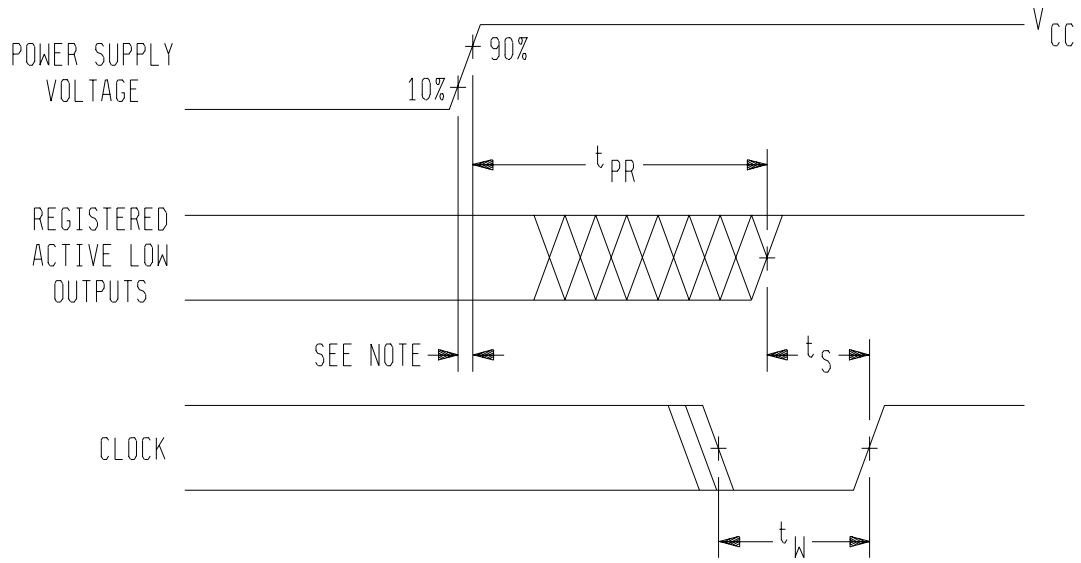


FIGURE 4. Switching waveforms.



Note: The power-up reset feature ensures that all flip-flops will be reset to low after the device has been powered up. The following conditions are required:

a) The V_{CC} rise must be monotonic.
b) After reset occurs, all applicable input and feedback setup times must be met before driving the clock pin high.
c) The clock signal must remain stable beginning prior to the occurrence of the 10% level and continuing until the end of t_{PR}.

FIGURE 5. Power-up Reset waveform.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Devices shall be burned-in containing a pattern that assures all inputs and I/O's are dynamically switched. This pattern must have all cells programmed in a high or low state (not neutralized).

(4) The burn-in pattern shall be read before and after burn-in. Devices having any logic array bits not in the proper state shall constitute a device failure and shall be added as failures for PDA calculation.

b. Interim and final electrical parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. An endurance/retention test prior to burn-in (may be performed at wafer level), in accordance with method 1033 of MIL-STD-883, shall be included as part of the screening procedure with the following conditions:

(1) Cycling may be at equipment room ambient temperature and shall cycle all bit locations for a minimim of 100 cycles. After cycling, devices containing bits which fail to verify shall be considered device failures.

(2) The retention pattern must have a minimum of 50 percent of the logic array programmed.

(3) After cycling, perform a high temperature unbiased bake for a minimum of 48 hours at +150°C. The bake time may be accelerated by using higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = Acceleration factor (unitless quantity) = t_1/t_2.
T = Temperature in Kelvin (i.e., °C + 273 = K).
t_1 = Time (hrs) at temperature T_1.
t_2 = Time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 eV.

The maximum bake temperature shall not exceed +250°C.

(4) After cycling and bake, and prior to burn-in, read the data retention pattern. Test using subgroups 1 and 7 (at the manufacturer's option, high temperature equivalent subgroups 2 and 8A or low temperature equivalent subgroups 3 and 8B may be used in lieu of subgroups 1 and 7). Devices having any logic array bits not in the proper state after storage shall constitute device failure.

(5) At the manufacturer's option, the testing specified in 4.2c(4) may be deleted if the devices are put into burn-in with no reprogramming allowed between the start of data retention bake and the end of burn-in. Exercising this option will result in data retention bake failures being caught and included in post burn-in PDA calculations.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and $C_{I/O/Q}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. I_{OS} measurements in subgroup 1 shall be measured only for the initial test and after process or design changes which may affect I_{OS}. Sample size is 15 devices with no failures, and all output terminals tested.

e. Subgroups 7 and 8 shall be sufficient to verify the truth table.

4.3.2 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) TA = +125°C, minimum.

(3) Test duration: 1,000 hours except as permitted by method 1005 of MIL-STD-883.

(4) All devices shall be programmed with a pattern that assures all inputs and I/O's are dynamically switched.

c. An extended data retention test shall be added. A new sample shall be selected, and the sample size, accept number and frequency of testing shall be the same as that required for group C inspection. Extended data retention shall also consist of the following:

(1) All devices shall have a minimum of 50 percent of the logic array programmed with a charge on all cells, such that the cell will not be in a neutral state.

(2) Unbiased bake for 1,000 hours (minimum) at +150°C (minimum). The unbiased bake time may be accelerated by using a higher temperature in accordance with the Arrhenius Relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

AF = Acceleration factor (unitless quantity) = t_1/t_2.
T = Temperature in Kelvin (i.e., °C + 273 = K).
t_1 = Time (hrs) at temperature T_1.
t_2 = Time (hrs) at temperature T_2.
K = Boltzmanns constant = 8.62 x 10-5 eV/°K using an apparent activation energy (EA) of 0.6 eV.

The maximum bake temperature shall not exceed +200°C.

(3) Read the pattern after bake and perform end-point electrical tests in accordance with table II herein for group C.

4.3.3 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.4 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

4.5 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be made available to the user on request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 02 - 10 - 10

Approved sources of supply for SMD 5962-89841 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8984101LA	3/	PALC22V10D-30DMB
	3/	PALCE22V10-30DMB
	3/	PALCE22V10H-30E4/BLA
	66675	GAL22V10C-30LD/883C
	66675	GAL22V10D-30LD/883C
	0C7V7	QPC22V10-30/BLA
5962-8984101KA	3/	PALC22V10D-30KMB
	3/	PALCE22V10-30KMB
	3/	PALCE22V10H-30E4/BKA
	0C7V7	QPC22V10-30/BKA
5962-89841013A	3/	PALC22V10D-30LMB
	3/	PALCE22V10-30LMB
	3/	PALCE22V10H-30E4/B3A
	0C7V7	QPC22V10-30/B3A
5962-8984102LA	65786	PALC22V10D-20DMB
	65786	PALCE22V10-20DMB
	3/	PALCE22V10H-20E4/BLA
	66675	GAL22V10C-20LD/883C
	66675	GAL22V10D-20LD/883C
	0C7V7	QPC22V10-20/BLA
5962-8984102KA	65786	PALC22V10D-20KMB
	65786	PALCE22V10-20KMB
	3/	PALCE22V10H-20E4/BKA
5962-89841023A	66675	GAL22V10C-20LR/883C
	66675	GAL22V10D-20LR/883C
	3/	PALC22V10D-20LMB
	3/	PALCE22V10-20LMB
	3/	PALCE22V10H-20E4/B3A
	0C7V7	QPC22V10-20/B3A
5962-8984103LA	66675	GAL22V10C-15LD/883C
	66675	GAL22V10D-15LD/883C
	65786	PALC22V10D-15DMB
	65786	PALCE22V10-15DMB
	1FN41	ATF22V10B-15GM/883
5962-8984103LC	6S055	DPA22V10-15LC
5962-8984103KA	3/	PALC22V10D-15KMB
	3/	PALCE22V10-15KMB
	0C7V7	QPC22V10-15/BKA

See footnote at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-89841033A	66675	GAL22V10C-15LR/883C
	66675	GAL22V10D-15LR/883C
	65786	PALC22V10D-15LMB
	65786	PALCE22V10-15LMB
	1FN41	ATF22V10B-15NM/883
5962-8984104LA	3/	PALC22V10D-25DMB
	3/	PALCE22V10-25DMB
	3/	ATF22V10B-25GM/883
	66675	GAL22V10C-25LD/883C
	66675	GAL22V10D-25LD/883C
	3/	PALCE22V10H-25E4/BLA
	0C7V7	QPC22V10-25/BLA
5962-8984104KA	3/	PALC22V10D-25KMB
	3/	PALCE22V10-25KMB
	3/	PALCE22V10H-25E4/BKA
	0C7V7	QPC22V10-25/BKA
5962-89841043A	65786	PALC22V10D-25LMB
	65786	PALCE22V10-25LMB
	3/	ATF22V10B-25NM/883
	3/	PALCE22V10H-25E4/B3A
5962-8984105LA	65786	PALC22V10D-15DMB
	65786	PALCE22V10-15DMB
	1FN41	ATF22V10B-15GM/883
	3/	PALCE22V10H-15E4/BLA
	0C7V7	QPC22V10-15/BLA
5962-8984105KA	3/	PALC22V10D-15KMB
	3/	PALCE22V10-15KMB
	3/	PALCE22V10H-15E4/BKA
	0C7V7	QPC22V10-15/BKA
5962-89841053A	3/	PALC22V10D-15LMB
	3/	PALCE22V10-15LMB
	1FN41	ATF22V10B-15NM/883
	3/	PALCE22V10H-15E4/B3A
5962-8984106LA	65786	PALC22V10D-10DMB
	65786	PALCE22V10-10DMB
	66675	GAL22V10C-10LD/883C
	66675	GAL22V10D-10LD/883C
	1FN41	ATF22V10B-10GM/883
5962-8984106KA	65786	PALC22V10D-10KMB
	65786	PALCE22V10-10KMB
5962-89841063A	65786	PALC22V10D-10LMB
	65786	PALCE22V10-10LMB
	66675	GAL22V10C-10LR/883C
	66675	GAL22V10D-10LR/883C
	1FN41	ATF22V10B-10NM/883

See footnote at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8984107LA	3/	PALC22V10D-30DMB
	3/	PALCE22V10-30DMB
	0C7V7	QPC22V10-30/BLA
5962-8984107KA	3/	PALC22V10D-30KMB
	3/	PALCE22V10-30KMB
	0C7V7	QPC22V10-30/BKA
5962-89841073A	3/	PALC22V10D-30LMB
	3/	PALCE22V10-30LMB
	0C7V7	QPC22V10-30/B3A
5962-8984108LA	65786	PALC22V10D-20DMB
	65786	PALCE22V10-20DMB
	0C7V7	QPC22V10-20/BLA
5962-8984108KA	65786	PALC22V10D-20KMB
	65786	PALCE22V10-20KMB
	0C7V7	QPC22V10-20/BKA
5962-89841083A	65786	PALC22V10D-20LMB
	65786	PALCE22V10-20LMB
	0C7V7	QPC22V10-20/B3A
5962-8984109LA	3/	PALC22V10D-15DMB
	3/	PALCE22V10-15DMB
	0C7V7	QPC22V10-15/BLA
5962-8984109KA	3/	PALC22V10D-15KMB
	3/	PALCE22V10-15KMB
	0C7V7	QPC22V10-15/BKA
5962-89841093A	3/	PALC22V10D-15LMB
	3/	PALCE22V10-15LMB
	0C7V7	QPC22V10-15/B3A
5962-8984110LA	65786	PALC22V10D-25DMB
	65786	PALCE22V10-25DMB
	0C7V7	QPC22V10-25/BLA
5962-8984110KA	65786	PALC22V10D-25KMB
	65786	PALCE22V10-25KMB
	0C7V7	QPC22V10-25/BKA
5962-89841103A	65786	PALC22V10D-25LMB
	65786	PALCE22V10-25LMB
	0C7V7	QPC22V10-25/B3A
5962-8984111LA	3/	PALC22V10D-15DMB
	3/	PALCE22V10-15DMB
	0C7V7	QPC22V10-15/BLA
5962-8984111KA	3/	PALC22V10D-15KMB
	3/	PALCE22V10-15KMB
	0C7V7	QPC22V10-15/BKA

See footnote at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-89841113A	3/ 3/ 0C7V7	PALC22V10D-15LMB PALCE22V10-15LMB QPC22V10-15/B3A
5962-8984112LA	3/ 3/ 0C7V7	PALC22V10D-10DMB PALCE22V10-10DMB QPC22V10-10/BLA
5962-8984112KA	3/ 3/ 0C7V7	PALC22V10D-10KMB PALCE22V10-10KMB QPC22V10-10/BKA
5962-89841123A	3/ 3/ 0C7V7	PALC22V10D-10LMB PALCE22V10-10LMB QPC22V10-10/B3A
5962-8984113LA	3/	ATF22V10BQL-25GM/883
5962-89841133A	3/	ATF22V10BQL-25NM/883
5962-8984114LA	3/	ATF22V10BQL-20GM/883
5962-89841143A	3/	ATF22V10BQL-20NM/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ No longer available from an approved source of supply.

Vendor CAGE number	Vendor name and address
66675	Lattice Semiconductor Corporation 5555 NE Moore Court Hillsboro, OR 97124-6421
65786	Cypress Semiconductor Corporation 3901 North First Street San Jose, CA 95134
1FN41	Atmel Corporation 2325 Orchard Parkway San Jose, CA 95131
6S055	DPA Laboratories 2251 Ward Ave. Simi Valley, CA 93065
0C7V7	QP Laboratories 3605 Kifer Road Santa Clara, CA 95051