

CMOS 16-Bit Microcontrollers TMP91FY12AF

1. Outline and Features

TMP91FY12AF is a high-speed 16-bit microcontroller designed for the control of various mid- to large-scale equipment.

TMP91FY12AF comes in a 100-pin flat package.

Listed below are the features.

- (1) High-speed 16-bit CPU (900/L1 CPU)
 - Instruction mnemonics are upward-compatible with TLCS-90/900
 - 16 Mbytes of linear address space
 - General-purpose registers and register banks
 - 16-bit multiplication and division instructions; bit transfer and arithmetic instructions
 - Micro DMA: 4 channels (1.0 μ s/2 bytes at 16 MHz)
- (2) Minimum instruction execution time: 148 ns (at 27 MHz)
- (3) Built-in RAM: 4 Kbytes
Built-in ROM: 256 Kbytes Flash memory
2 Kbytes mask ROM (used for booting)
- (4) External memory expansion
 - Expandable up to 16 Mbytes (shared program/data area)
 - Can simultaneously support 8-/16-bit width external data bus
... Dynamic data bus sizing
- (5) 8-bit timers: 8 channels
- (6) 16-bit timer/event counter: 2 channels
- (7) General-purpose serial interface: 2 channels
 - UART/Synchronous mode: 2 channels
 - IrDA ver 1.0 (115.2 kbps) supported: 1 channel

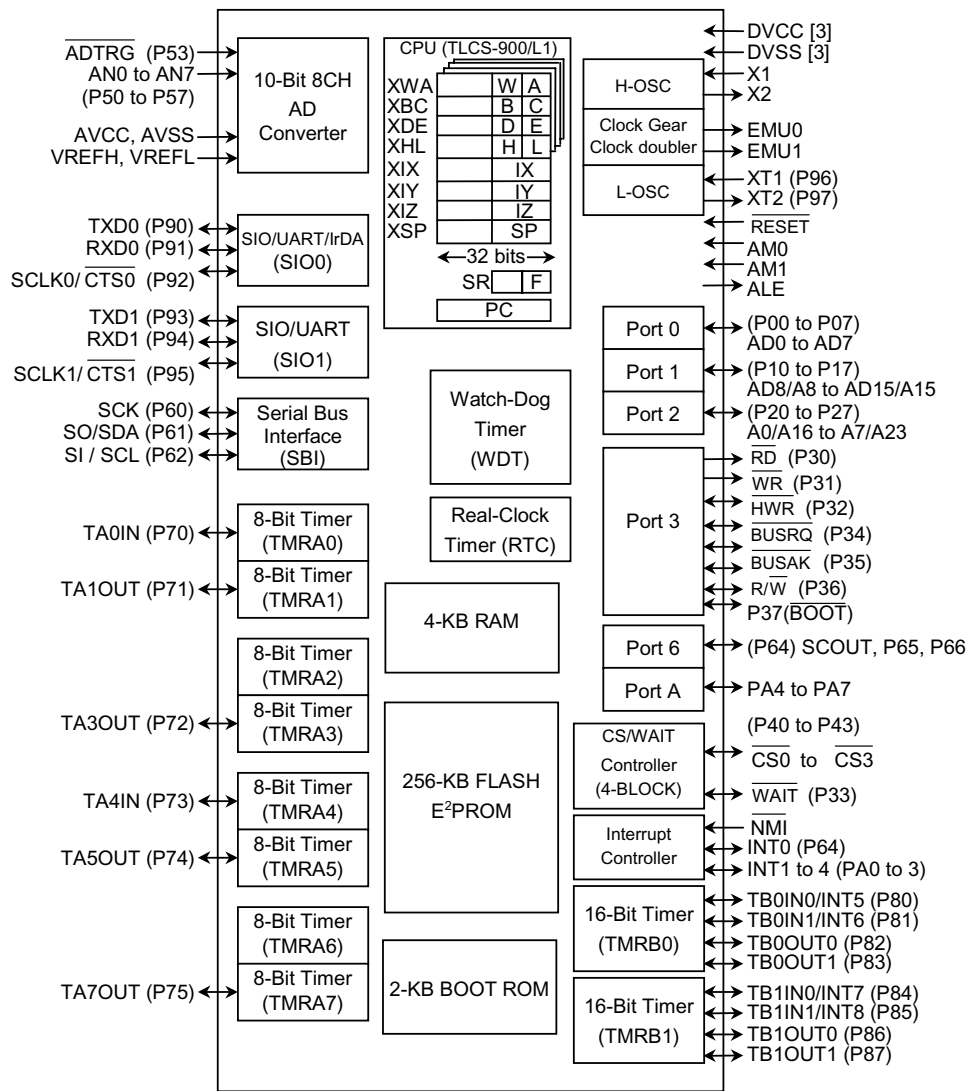
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- (8) Serial bus interface: 1 channel
 - I²C bus mode/clock synchronous select mode
- (9) 10-bit AD converter (sample-hold circuit is built in): 8 channels
- (10) Watchdog timer
- (11) Timer for real-time clock (RTC)
- (12) Chip Select/Wait controller: 4 channels
- (13) Interrupts: 45 interrupts
 - 9 CPU interrupts: Software interrupt instruction and illegal instruction
 - 26 internal interrupts: 7-level priority can be set.
 - 10 external interrupts: 7-level priority can be set.
- (14) Input/output ports: 81 pins
- (15) Standby function
 - Three Halt modes: Idle2 (programmable), Idle1, Stop
- (16) Triple-clock controller
 - Clock Doubler (DFM)
 - Clock Gear (f_c to $f_c/16$)
 - Slow mode ($f_s = 32.768$ kHz)
- (17) Operating voltage
 - $V_{CC} = 2.7$ V to 3.6 V (f_c max = 27 MHz)
- (18) Package
 - 100-pin QFP: P-QFP100-1414-0.50E



(): Initial function after reset

Figure 1.1 TMP91FY12AF Block Diagram

2. Pin Assignment and Pin Functions

The assignment of input/output pins for the TMP91FY12AF, their names and functions are as follows:

2.1 Pin Assignment Diagram

Figure 2.1.1 shows the pin assignment of the TMP91FY12AF.

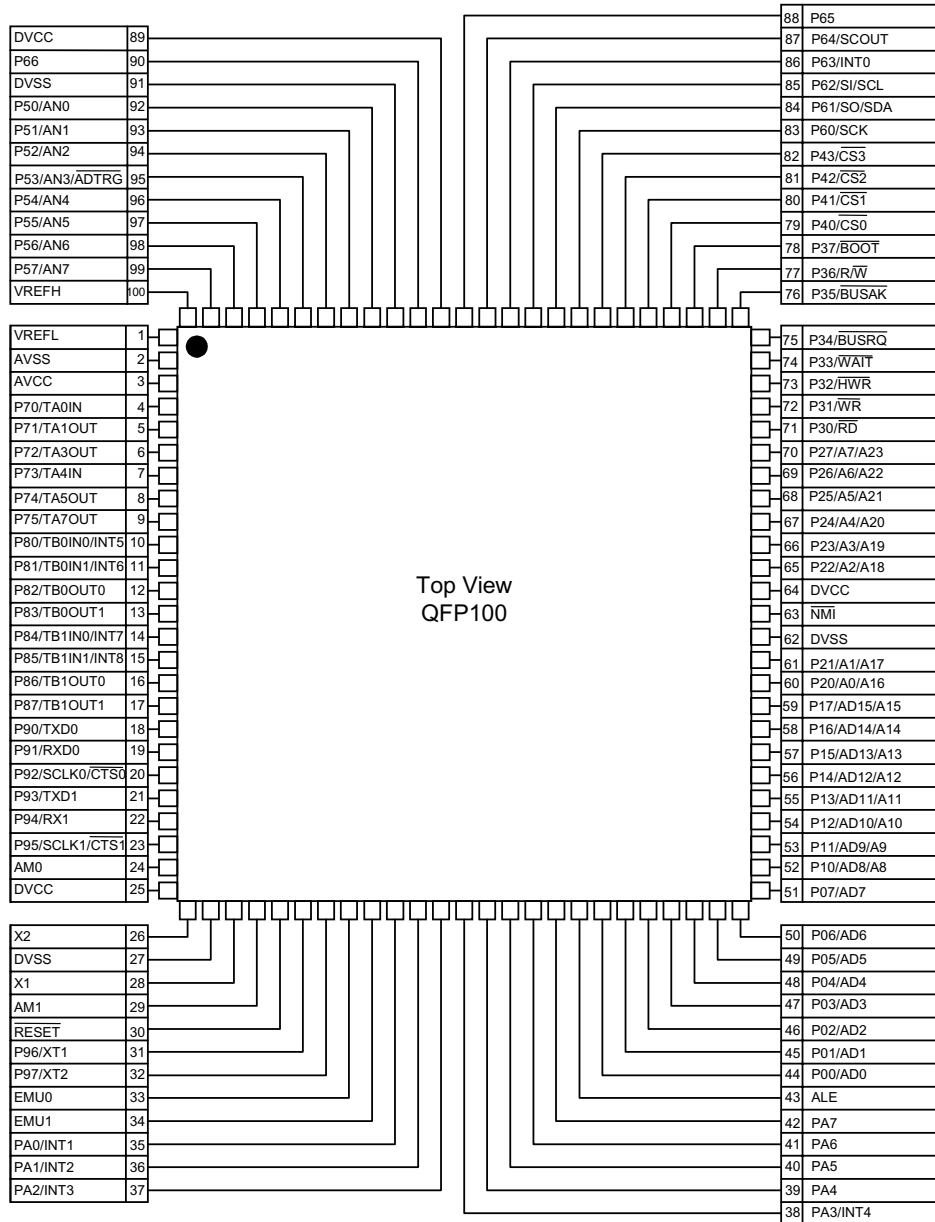


Figure 2.1.1 Pin assignment diagram (100-pin QFP)

2.2 Pin Names and Functions

The names of the input/output pins and their functions are described below.

Table 2.2.1 Pin names and functions.

Table 2.2.1 Pin names and functions (1/3)

Pin Name	Number of Pins	I/O	Functions
P00 to P07 AD0 to AD7	8	I/O Tri-state	Port 0: I/O port that allows I/O to be selected at the bit level Address and data (lower): Bits 0 to 7 of address and data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O Tri-state Output	Port 1: I/O port that allows I/O to be selected at the bit level Address and data (upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows I/O to be selected at the bit level (with pull-down resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 \overline{RD}	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 \overline{WR}	1	Output Output	Port 31: Output port Write: Strobe signal for writing data to pins AD0 to AD7
P32 \overline{HWR}	1	I/O Output	Port 32: I/O port (with pull-up resistor) High Write: Strobe signal for writing data to pins AD8 to AD15
P33 \overline{WAIT}	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 \overline{BUSRQ}	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus Request: Signal used to request Bus Release
P35 \overline{BUSAK}	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus Acknowledge: Signal used to acknowledge Bus Release
P36 R/ \overline{W}	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/Write: 1 represents Read or Dummy cycle; 0 represents Write cycle.
P37 \overline{BOOT}	1	I/O Input	Port 37: I/O port (with pull-up resistor) This pin sets single boot mode.
P40 $\overline{CS0}$	1	I/O Output	Port 40: I/O port (with pull-up resistor) Chip Select 0: Outputs 0 when address is within specified address area
P41 $\overline{CS1}$	1	I/O Output	Port 41: I/O port (with pull-up resistor) Chip Select 1: Outputs 0 if address is within specified address area
P42 $\overline{CS2}$	1	I/O Output	Port 42: I/O port (with pull-up resistor) Chip Select 2: Outputs 0 if address is within specified address area
P43 $\overline{CS3}$	1	I/O Output	Port 43: I/O port (with pull-up resistor) Chip Select 3: Outputs 0 if address is within specified address area
P50 to P57 AN0 to AN7 \overline{ADTRG}	8	Input Input Input	Port 5: pin used to input port Analog input: Pin used to input to AD converter AD Trigger: Signal used to request start of AD converter
P60 SCK	1	I/O I/O	Port 60: I/O port Serial bus interface clock in SIO Mode
P61 SO SDA	1	I/O Output I/O	Port 61: I/O port Serial bus interface output data in SIO Mode Serial bus interface data in I ² C bus Mode
P62 SI SCL	1	I/O Input I/O	Port 62: I/O port Serial bus interface input data in SIO Mode Serial bus interface clock in I ² C bus Mode
P63 INT0	1	I/O Input	Port 63: I/O port Interrupt Request Pin 0: Interrupt request pin with programmable level / rising edge / falling edge
P64 SCOUT	1	I/O Output	Port 64: I/O port System Clock Output: Outputs f_{PPH} or fs clock.

Table 2.2.1 Pin names and functions (2/3)

Pin Name	Number of Pins	I/O	Functions
P65	1	I/O	Port 65: I/O port
P66	1	I/O	Port 66: I/O port
P70 TA0IN	1	I/O Input	Port 70: I/O port Timer A0 Input
P71 TA1OUT	1	I/O Output	Port 71: I/O port Timer A1 Output
P72 TA3OUT	1	I/O Output	Port 72: I/O port Timer A3 Output
P73 TA4IN	1	I/O Input	Port 73: I/O port Timer A4 Input
P74 TA5OUT	1	I/O Output	Port 74: I/O port Timer A5 Output
P75 TA7OUT	1	I/O Output	Port 75: I/O port Timer A7 Output
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: I/O port Timer B0 Input 0 Interrupt Request Pin 5: Interrupt request pin with programmable rising edge / falling edge.
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: I/O port Timer B0 Input 1 Interrupt Request Pin 6: Interrupt request on rising edge
P82 TB0OUT0	1	I/O Output	Port 82: I/O port Timer B0 Output 0
P83 TB0OUT1	1	I/O Output	Port 83: I/O port Timer B0 Output 1
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: I/O port Timer B1 Input 0 Interrupt Request Pin 7: Interrupt request pin with programmable rising edge / falling edge.
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: I/O port Timer B1 Input 1 Interrupt Request Pin 8: Interrupt request on rising edge
P86 TB1OUT0	1	I/O Output	Port 86: I/O port Timer B1 Output 0
P87 TB1OUT1	1	I/O Output	Port 87: I/O port Timer B1 Output 1
P90 TXD0	1	I/O Output	Port 90: I/O port Serial Send Data 0 (Programmable open-drain)
P91 RXD0	1	I/O Input	Port 91: I/O port Serial Receive Data 0
P92 SCLK0 CTS0	1	I/O I/O Input	Port 92: I/O port Serial Clock I/O 0 Serial Data Send Enable 0 (Clear to Send)
P93 TXD1	1	I/O Output	Port 93: I/O port Serial Send Data 1 (Programmable open-drain)
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial Receive Data 1
P95 SCLK1 CTS1	1	I/O I/O Input	Port 95: I/O port (with pull-up resistor) Serial Clock I/O 1 Serial Data Send Enable 1 (Clear to Send)
P96 XT1	1	I/O Input	Port 96: I/O port (Open-drain output) Low-frequency oscillator connection pin

Table 2.2.1 Pin names and functions (3/3)

Pin Name	Number of Pins	I/O	Functions
P97 XT2	1	I/O Output	Port 97: I/O port (Open-drain output) Low-frequency oscillator connection pin
PA0 to PA3 INT1 to INT4	4	I/O Input	Ports A0 to A3: I/O ports Interrupt Request Pins 1 to 4: Interrupt request pins with programmable rising edge / falling edge.
PA4 to PA7	4	I/O	Ports A4 to A7: I/O ports
ALE	1	Output	Address Latch Enable Can be disabled to reduce noise.
$\overline{\text{NMI}}$	1	Input	Non-Maskable Interrupt Request Pin: Interrupt request pin with programmable falling edge or both edge.
AM0 to 1	2	Input	Address Mode: The Vcc pin should be connected.
EMU0/EMU1	1	Output	Test Pins: Open pins
$\overline{\text{RESET}}$	1	Input	Reset: initializes TMP91FY12A. (With pull-up resistor)
VREFH	1	Input	Pin for reference voltage input to AD converter (H)
VREFL	1	Input	Pin for reference voltage input to AD converter (L)
AVCC	1	I/O	High-frequency oscillator connection pins
AVSS	1		Power supply pin for AD converter
X1/X2	2		GND pin for AD converter (0 V)
DVCC	3		Power supply pins (All VCC pins should be connected with the power supply pin.)
DVSS	3		GND pins (0 V) (All VSS pins should be connected with the power supply pin.)

Note: An external DMA controller cannot access the device's built-in memory or built-in I/O devices using the $\overline{\text{BUSRQ}}$ and $\overline{\text{BUSAK}}$ signal.

3. Functional Description

This section shows the hardware configuration of the TMP91FY12A and explains how it operates.


This device is a version of the created by replacing the predecessor's internal mask ROM with a 256-Kbyte internal flash memory. The configuration and the functionality of this device are the same as those of the TMP91CW12A. For the functions of this device that are not described here, refer to the TMP91CW12A data sheet.

3.1 Outline of operation modes

There are single-chip and single-boot modes. Which mode is selected depends on the device's pin state after a reset (including when the watchdog timer output is connected to reset (inside the chip)).

- Single Chip Mode: The device normally operates in this mode. After a reset, the device starts executing the internal flash memory program.
- Single Boot Mode: This mode is used to rewrite the internal flash memory by serial transfer (UART). After a reset, the internal boot ROM starts up, executing a on-board rewrite program.

Table 3.1.1 Operation Mode Setup table

Operation Mode	Mode Setup Input Pin			
	RESET	BOOT (P37)	AM0	AM1
Single-chip mode		H	H	H
Single-boot mode		L		

3.2 Memory Map

The memory map of this device differs from that of the TMP91CW12A.

Figure 3.2.1 shows a memory map of the device in single-chip mode and its memory areas that can be accessed in each addressing mode of the CPU.

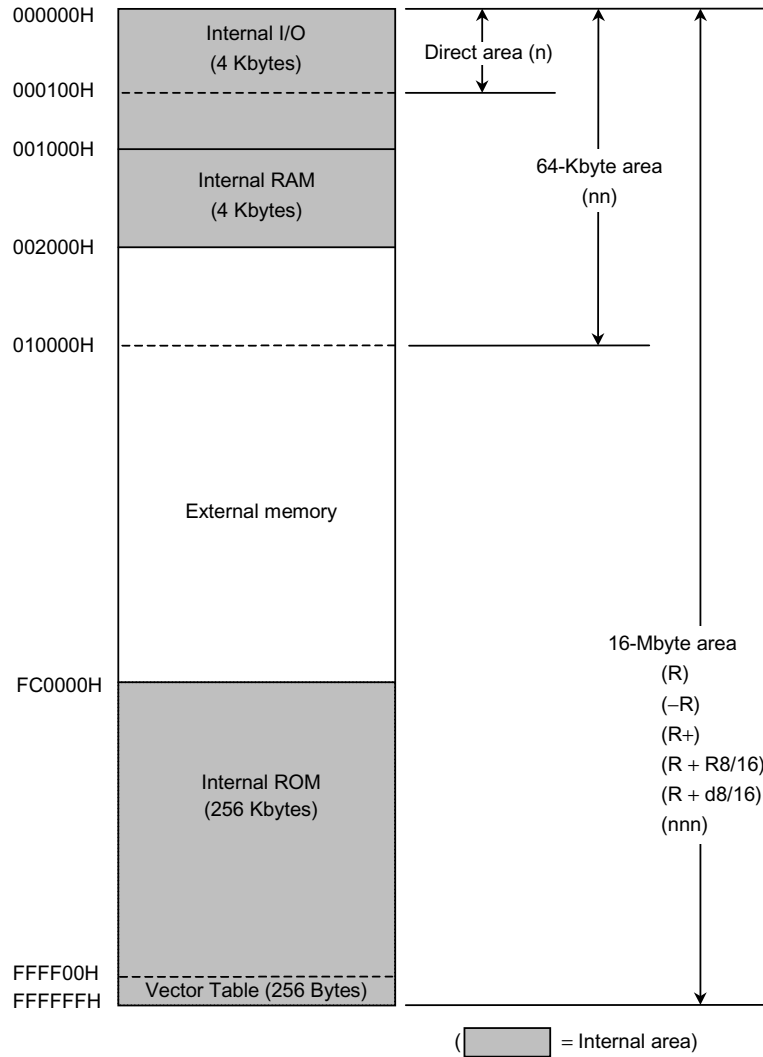


Figure 3.2.1 Memory Map (Single-chip Mode)

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	-0.5 to 4.0	V
Input Voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
Output Current	I _{OL}	2	mA
Output Current	I _{OH}	-2	mA
Output Current (total)	ΣI _{OL}	80	mA
Output Current (total)	ΣI _{OH}	-80	mA
Power Dissipation (T _a = 85°C)	PD	600	mW
Soldering Temperature (10 s)	T _{SOLDER}	260	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	T _{OPR}	-20 to 70	°C
Number of Times Program Erase	N _{EW}	10000	Cycle

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2)

Parameter	Symbol	Condition		Min	Typ. (Note 1)	Max	Unit
Power Supply Voltage ($V_{CC} = DV_{CC}$) ($V_{SS} = DV_{SS} = 0\text{ V}$)	V_{CC}	$f_c = 4\text{ to }27\text{ MHz}$	$f_s = 30\text{ to }34\text{ kHz}$	2.7		3.6	V
Input Low Voltage	P00 to P17 (AD0 to 15)	V_{IL}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	-0.3		0.6	V
	P20 to PA7 (except P63)	V_{IL1}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$		$0.3 V_{CC}$		
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P63 (INT0)	V_{IL2}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$		$0.25 V_{CC}$		
	AM0, 1	V_{IL3}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$		0.3		
	X1	V_{IL4}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$		$0.2 V_{CC}$		
Input High Voltage	P00 to P17 (AD0 to 15)	V_{IH}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	2.0		$V_{CC} + 0.3$	V
	P20 to PA7 (except P63)	V_{IH1}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	$0.7 V_{CC}$			
	$\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P63 (INT0)	V_{IH2}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	$0.75 V_{CC}$			
	AM0, 1	V_{IH3}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	$V_{CC} - 0.3$			
	X1	V_{IH4}	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	$0.8 V_{CC}$			
Output Low Voltage	V_{OL}	$I_{OL} = 1.6\text{ mA}$	$V_{CC} = 2.7\text{ to }3.6\text{ V}$			0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\text{ }\mu\text{A}$	$V_{CC} = 2.7\text{ to }3.6\text{ V}$	2.4			

Note 1: Typical values are for when $T_a = 25^\circ\text{C}$ and $V_{CC} = 3.0\text{ V}$ unless otherwise noted.

4.2 DC Characteristics (2/2)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Input Leakage Current)	ILI	$0.0 \leq V_{IN} \leq V_{CC}$		0.02	± 5	μA
Output Leakage Current	ILO	$0.2 \leq V_{IN} \leq V_{CC} - 0.2$		0.05	± 10	
Power Down Voltage (at STOP, RAM back-up)	VSTOP	$V_{IL2} = 0.2 V_{CC}$, $V_{IH2} = 0.8 V_{CC}$	2.7		3.6	V
RESET Pull-up Resistor	RRST	$V_{CC} = 3 V \pm 10\%$	100		400	K Ω
Pin Capacitance	CIO	$f_c = 1 \text{ MHz}$			10	PF
Schmitt Width RESET, NMI, INTO	VTH	$V_{CC} = 2.7 \text{ to } 3.6 \text{ V}$	0.4	1.0		V
Programmable Pull-up Resistor	RKH	$V_{CC} = 3 V \pm 10\%$	100		400	K Ω
Normal (Note 2)	I _{CC}	$V_{CC} = 3 V \pm 10\%$ $f_c = 27 \text{ MHz}$		30.0	45.0	mA
Idle2				4.5	7.0	
Idle1				2.0	4.0	
Slow (Note 2)		$V_{CC} = 3 V \pm 10\%$ $f_s = 32.768 \text{ kHz}$		30.0	40	μA
Idle2				9.0	25	
Idle1				6.0	15	
Stop		$V_{CC} = 3 V \pm 10\%$		1.0	15	μA

Note 1: Typical values are for when $T_a = 25^\circ C$ and $V_{CC} = 3.0 \text{ V}$ unless otherwise noted.

Note 2: I_{CC} measurement conditions (Normal, Slow):

All functions are operating; output pins are open and input pins are fixed.

4.3 AC Characteristics

(1) $V_{CC} = 3.0 \text{ V} \pm 10\%$

No.	Parameter	Symbol	Variable		$f_{FPH} = 27 \text{ MHz}$		Unit
			Min	Max	Min	Max	
1	f_{FPH} Period (= x)	t_{FPH}	37.0	31250	37.0		ns
2	A0 to A15 Valid → ALE Fall	t_{AL}	$0.5x - 6$		12		ns
3	ALE Fall → A0 to A15 Hold	t_{LA}	$0.5x - 16$		2		ns
4	ALE High Width	t_{LL}	$x - 20$		17		ns
5	ALE Fall → \overline{RD} / \overline{WR} Fall	t_{LC}	$0.5x - 14$		4		ns
6	\overline{RD} Rise → ALE Rise	t_{CLR}	$0.5x - 10$		8		ns
7	\overline{WR} Rise → ALE Rise	t_{CLW}	$x - 10$		27		ns
8	A0 to A15 Valid → \overline{RD} / \overline{WR} Fall	t_{ACL}	$x - 23$		14		ns
9	A0 to A23 Valid → \overline{RD} / \overline{WR} Fall	t_{ACH}	$1.5x - 26$		29		ns
10	\overline{RD} Rise → A0 to A23 Hold	t_{CAR}	$0.5x - 13$		5		ns
11	\overline{WR} Rise → A0 to A23 Hold	t_{CAW}	$x - 13$		24		ns
12	A0 to A15 Valid → D0 to D15 Input	t_{ADL}		$3.0x - 38$		73	ns
13	A0 to A23 Valid → D0 to D15 Input	t_{ADH}		$3.5x - 41$		88	ns
14	\overline{RD} Fall → D0 to D15 Input	t_{RD}		$2.0x - 30$		44	ns
15	\overline{RD} Low Width	t_{RR}	$2.0x - 15$		59		ns
16	\overline{RD} Rise → D0 to A15 Hold	t_{HR}	0		0		ns
17	\overline{RD} Rise → A0 to A15 Output	t_{RAE}	$x - 15$		22		ns
18	\overline{WR} Low Width	t_{WW}	$1.5x - 15$		40		ns
19	D0 to D15 Valid → \overline{WR} Rise	t_{DW}	$1.5x - 35$		20		ns
20	\overline{WR} Rise → D0 to D15 Hold	t_{WD}	$x - 25$		12		ns
21	A0 to A23 Valid → \overline{WAIT} Input $\left[\begin{smallmatrix} 1 \text{ WAIT} \\ +n \text{ Mode} \end{smallmatrix} \right]$	t_{AWH}		$3.5x - 60$		69	ns
22	A0 to A15 Valid → \overline{WAIT} Input $\left[\begin{smallmatrix} 1 \text{ WAIT} \\ +n \text{ Mode} \end{smallmatrix} \right]$	t_{AWL}		$3.0x - 50$		61	ns
23	\overline{RD} / \overline{WR} Fall → \overline{WAIT} Hold $\left[\begin{smallmatrix} 1 \text{ WAIT} \\ +n \text{ Mode} \end{smallmatrix} \right]$	t_{CW}	$2.0x + 0$		74		ns
24	A0 to A23 Valid → Port Input	t_{APH}		$3.5x - 89$		40	ns
25	A0 to A23 Valid → Port Hold	t_{APH2}	$3.5x$		129		ns
26	A0 to A23 Valid → Port Valid	t_{AP}		$3.5x + 80$		209	ns

AC Measuring Conditions

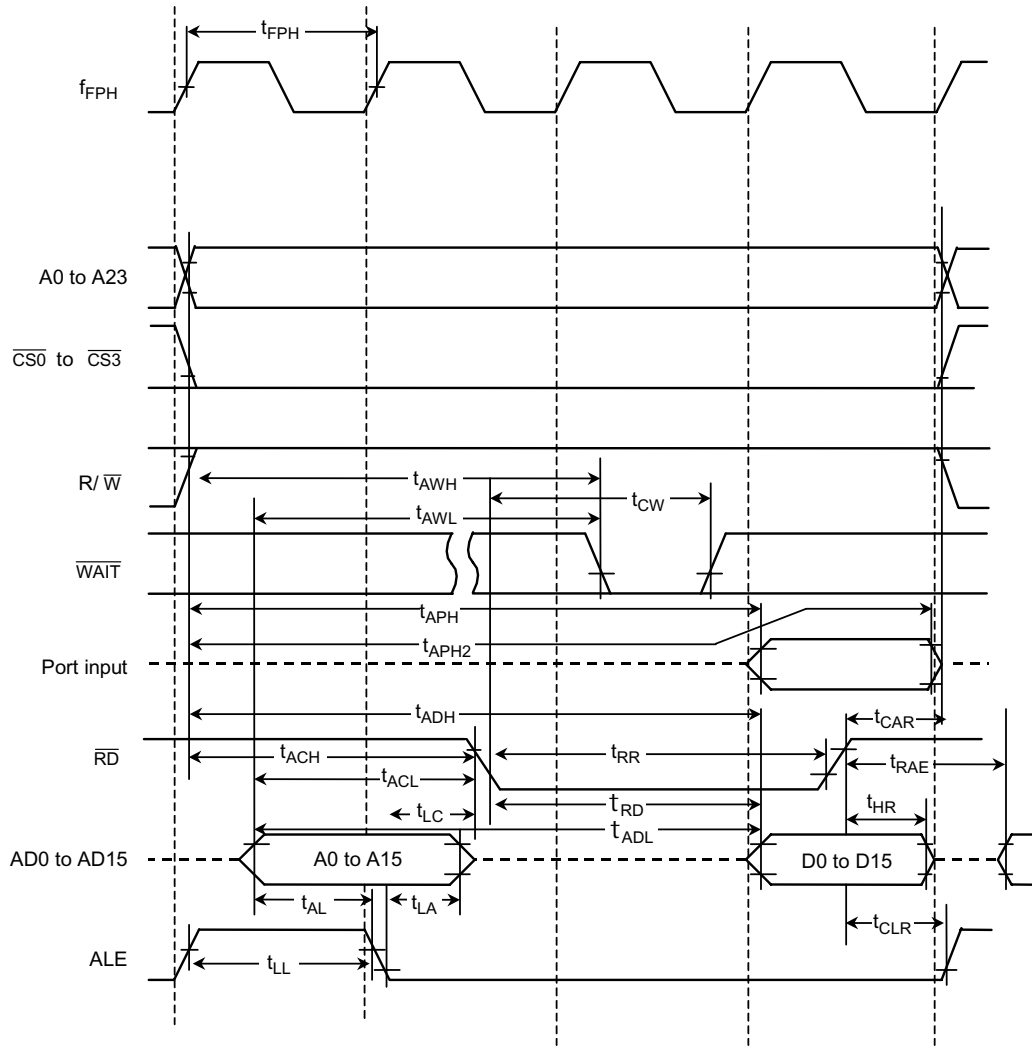
- Output Level: High = $0.7 \times V_{CC}$, Low = $0.3 \times V_{CC}$, CL = 50 pF
- Input Level: High = $0.9 \times V_{CC}$, Low = $0.1 \times V_{CC}$

Note: x used in an expression shows a frequency for the clock f_{FPH} selected by SYSCR1<SYSCK>.

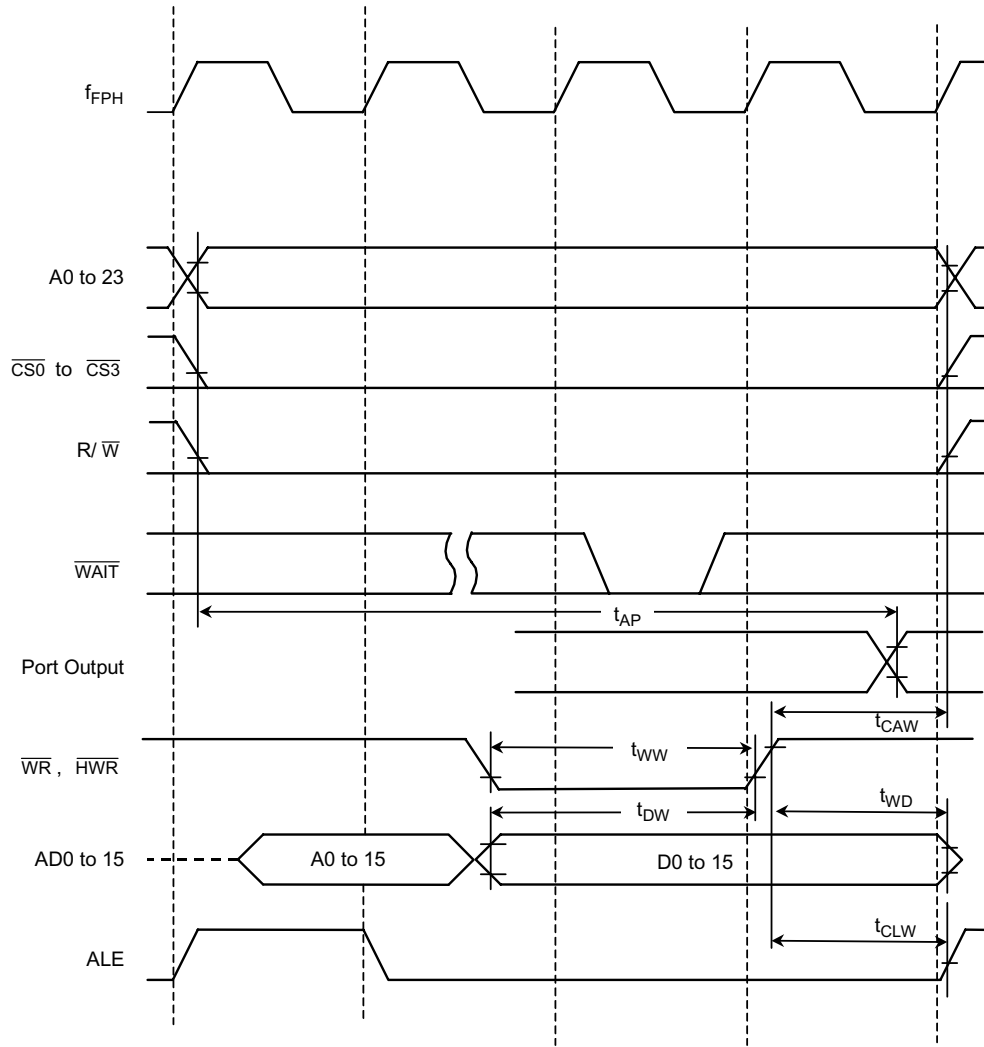
The value of x changes according to whether a clock gear or a low-speed oscillator is selected.

An example value is calculated for f_c , with gear = 1/ f_c (SYSCR1<SYSCK,GEAR2 to 0> = 0000) .

(2) Raed Cycle



(3) Write Cycle



4.4 AD Conversion Characteristics

AVCC = VCC, AVSS = VSS

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Analog Reference Voltage (+)	VREFH	$V_{CC} = 3\text{ V} \pm 10\%$	$V_{CC} - 0.2\text{ V}$	V_{CC}	V_{CC}	V
Analog Reference Voltage (-)	VREFL	$V_{CC} = 3\text{ V} \pm 10\%$	V_{SS}	V_{SS}	$V_{SS} + 0.2\text{ V}$	
Analog Input Voltage Range	VAIN		V_{REFL}		V_{REFH}	
Analog Current for Analog Reference Voltage <VREFON> = 1	IREF (VREFL = 0V)	$V_{CC} = 3\text{ V} \pm 10\%$		0.94	1.20	mA
<VREFON> = 0		$V_{CC} = 3\text{ V} \pm 10\%$		0.02	5.0	μA
Error (not including quantizing errors)	-	$V_{CC} = 3\text{ V} \pm 10\%$		± 1.0	± 4.0	LSB

Note 1: $1\text{ LSB} = (V_{REFH} - V_{REFL})/1024\text{ [V]}$

Note 2: The operation above is guaranteed for $f_{FPH} \geq 4\text{ MHz}$.

Note 3: The value for I_{CC} includes the current which flows through the AVCC pin.

4.5 Serial Channel Timing (I/O Internal Mode)

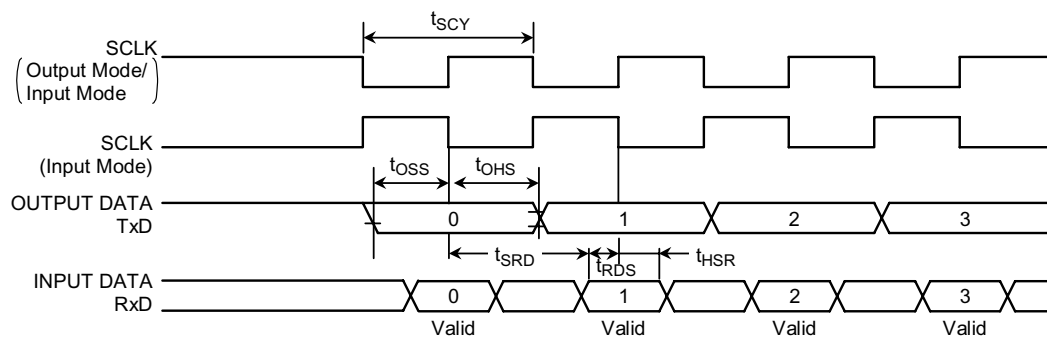
(1) SCLK Input Mode

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period	t_{SCY}	16X		1.6		0.59		μ s
Output Data → SCLK Rising /Falling Edge (Note)	t_{OSS}	$t_{SCY}/2 - 4X - 110$		290		38		ns
SCLK Rising/Falling Edge (Note) → Output Data Hold	t_{OHS}	$t_{SCY}/2 + 2x + 0$		1000		370		ns
SCLK Rising/Falling Edge (Note) → Input Data Hold	t_{HSR}	$3x + 10$		310		121		ns
SCLK Rising/Falling Edge (Note) → Valid Data Input	t_{SRD}		$t_{SCY} - 0$		1600		592	ns
Valid Data Input SCLK → Rising/Falling Edge (Note)	t_{RDS}	0		0		0		ns

Note : SCLK Rising/Falling Edge: The rising edge is used in SCLK Rising Mode.
The falling edge is used in SCLK Falling Mode.

(2) SCLK Output Mode

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Period (programmable)	t_{SCY}	16X	8192X	1.6	819	0.59	303	μ s
Output Data → SCLK Rising Edge	t_{OSS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising Edge → Output Data Hold	t_{OHS}	$t_{SCY}/2 - 40$		760		256		ns
SCLK Rising Edge → Input Data Hold	t_{HSR}	0		0		0		ns
SCLK Rising Edge → Valid Data Input	t_{SRD}		$t_{SCY} - 1x - 180$		1320		375	ns
Valid Data Input → SCLK Rising Edge	t_{RDS}	$1x + 180$		280		217		ns



4.6 Event Counter (TA0IN, TA4IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock Period	t_{VCK}	$8X + 100$		900		396		ns
Clock Low Level Width	t_{VCKL}	$4X + 40$		440		188		ns
Clock High Level Width	t_{VCKH}	$4X + 40$		440		188		ns

4.7 Interrupt and Capture

(1) \overline{NMI} , INT0 to INT4 Interrupts

Parameter	Symbol	Variable		10 MHz		27 MHz		Unit
		Min	Max	Min	Max	Min	Max	
\overline{NMI} , INT0 to INT4 Low level width	t_{INTAL}	$4X + 40$		440		188		ns
\overline{NMI} , INT0 to INT4 High level width	t_{INTAH}	$4X + 40$		440		188		ns

(2) INT5 to INT8 Interrupts, Capture

The INT5 to INT8 input width depends on the system clock and prescaler clock settings.

System Clock Selected <SYSCK>	Prescaler Clock Selected <PRCK1, PRCK0>	t_{INTBL} (INT5 to INT8 Low level Width)		t_{INTBH} (INT5 to INT8 High Level Width)		Unit
		Variable	$f_{FPH} = 27 \text{ MHz}$	Variable	$f_{FPH} = 27 \text{ MHz}$	
		Min	Min	Min	Min	
0 (f_c)	00 (f_{FPH})	$8X + 100$	396	$8X + 100$	396	ns
	10 ($f_c/16$)	$128X_c + 0.1$	4.8	$128X_c + 0.1$	4.8	μs
1 (f_s)	00 (f_{FPH})	$8X + 0.1$	244.3	$8X + 0.1$	244.3	

Note: X_c = Period of Clock f_c

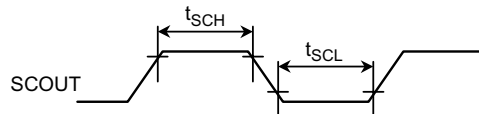
4.8 SCOUT Pin AC Characteristics

Parameter	Symbol	Variable		10 MHz		27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Low level Width	t_{SCH}	$0.5T - 13$		37		5		$V_{cc} = 2.7 \text{ to } 3.6 \text{ V}$	ns
High level Width	t_{SCL}	$0.5T - 13$		37		5		$V_{cc} = 2.7 \text{ to } 3.6 \text{ V}$	ns

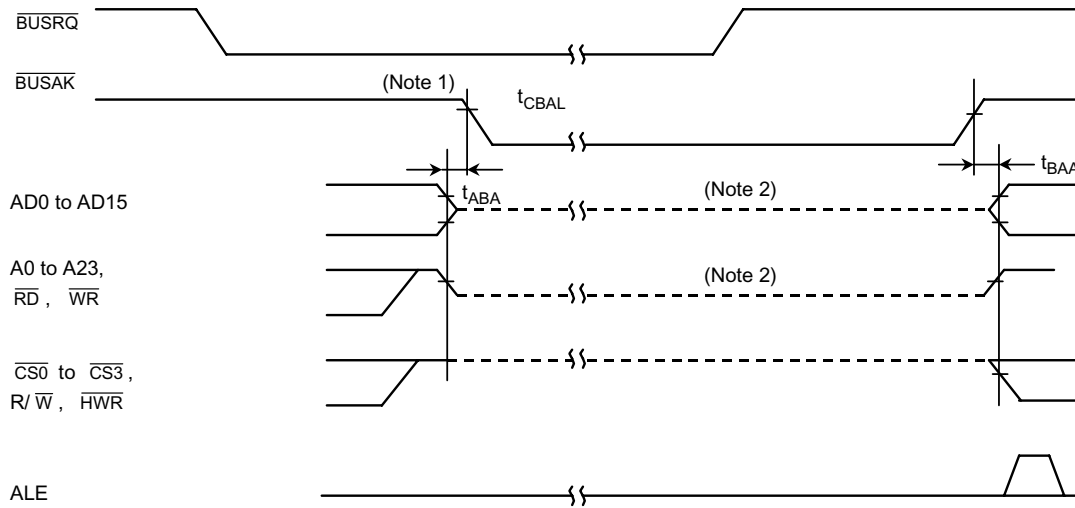
Note: T = Period of SCOUT

Measurement Condition

- Output Level: High 0.7 V_{cc} /Low 0.3 V_{cc} , $CL = 10\text{pF}$



4.9 Bus Request/Bus Acknowledge



Parameter	Symbol	Variable		f _{FPH} = 10 MHz		f _{FPH} = 27 MHz		Condition	Unit
		Min	Max	Min	Max	Min	Max		
Output Buffer Off to $\overline{\text{BUSAK}}$ Low	t_{ABA}	0	80	0	80	0	80	V _{CC} = 2.7 to 3.6 V	ns
$\overline{\text{BUSAK}}$ High to Output Buffer On	t_{BAA}	0	80	0	80	0	80	V _{CC} = 2.7 to 3.6 V	ns

Note 1: Even if the $\overline{\text{BUSRQ}}$ Signal goes Low, the bus will not be released while the $\overline{\text{WAIT}}$ signal is Low. The bus will only be released when $\overline{\text{BUSRQ}}$ goes Low while $\overline{\text{WAIT}}$ is High.

Note 2: This line shows only that the output buffer is in the Off state.

It does not indicate that the signal level is fixed.

Just after the bus is released, the signal level set before the bus was released is maintained dynamically by the external capacitance. Therefore, to fix the signal level using an external resistor during bus release, careful design is necessary, since fixing of the level is delayed.

The internal programmable pull-up/pull-down resistor is switched between the Active and Non-Active states by the internal signal.

4.10 Recommended Oscillation Circuit

The TMP91FY12AF has been evaluated by the following resonator manufacturer. The evaluation results are shown below for your information.

Note: The load capacitance of the oscillation terminal is the sum of the load capacitances of C1 and C2 to be connected and the stray capacitance on the board. Even if the ratings of C1 and C2 are used, the load capacitance varies with each board and the oscillator may malfunction. Therefore, when designing a board, make the pattern around the oscillation circuit shortest. It is recommended that final evaluation of the resonator be performed on the board.

(1) Examples of resonator connection

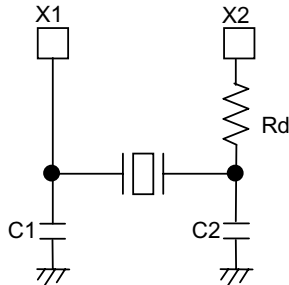


Figure 4.10.1 High-frequency Oscillator Connection

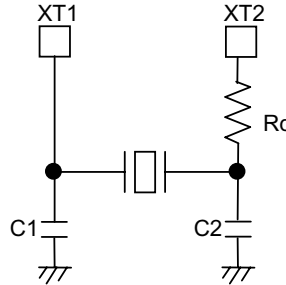


Figure 4.10.2 Low-frequency Oscillator Connection

(2) Recommended ceramic resonators for the TMP91FY12AF: Murata Manufacturing Co., Ltd.

Ta = -40 to 85°C

Item	Oscillation frequency [MHz]	Recommended resonator	Recommended rating			VCC [V]	Remarks
			C1 [pF]	C2 [pF]	Rd [kΩ]		
High-frequency oscillator	4.0	CSTS0400MG06	(47)	(47)	0	2.7 to 3.3	—
	6.75	CSTS0675MG06	(47)	(47)			
	12.5	CSA12.5MTZ	30	30			
		CST12.5MTW	(30)	(30)			
	20.0	CSA20.00MXZ040	7	7			
		CSA27.00MXZ040	5	5			
		CST27.00MXW040	(5)	(5)			

- The values enclosed in brackets in the C1 and C2 columns apply to the condenser built-in type.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL;
<http://www.murata.co.jp/search/index.html>

