

PFC-DCM

TDA4817

Power Factor Controller
IC for Higher Power Factor and
Active Harmonic Filtering

Power Management & Supply



Never stop thinking.

Previous Version:

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Power Factor Controller
IC for High Power Factor and
Active Harmonic Filtering

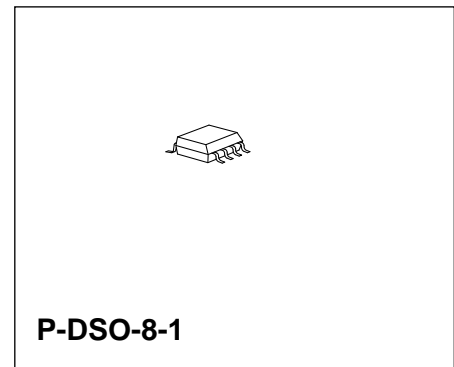
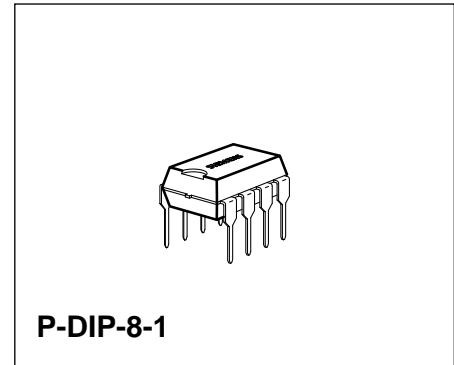
TDA 4817

Advance Information

Bipolar IC

Features

- IC for sinusoidal line-current consumption
- Power factor approaching 1
- Controls boost converter as an active harmonics filter
- Direct drive of SIPMOS transistor
- Zero crossing detector for discontinuous operation mode with variable frequency
- 110/220 V AC operation without switchover
- Standby current consumption of 0.5 mA



Type	Ordering Code	Package
▼ TDA 4817	Q67000-A8298	P-DIP-8-1
▼ TDA 4817 G	Q67000-A8299	P-DSO-8-1 (SMD)

▼ = New type

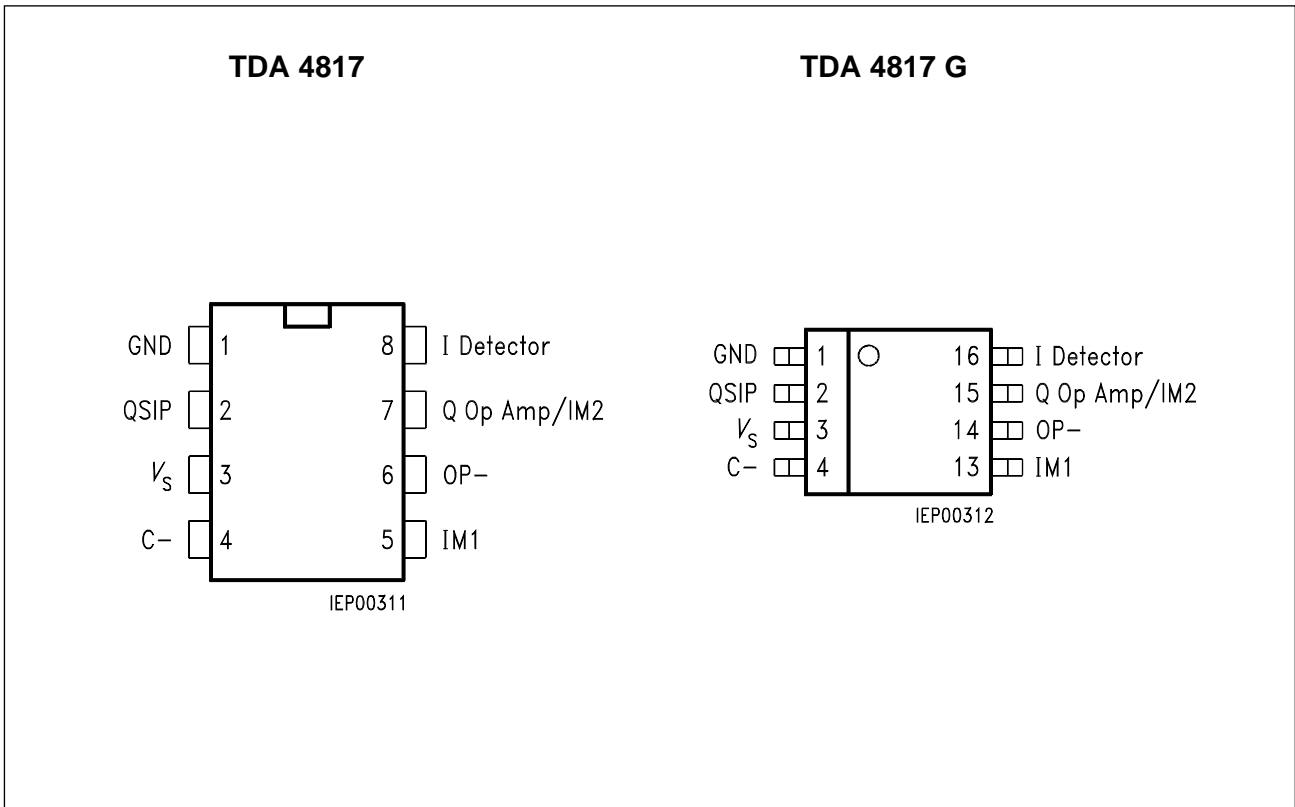
The TDA 4817 contains all functions for designing electronic ballasts and switched-mode power supplies with sinusoidal line current consumption and a power factor approaching 1.

The TDA 4817 controls a boost converter as an active harmonic filter in a discontinuous (triangular shaped current) mode with variable frequency.

A typical application is in electronic ballasts, especially when a large number of such lamps are concentrated on one line supply point.

The output voltage of this filter is regulated with high efficiency. Therefore the device can be easily operated on different line voltages (110/220 V_{AC}) without any switchover.

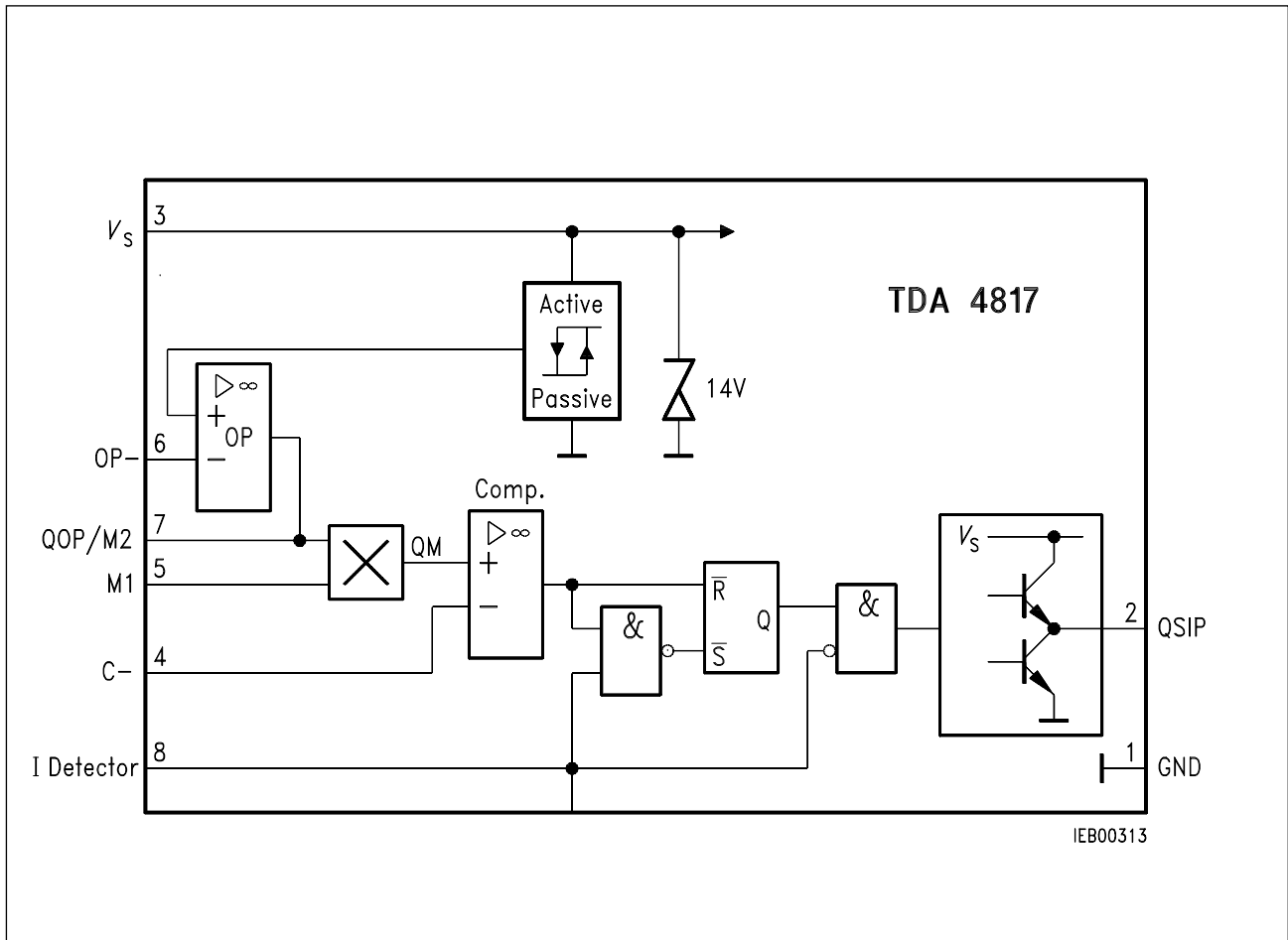
The TDA 4817 is an 8-pin-economy-version of the TDA 4814 A without reference voltage output and start/stop monitoring circuit.



Pin Configurations
(top view)

Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	QSIP	Driver output
3	V_S	Supply voltage
4	C –	Comparator input
5	IM1	Multiplier input
6	OP –	Input
7	QOP/IM2	Operational-amplifier output QOP and multiplier input M2
8	I Detector	Detector input



Block Diagram

Circuit Description

This device has a conditioning circuit for the internal power supply. It allows standby operation with very low current consumption (less than 0.5 mA), a hysteresis between enable and switch-off levels and an internal voltage stabilization. An integrated Z-diode limits the voltage on V_S , when impressed current is fed.

The **output driver (Q SIP)** is controlled by detector input and current comparator.

The **detector input (I DET)** which is highly resistive in the operating state reacts on hysteresis-determined voltage levels. To keep down the amount of circuitry required, clamping diodes are provided which allow control by a current source.

The operating state of the boost converter choke is sensed via the detector input. H-level means that the choke discharges and the output driver is inhibited. H-level sets a flip-flop, which stores the switch-off instruction of the current comparator to reduce susceptibility to interference. As soon as demagnetization is finished the choke voltage reverses and the detector input is set to L-level, thus enabling the output driver. This ensures that the choke is always currentless when the SIPMOS transistor switches on and that no current gaps appear.

The nominal voltage of the multiplier output is compared to the voltage derived from the actual line current (**- I COMP**), thus setting the switch-off threshold of the comparator. The current comparator blocks the output driver when the nominal peak value of the choke current given by the multiplier output is reached.

This state is maintained in the flip-flop until H-level appears at detector input which takes over the hold function and resets the flip-flop.

Operating states might occur without any useful detector signal. This is the case with magnetic saturation of the choke and when the input voltage approaches or exceeds the output voltage as, for example, during switch-on. The driver remains inhibited for the flip-flop due to the absent set signal.

The trigger signal can be derived from the subsequent lamp generator or a SMPS control device. The trigger signal level should be so low that with standard operation the signal from the detector winding dominates. The multiplier delivers the preset nominal value for the current comparator by multiplying the input voltage (**IM1**), which determines the nominal waveform and the output voltage of the control amplifier.

The control amplifier stabilizes the output dc voltage of the active harmonic filter in the event of load and input voltage changes. The **control amplifier** compares the actual output voltage to a reference voltage which is provided in the IC and stable with temperature.

Output Driver

The output driver is intended to drive a SIPMOS transistor directly.

It is designed as a push-pull stage.

Both the capacitive input impedance and keeping the gate level at zero potential in standby operation by an internal 10-k Ω -resistor are taken into account. Possible effects on the output driver by line inductances or capacitive couplings via SIPMOS transistor Miller capacitance are limited by diodes connected to ground and supply voltage.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply voltage	V_S	- 0.3		V_Z	V	$V_Z = Z$ -voltage
Inputs	$V_C -$	- 0.3		20	V	
Comparator	$V_{OP} -$	- 0.3		20	V	
Operational amplifier	V_{M1}	- 0.3		20	V	
Multiplier						
Output OP	V_{QOP}	- 0.3		6	V	
Z-current V_S -GND	I_Z	0		100	mA	Observe P_{max}
Driver output QSIP	V_{QSIP}	- 0.3		V_S	V	
QSIP clamping diodes	I_{QSIP}	- 10		10	mA	$V_{QSIP} > V_S$ or $V_{QSIP} < - 0.3$ V
Detector input	V_{Det}	0.9		6	V	
Detector clamping diodes	I_{Det}	- 10		10	mA	$V_{Det} > 6$ V or $V_{Det} < 0.9$ V
Junction temperature	T_j			150	°C	
Storage temperature	T_{stg}	- 55		125	°C	
Thermal resistance						
system-air						
TDA 4817	$R_{th SA}$			100	K/W	P-DIP-8 package
TDA 4817 G	$R_{th SA}$			170	K/W	P-DSO-8 package

Operating Range

Supply voltage	V_S	V_{Son}		V_Z	V	¹⁾
Z-current	I_Z	0		100	mA	Observe P_{max}
Driver current	I_{QSIP}	- 500		500	mA	Observe P_{max}
Ambient temperature	T_A	- 25		85	°C	

Characteristics

$$V_{SON} < V_S < V_Z; T_A = -25 \text{ to } 85 \text{ }^\circ\text{C}$$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

Current Consumption

Without load on driver (QSIP) and V_{REF} ; QSIP low	I_S			0.5	mA	$0 \text{ V} < V_S < V_{SON}$ $V_{SON} < V_S < V_Z$ $V_S = 12 \text{ V};$ $f_{switch} = 50 \text{ kHz};$ load QSIP = 10 nF
Load on QSIP with SIPMOS gate;	I_S	5		10	mA	
dynamic operation	I_S			15	mA	

Hysteresis on V_S

Turn-ON threshold for V_S rising	V_{SH}	9.6	10.4	11.2	V	
Switching hysteresis	V_{Shy}	1.0		1.7	V	

Comparator

Input offset voltage	V_{IO}	-10		10	mV	
Input current	$-I_I$			2	μA	
Common-mode input voltage	V_{ICM}	0		3.5	V	

Operational Amplifier

Open-loop voltage gain	G_{VO}	60	80		dB	$T_j = 25 \text{ }^\circ\text{C}$ Pin 6 connected to Pin 7
Input offset voltage	V_{IO}	-10		10	mV	
Input current	$-I_I$			2	μA	
Common-mode input voltage	V_{IC}	0		3.5	V	
Output current	I_Q	-3		1.5	mA	
Output voltage	V_Q	1.2		4	V	
Gain-bandwidth product	f_T		2		MHz	
Transition phase	Φ_T		120		deg	
Voltage Feedback Threshold	V_{FB}	1.96	2	2.04	V	
Temperature response	$\Delta V_{FB}/\Delta T$	-0.3		0.3	mV/K	

Output Driver

H-output voltage	V_{QSIPH}	5			V	$I_{QSIP} = -10 \text{ mA}$
L-output voltage	V_{QSIPL}			1	V	$I_{QSIP} = 10 \text{ mA}$
Output current rising edge	$-I_{QSIP}$	200	300	400	mA	$C_L = 10 \text{ nF}$
falling edge	I_{QSIP}	250	350	450	mA	$C_L = 10 \text{ nF}$

Characteristics (cont'd)
 $V_{SON} < V_S < V_Z; T_A = -25 \text{ to } 85 \text{ } ^\circ\text{C}$

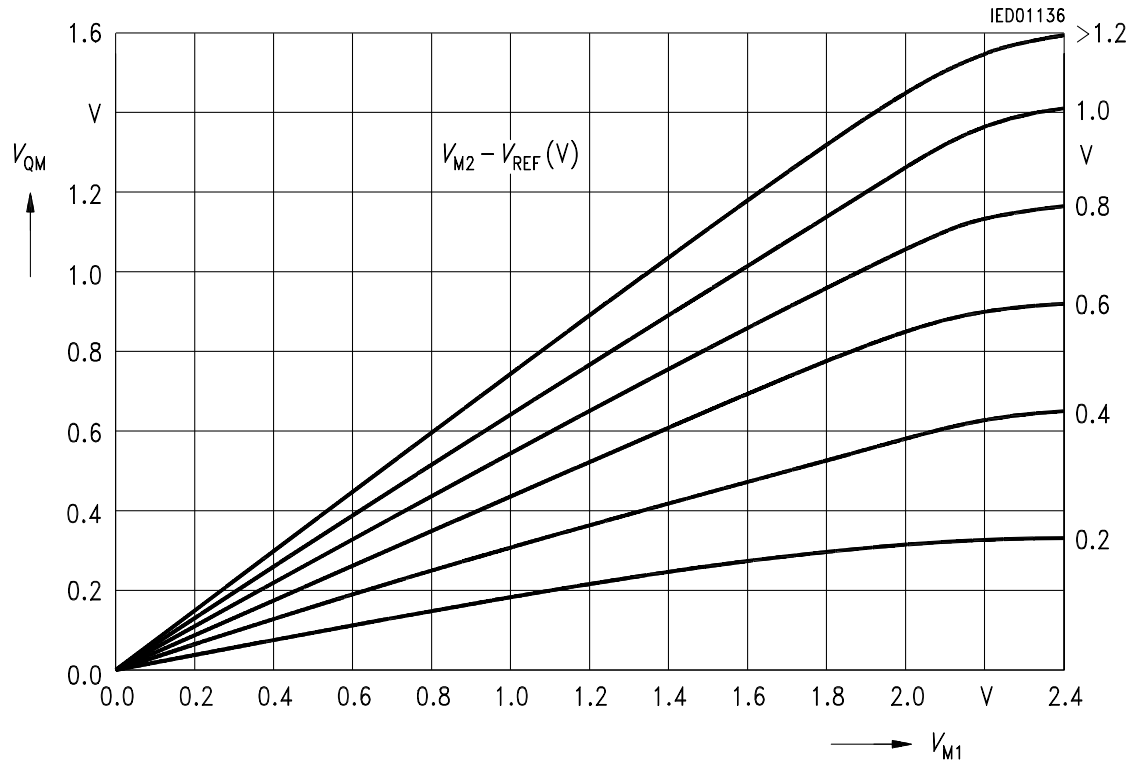
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Z-Diode (V_S)						
Z-voltage (observe P_{max})	V_Z	13	15.5	17	V	$I_Z = 200 \text{ mA}$
Multiplier						
Quadrant for input voltages			1.		qu	
Input voltage M1	V_{M1}	0		2	V	
Reference level for M1	$V_{REF M1}$		0		V	
Input voltage M2	V_{M2}	V_{REF}		$V_{REF} + 1$	V	
Reference level for M2	$V_{REF M2}$		V_{REF}		V	
Input current M1, M2	$-I_I$	0		2	μA	
Max. output voltage	$V_{QM max}$		1.6		V	
Multiplier gain	C_{Q25}	0.62	0.67	0.72	V^{-1}	$T_j = 25 \text{ } ^\circ\text{C}$ ¹⁾
Multiplier gain	C_Q	0.55		0.77	V^{-1}	¹⁾
Temperature response of coefficient	$\Delta TC/C_Q$	-0.3	-0.1	0.1	%/K	
Delay Times						
Input comparator-QSIP	t_i		500	700	ns	²⁾
Detector						
Upper switching voltage for voltage rising (H)	V_{DetH}	1.0	1.3	1.6	V	
Lower switching voltage for voltage falling (L)	V_{DetL}	0.95			V	
Input current	$-I_{Det}$			10	μA	$0.9 \text{ V} < V_{Det} < 6 \text{ V}$
Clamping-diode level	positive	$V_{Det +}$	6.9		V	$I_{Det} = 3 \text{ mA}$
	negative	$V_{Det -}$	0.6		V	$I_{Det} = 3 \text{ mA}$
Switching hysteresis	V_{Dethy}	50		300	mV	

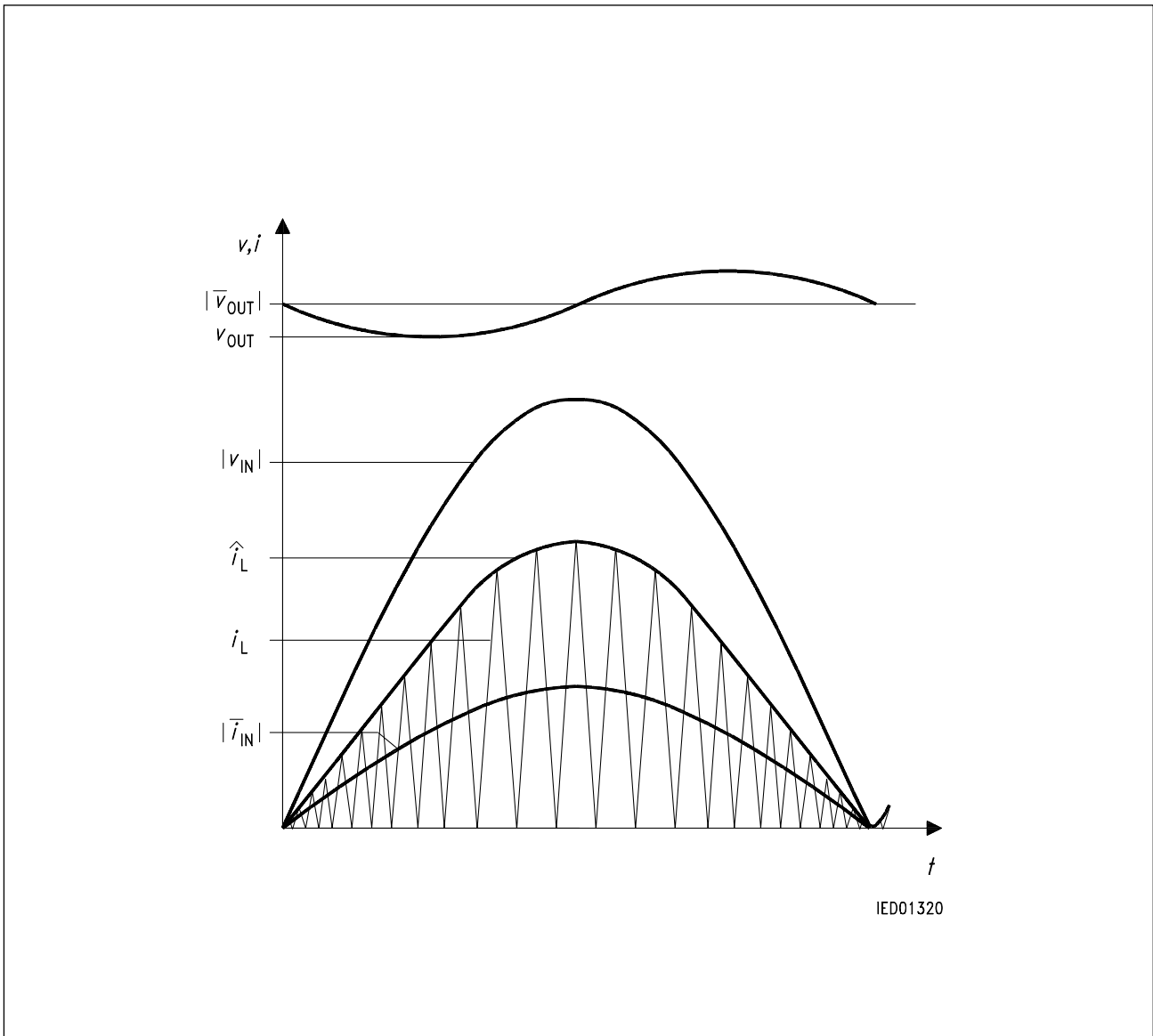
Calculation of output voltage V_{QM} : $V_{QM} = C \times V_{M1} \times V_{M2}$ in V.

1) $V_{M1} = 1 \text{ V}$
 $V_{M2} = V_{REF} + 1 \text{ V}$

2) Step function on comparator input ΔV_{Comp} from -100 mV to +100 mV.

Multiplier Characteristics





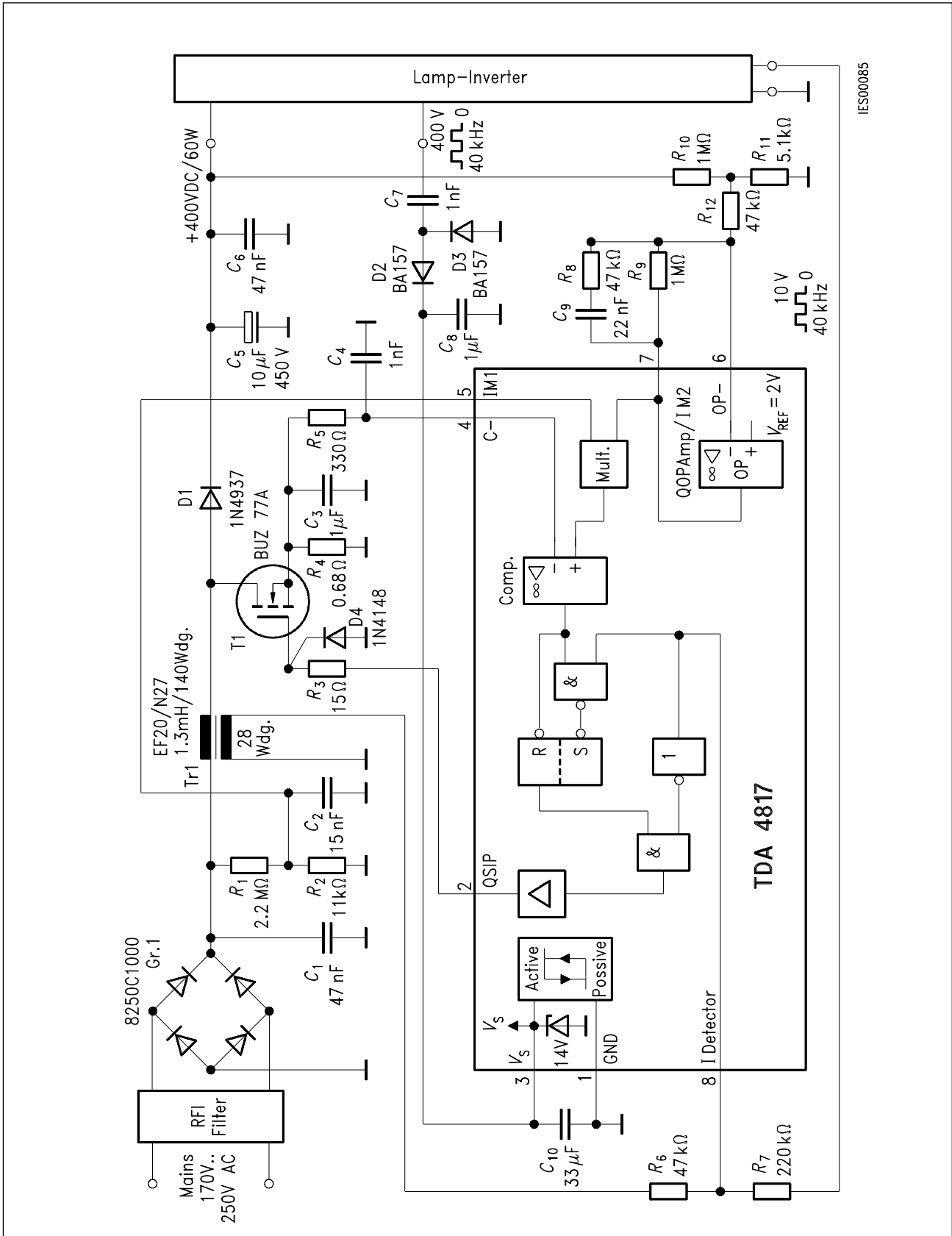
Discontinuous Operation Mode with Variable Frequency

The TDA 4817 works in a discontinuous operation mode with variable frequency.

The principle of a freely oscillating controller exploits the physical relationship between current and voltage at the boost converter choke. The current in the semiconductors flows in a triangular shape. This is only when the current in the boost converter diode has gone to zero that the transistor goes conductive. This arrangement does away with the diode's power-squandering reverse currents.

If triangular currents flow continuously through the boost converter choke the input current averaged over a high-frequency period is exactly half the peak of the high-frequency choke current.

If the peak values of the choke current are located along an envelope curve that is proportional to a sinusoidal low-frequency input voltage, the input current available after smoothing in an RFI filter is sinusoidal.



IES00085

Application Circuit: Electronic Ballast

The TDA 4817 controls a boost converter as an active harmonic filter, drawing a sinusoidal line current and providing a regulated DC voltage at the converter output.

The active harmonic filter improves the power factor in electronic ballasts for fluorescent lamps and in switched-mode power supplies, reducing the harmonic content of the incoming, non rectified mains current and if suitably dimensioned permitting operation at input voltages between 90 V and 270 V.

Benefits of TDA 4817 in Electronic Ballasts and SMPS

- Sinusoidal line current consumption
- Power factor approaching 1 increases the power available from the AC line by more than 35 % compared to conventional rectifier circuits. Circuit breakers and connectors become more reliable because of the lower peak currents.
- Active harmonic filtering reduces harmonic content in line current to meet VDE/IEC/EN-standards.
- Wide-range power supplies are easier to implement for AC input voltages of 90 to 250 V without switch-over.
- Preregulated DC output voltage provides optimal operating conditions for a subsequent converter.
- Reduced smoothing capacitance:
For a given amplitude of the 100/120 Hz ripple voltage the smoothing capacitance can be reduced by 50 % in comparison to a conventional rectifier circuit.
Reduced choke size:
Rectifier circuits capable of more than 200 W usually employ chokes to decrease the charging current of the capacitor. These chokes are larger than those used in a preregulator with power-factor control.
- Higher efficiency:
A preregulator does cause some additional losses, but these are more than compensated for by the cut in losses created by the rectifier configuration and the optimum operating conditions that are produced for a subsequent converter, even in the event of supply-voltage fluctuations.

Summary of Effects of DC-Voltage Preregulation with Power-Factor Control

Parameter	Conventional Power Rectification	Power Rectification with Preregulator and Power-Factor Control
Mean DC supply voltage	280 V	340 V
Maximum DC supply voltage with line overvoltage	350 V	350 V
Minimum DC supply voltage with line undervoltage	230 V	330 V
Relative reverse voltage of diodes with line overvoltage	1	0.7
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and line undervoltage	1	2.06
Relative forward resistance of SIPMOS transistors with sustained conducting-state power loss and rated supply voltage	1	1.74
Relative input capacitance with sustained ripple voltage	1	0.3 to 0.5
Power factor	0.5 to 0.7	0.99

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