Dual, SiGe, High-Linearity, 1700MHz to 2700MHz Downconversion Mixer with Advanced Shutdown Features

General Description

The MAX19757 dual-channel downconverter is designed to provide 8.8dB gain, +25.3dBm input IP3 and 10.4dB NF for a multitude of 1700MHz to 2700MHz basestation receiver applications. With an optimized LO frequency range of 1800MHz to 2600MHz, this mixer supports both high- and low-side LO injection architectures for 1700MHz to 2200MHz and 2000MHz to 2700MHz RF bands, respectively. Independent path shutdown allows the user to save DC power during low-peak usage times or in TDD TX mode.

The device integrates baluns in the RF and LO ports, an LO buffer, two double-balanced mixers, and a pair of differential IF output amplifiers. The MAX19757 requires a typical LO drive of 0dBm, and a supply current typically 300mA at band center and 350mA across the LO frequency band to achieve the targeted linearity performance.

The MAX19757 is available in a compact 36-pin TQFN package (6mm x 6mm x 0.8mm) with an exposed paddle. Electrical performance is guaranteed over the extended -40°C to +105°C temperature range.

Applications

- 2.3GHz WCS Base Stations
- 2.5GHz WiMAX®, LTE, TD-LTE Base Stations
- 2.7GHz MMDS Base Stations
- UMTS/WCDMA, TD-SCDMA and cdma2000® 3G Base Stations
- DCS1800 and PCS1900 and EDGE Base Stations
- Fixed Broadband Wireless Access
- Wireless Local Loop
- Private Mobile Radios
- Military Systems

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX19757.related**.*

Benefits and Features

- 1700MHz to 2700MHz RF Frequency Range
- 1800MHz to 2600MHz LO Frequency Range
- 50MHz to 500MHz IF Frequency Range
- 25.3dBm IIP3
- 8.8dB Conversion Gain
- 13.1dBm Input 1dB Compression Point
- 10.4dB Noise Figure
- 73dBc 2RF–2LO Spurious Rejection at P_{RF} = -10dBm
- Dual Channels Ideal for Diversity Receiver Applications
- Integrated LO Buffer
- -3dBm to +3dBm LO Drive
- Built-In SPDT LO Switch with 50dB LO-to-LO Isolation and 240ns Switching Time
- 46dB Channel Isolation
- Optional On-Chip Detector at IF Output Automatically Adjusts Bias Current for Optimum Power Management
- External Current-Setting Resistors Allow Tradeoff Between Power and Performance
- Advanced Shutdown Features Include:
  - Independent Path Power-Down
  - Rapid Power-Down/Power-Up Modes for Toggling Between On/Off States in TDD Applications
  - Controlled LO Port Impedance Minimizes VCO Pulling During Power Cycling

19-6280; Rev 0; 12/12

Absolute Maximum Ratings

V_{CC} .... -0.3V to +5.5V
RFMAIN, RFDIV, LO1, LO2,
IFM+, IFM-, IFD+, IFD- .... -0.3V to (V_{CC} + 0.3V)
IF_RADJ, LO_VADJ, LOSEL,
LO_TUNE1, LO_TUNE2 .... -0.3V to (V_{CC} + 0.3V)
RFMAIN to RFM_RTN, RFDIV to RFD_RTN 20mA
PD1, PD2, STBY, IF_DET_OUT,
IF_DET_CEXT .... -0.3V to (V_{CC} + 0.3V)
RFMAIN, RFDIV, LO1, LO2 Input Power .... +20dBm
Continuous Power Dissipation (Note 1) 8.7W
Operating Case Temperature Range (Note 2) ... -40°C to +105°C
Maximum Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

TQFN
Junction-to-Ambient Thermal Resistance θ_{JA}
(Notes 3, 4) .... +36°C/W
Junction-to-Case Thermal Resistance θ_{JC}
(Notes 1, 4) .... +7.4°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

5V DC Electrical Characteristics

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, RF and IF single ended ports = 50Ω to GND, LO1 port driven from 50Ω source, P_{LO} = 0dBm, f_{LO} = 2350MHz, LOSEL = 5V, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{LO} = 0dBm, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, T_C = +25°C, unless otherwise noted.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Dual-Channel Operation Supply Current	I_{DUALCH}	f_{LO} = 1800MHz, LO_TUNE1 = 0, LO_TUNE2 = 1		350	420	mA
		f_{LO} = 1900MHz, LO_TUNE1 = 0, LO_TUNE2 = 1		324	395	
		f_{LO} = 2100MHz, LO_TUNE1 = 0, LO_TUNE2 = 0		305	365	
		f_{LO} = 2300MHz, LO_TUNE1 = 1, LO_TUNE2 = 1		293	350	
		f_{LO} = 2350MHz, LO_TUNE1 = 1, LO_TUNE2 = 1		290	350	
		f_{LO} = 2500MHz, LO_TUNE1 = 1, LO_TUNE2 = 0		285	345	

5V DC Electrical Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, RF and IF single ended ports = 50Ω to GND, LO1 port driven from 50Ω source, P_{LO} = 0dBm, f_{LO} = 2350MHz, LOSEL = 5V, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{LO} = 0dBm, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, T_C = +25°C, unless otherwise noted.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Channel Operation Supply Current	$I_{SINGLECH}$	PD1 = 0, PD2 = 1 or PD1 = 1, PD2 = 1		163	197	mA
Power-Down Supply Current	I_{PD}	PD1 = 1, PD2 = 0		5.3	8.5	mA
Standby (STBY) Supply Current	I_{STBY}	STBY = 1 in any power-down mode		35	49	mA
LOSEL, PD1, PD2, STBY, LO_TUNE1, LO_TUNE2, Input High Voltage	V_{IH}		1.17			V
LOSEL, PD1, PD2, STBY LO_TUNE1, LO_TUNE2, Input Low Voltage	V_{IL}				0.5	V
Control Logic Input Current	I_{IL} and I_{IH}	$V_{IL} > -0.25$; $V_{IH} < V_{CC} + 0.25V$; internal 50kΩ pulldown resistors	-50		+250	µA

3.3V DC Electrical Characteristics

(*Typical Application Circuit*, V_{CC} = 3.1V to 3.5V, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, RF and IF single-ended ports = 50Ω to GND, LO1 port driven from 50Ω source, P_{LO} = 0dBm, f_{LO} = 2350MHz, LOSEL = 5V, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 3.3V, P_{LO} = 0dBm, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, T_C = +25°C, unless otherwise noted.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		3.1	3.3	3.5	V
Dual-Channel Operation Supply Current	I_{DUALCH}	Total supply current		305	385	mA
Single-Channel Operation Supply Current	$I_{SINGLECH}$	PD1 = 0, PD2 = 1 or PD1 = 1, PD2 = 1		163		mA
Power-Down Supply Current	I_{PD}	PD1 = 1, PD2 = 0		3.5		mA
Standby (STBY) Supply Current	I_{STBY}	STBY = 1 in any power-down mode		33		mA
LOSEL, PD1, PD2, STBY, LO_TUNE1, LO_TUNE2, Input High Voltage	V_{IH}			1.0		V
LOSEL, PD1, PD2, STBY, LO_TUNE1, LO_TUNE2, Input Low Voltage	V_{IL}			0.75		V
Control Logic Input Current	I_{IL} and I_{IH}	$V_{IL} > -0.25$; $V_{IH} < V_{CC} + 0.25V$; internal 50kΩ pulldown resistors		0 to 100		µA

Recommended AC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 7)	1700		2700	MHz
LO Frequency	f_{LO}	(Note 7)	1800		2600	MHz
IF Frequency (Note 7)	f_{IF}	Using Mini-Circuits TC4-1W-17 4:1 transformer as defined in the *Typical Application Circuit*; IF matching components affect the IF frequency range	100		500	MHz
		Using alternative Mini-Circuits TC4-1W-7A 4:1 transformer as defined in the *Typical Application Circuit*, IF matching components affect the IF frequency range	50		250	
LO Drive Level	P_{LO}		-3		+3	dBm

5V AC Electrical Characteristics (Low-Side LO)

(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{RF} = -5dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz, P_{LO1} = -3dBm to +3dBm, LOSEL = 1, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, f_{IF} = 200MHz, and T_C = +25°C.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	G_C			7.4	8.8	9.9	dB
		T_C = +25°C		8.1	8.8	9.7	
RF Gain Flatness		Flatness over any 120MHz portion of the RF band, f_{IF} = 200MHz			0.10		dB
Conversion Gain Flatness	G_{FREQ}	Flatness over a 100MHz RF band, f_{IF} = 200 ±50MHz (Note 9)			0.34	0.55	dB
Gain Variation Over Temperature	TC_{CG}	T_C = -40°C to +105°C			-0.010		dB/°C
1σ Gain Deviation		T_C = -40°C to +105°C			0.082		dB
Input 1dB Compression Point	IP_{1dB}	(Notes 8, 9)		11	13.1		dBm
Output 1dB Compression Point	OP_{1dB}	(Notes 8, 9)		17	20.9		dBm
Input 0.1dB Compression Point	$IP_{0.1dB}$	(Note 9)		4	5.6		dBm
Small-Signal Compression Under Blocking Conditions		P_{RF} = -5dBm, $f_{BLOCKER}$ = 2545MHz, $P_{BLOCKER}$ = 8dBm (Note 8)			0.4		dB
Input Third-Order Intercept Point	IIP3	f_{RF1}-f_{RF2} = 1MHz, P_{RF} = -5dBm/tone (Notes 9,10)	T_C = +25°C	23.9	25.3		dBm
				23.5	25.3		
Input Third-Order Intercept Point 1σ Deviation	$IIP3_{dev}$	f_{RF1}-f_{RF2} = 1MHz, P_{RF} = -5dBm/tone			0.17		dBm
Input Third-Order Intercept Point Variation Over Temperature	TC_{IIP3}	f_{RF1}-f_{RF2} = 1MHz, P_{RF} = -5dBm/tone, T_C = -40°C to +105°C			0.0035		dB/°C
Output Third-Order Intercept Point	OIP3	f_{RF1}-f_{RF2} = 1MHz, P_{RF} = -5dBm/tone (Notes 9, 10)	T_C = +25°C	30.8	34.1		dBm
				30.4	34.1		

5V AC Electrical Characteristics (Low-Side LO) (continued)

(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{RF} = -5dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz, P_{LO1} = -3dBm to +3dBm, LOSEL = 1, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, f_{IF} = 200MHz, and T_C = +25°C.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Noise Figure, Single Sideband (Note 9)	NF_{SSB}	T_C = +25°C, no blockers present, RF trace de-embedded			10.4	10.9	dB
		No blockers present, RF trace de-embedded, T_C = -40°C to +100°C			10.4	12.2	
Noise Figure Temperature Coefficient	TC_{NF}	Single sideband, no blockers present, T_C = -40°C to +105°C			0.0166		dB/°C
1σ NF deviation	NF_{STD}				0.09		dB
Noise Figure with Blocker	NF_B	$P_{BLOCKER}$ = 8dBm, $f_{BLOCKER}$ = 2300MHz, f_{RF} = 2200MHz, f_{LO} = 1950MHz, $f_{IFDESIRED}$ = 250MHz, $f_{IFBLOCKER}$ = 350MHz P_{LO} = 0dBm, V_{CC} = 5.0V, T_C = +25°C (Notes 9, 11)			18.3	20	dB
2RF - 2LO Spur Rejection (Note 9)	2 x 2	f_{SPUR} = f_{LO} + 100MHz	P_{RF} = -10dBm	63	73		dBc
			P_{RF} = -5dBm (Note 10)	58	68		
3RF - 3LO Spur Rejection (Note 9)	3 x 3	f_{SPUR} = f_{LO} + 66.667MHz	P_{RF} = -10dBm	75	91		dBc
			P_{RF} = -5dBm (Note 10)	65	81		
LO Leakage at RF Port		P_{LO} = 3dBm (Note 9)			-39.8	-34	dBm
2LO Leakage at RF Port		P_{LO} = 3dBm (Note 9)			-24.3	-20	dBm
3LO Leakage at RF Port		P_{LO} = 3dBm (Note 9)			-46	-40	dBm
4LO Leakage at RF Port		P_{LO} = 3dBm (Note 9)			-31	-22	dBm
LO Leakage at IF Port		P_{LO} = 3dBm (Notes 9, 10)			-25.5	-23	dBm
LO Leakage at IF Port		P_{LO} = 3dBm, F_{LO} = 2150MHz, (Note 10)			-19.9		dBm
2LO Leakage at IF Port		P_{LO} = 3dBm			-37		dBm
RF to IF Isolation		(Notes 9, 10)		30	37.3		dB
LO1 to LO2 Isolation		P_{LO1} = 3dBm, P_{LO2} = 3dBm, f_{LO1}-f_{LO2} = 1MHz, P_{RF} = -5dBm (Note 12)		30	50		dB
Channel-to-Channel Isolation		P_{RF} = -10dBm, RFMAIN (RFDIV) power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω (Notes 9, 10)		40	46		dB
LO Switching Time		50% of LOSEL to IF settled within two degrees			0.24		µs
Power-Down IF Attenuation		0dBm at RF & LO ports; IF output power reduction from PD1 and PD2 switched from 0 to 1		40	61		dB

5V AC Electrical Characteristics (Low-Side LO) (continued)

(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{RF} = -5dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz, P_{LO1} = -3dBm to +3dBm, LOSEL = 1, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, f_{IF} = 200MHz, and T_C = +25°C.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Time		PD1 and PD2 switched from 0 to 1. Settled to within 5% of the final power down DC current.		20		ns
Power-Down Recovery Time		PD1 and PD2 switched from 1 to 0. The 'on' state is defined as IF phase settled to within < ±1° of the final value in a static measurement.		0.55		µs
STBY Time		STBY switched from 0 to 1. Settled to within 5% of the final shutdown DC current.		20		ns
STBY Recovery Time		STBY switched from 1 to 0. The 'on' state is defined as IF phase settled to within < ±1° of the final value in a static measurement.		0.5		µs
RF Input Impedance	Z_{RF}			50		Ω
RF Return Loss		LO on and IF terminated		20		dB
LO Input Impedance	Z_{LO}			50		Ω
LO Return Loss		LO port selected		16		dB
		LO port unselected		17		
IF Output Impedance	Z_{IF}	Nominal differential impedance at the IC's IF outputs		200		Ω
IF Return Loss		RF terminated into 50Ω, LO driven by 50Ω source, IF transformed to 50Ω using external components shown in the *Typical Application Circuit*		30		dB

5V AC Electrical Characteristics (High-Side LO)

(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO1} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 2150MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz, LOSEL = 1, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2150MHz, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, f_{IF} = 200MHz, and T_C = +25°C.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	G_C			7.7	9.2	10.2	dB
		T_C = +25°C		8.4	9.2	10.1	
RF Gain Flatness		Flatness over any 120MHz portion of the RF band, f_{IF} = 200MHz			0.10		dB
Conversion Gain Flatness	G_{FREQ}	Flatness over a 100MHz RF band, f_{IF} = 200 ±50MHz			0.4		dB
Gain Variation Over Temperature	TC_{CG}	T_C = -40°C to +105°C			-0.010		dB/°C
1σ Gain Deviation					0.08		dB
Input 1dB Compression Point	IP_{1dB}	(Notes 8, 9)		10.3	12.6		dBm
Output 1dB Compression Point	OP_{1dB}	(Notes 8, 9)		17.0	20.8		dBm
Input 0.1dB Compression Point	$IP_{0.1dB}$				7.1		dBm
Small-Signal Compression Under Blocking Conditions		P_{RF} = -5dBm, $f_{BLOCKER}$ = 2155MHz $P_{BLOCKER}$ = 8dBm (Note 8)			0.4		dB
Input Third-Order Intercept Point	IIP3	f_{RF1} - f_{RF2} = 1MHz, P_{RF} = -5dBm/tone			24.7		dBm
Input Third-Order Intercept Point 1σ Deviation	$IIP3_{dev}$	f_{RF1} - f_{RF2} = 1MHz, P_{RF} = -5dBm/tone			0.15		dBm
Input Third-Order Intercept Point Variation Over Temperature	TC_{IIP3}	f_{RF1} - f_{RF2} = 1MHz, P_{RF} = -5dBm/tone, T_C = -40°C to +105°C			-0.01		dB/°C
Output Third-Order Intercept Point	OIP3	f_{RF1} - f_{RF2} = 1MHz, P_{RF} = -5dBm/tone			34		dBm
Noise Figure, Single Sideband	NF_{SSB}	No blockers present			10.0		dB
Noise Figure Temperature Coefficient	TC_{NF}	Single sideband, no blockers present, T_C = -40°C to +105°C			0.017		dB/°C
Noise Figure with Blocker	NF_B	$P_{BLOCKER}$ = 8dBm, $f_{BLOCKER}$ = 1950MHz, f_{RF} = 2050MHz, f_{LO} = 2300MHz, $f_{IFDESIRED}$ = 250MHz, $f_{IFBLOCKER}$ = 350MHz (Note 11)			18.4		dB
2LO – 2RF Spur Rejection	2 x 2	f_{SPUR} = f_{LO} - 100MHz	P_{RF} = -10dBm		85		dBc
			P_{RF} = -5dBm		80		dBc
3LO – 3RF Spur Rejection	3 x 3	f_{SPUR} = f_{LO} - 66.667MHz	P_{RF} = -10dBm		85.5		dBc
			P_{RF} = -5dBm		75.5		dBc
LO Leakage at RF Port		P_{LO} = 3dBm			-40		dBm
2LO Leakage at RF Port		P_{LO} = 3dBm			-24		dBm
3LO Leakage at RF Port		P_{LO} = 3dBm			-40		dBm
4LO Leakage at RF Port		P_{LO} = 3dBm			-30		dBm
LO Leakage at IF Port		P_{LO} = 3dBm (Note 10)			-25.5		dBm
2LO Leakage at IF Port		P_{LO} = 3dBm			-37		dBm

5V AC Electrical Characteristics (High-Side LO) (continued)

(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO1} = -3dBm to +3dBm, P_{RF} = -5dBm, f_{RF} = 2150MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz, LOSEL = 1, LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD2 = STBY = 0, T_C = -40°C to +105°C. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2150MHz, f_{LO} = 2350MHz, LO_TUNE1 = LO_TUNE2 = 1, f_{IF} = 200MHz, and T_C = +25°C.) (Notes 5, 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF to IF Isolation		(Note 10)		34		dB
LO1 to LO2 Isolation		P_{LO1} = 3dBm, P_{LO2} = 3dBm, f_{LO1} - f_{LO2} = 1MHz, P_{RF} = -5dBm (Note 12)	30	50		dB
Channel-to-Channel Isolation		P_{RF} = -10dBm, RFMAIN (RFDIV) power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω, (Note 10)		50		dB
LO Switching Time		50% of LOSEL to IF settled within two degrees		0.24		µs
Power-Down IF Attenuation		0dBm at RF & LO ports; IF output power reduction from PD1 and PD2 switched from 0 to 1	40	61		dB
Power-Down Time		PD1 and PD2 switched from 0 to 1. Settled to within 5% of the final power down DC current.		20		ns
Power-Down Recovery Time		PD1 and PD2 switched from 1 to 0. The ‘on’ state is defined as IF phase settled to within < ±1° of the final value in a static measurement.		0.55		µs
STBY Time		STBY switched from 0 to 1. Settled to within 5% of the final shutdown DC current.		20		ns
STBY Recovery Time		STBY switched from 1 to 0. The ‘on’ state is defined as IF phase settled to within < ±1° of the final value in a static measurement.		0.5		µs
RF Input Impedance	Z_{RF}			50		Ω
RF Return Loss		LO on and IF terminated		20		dB
LO Input Impedance	Z_{LO}			50		Ω
LO Return Loss		LO port selected		16		dB
		LO port unselected		17		
IF Output Impedance	Z_{IF}	Nominal differential impedance at the IC’s IF outputs		200		Ω
IF Return Loss		RF terminated into 50Ω, LO driven by 50Ω source, IF transformed to 50Ω using external components shown in the *Typical Application Circuit*.		30		dB

3.3V AC Electrical Characteristics (Low-Side LO)

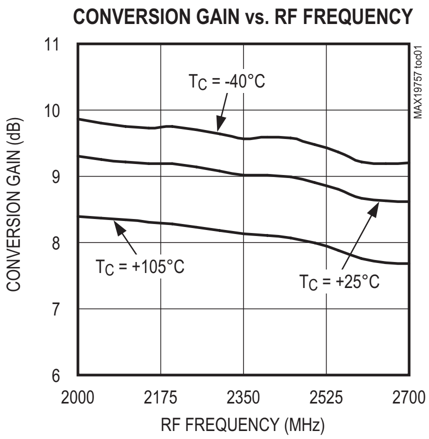
(*Typical Application Circuit*, R1 = 4.87kΩ, R3 = 154kΩ to V_{CC}, RF and LO ports are driven from 50Ω sources. Typical values are at V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 2550MHz, f_{LO} = 2350MHz, f_{IF} = 200MHz LO_TUNE1 = LO_TUNE2 = 1, PD1 = PD = STBY = 0, and T_C = +25°C.) (Note 6)

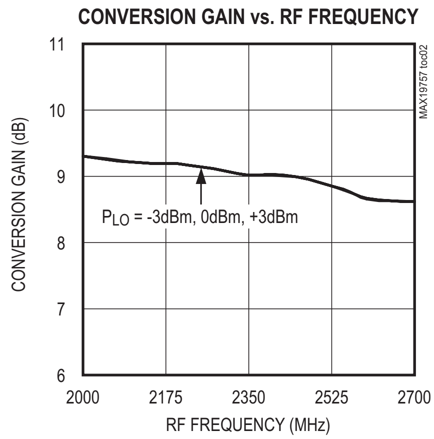
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Gain	G_C				8.9		dB
Gain Variation Over Temperature	TC_{CG}	T_C = -40°C to +105°C			0.011		dB/°C
Input 1dB Compression Point	IP_{1dB}	(Note 8)			10.2		dBm
Output 1dB Compression Point	OP_{1dB}	(Note 8)			18.1		dBm
Input Third-Order Intercept Point	IIP3	f_{RF1} - f_{RF2} = 1MHz, P_{RF} = -5dBm/tone			24.1		dBm
Output Third-Order Intercept Point	OIP3	f_{RF1} - f_{RF2}=1MHz, P_{RF} = -5dBm/tone			33		dBm
Noise Figure, Single Sideband	NF_{SSB}	No blockers present, RF trace de-embedded			10.3		dB
2RF - 2LO Spur Rejection	2 x 2	f_{SPUR} = f_{LO} + 100MHz	P_{RF} = -10dBm		71		dBc
			P_{RF} = -5dBm		66		dBc
3RF - 3LO Spur Rejection	3 x 3	f_{SPUR} = f_{LO} + 66.667MHz	P_{RF} = -10dBm		82		dBc
			P_{RF} = -5dBm		72		dBc
LO Leakage at RF Port		P_{LO} = 3dBm			-36.6		dBm
2LO Leakage at RF Port		P_{LO} = 3dBm			-22.6		dBm
LO Leakage at IF Port		P_{LO} = 3dBm			-26.3		dBm
RF to IF Isolation					35.6		dB
Channel-to-Channel Isolation		P_{RF} = -10dBm, RFMAIN (RFDIV) power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused ports terminated to 50Ω			45.6		dB
LO Switching Time		50% of LOSEL to IF settled within two degrees			0.24		us
RF Input Impedance	Z_{RF}				50		Ω
RF Return Loss		LO on and IF terminated			20		dB
LO Input Impedance	Z_{LO}				50		Ω
LO Return Loss		LO port selected			16		dB
		LO port unselected			17		
IF Output Impedance	Z_{IF}	Nominal differential impedance at the IC's IF outputs			200		Ω
IF Return Loss		RF terminated into 50Ω, LO driven by 50Ω source, IF transformed to 50Ω using external components shown in the *Typical Application Circuit*.			30		dB

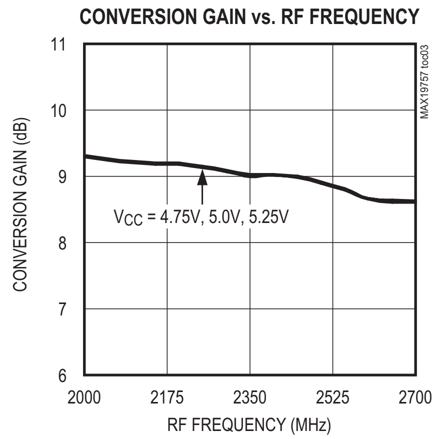
Note 5: Production tested and guaranteed at T_C = +25°C for worst-case supply voltage. Performance at T_C = -40°C and +105°C are guaranteed by production test characterization.
Note 6: All limits reflect 0.35dB loss for RF connectors and PCB RF trace, and 0.7dB loss for the IF transformer unless otherwise noted .Output measurements taken at IF outputs with the *Typical Application Circuit*.
Note 7: Not production tested. Operation outside this range is possible, but with degraded performance of some parameters. See *Typical Operating Characteristics*.
Note 8: Maximum reliable continuous input power applied to the RF or LO port of this device is 15dBm from a 50Ω source.
Note 9: Guaranteed by design and characterization. GBDC limits are 6-sigma.
Note 10: 100% production tested for functionality.
Note 11: Measured with external LO source noise filtered so the noise floor is -174dBm/Hz. This specification reflects the effects of all SNR degradations in the mixer, including the LO noise as defined in Maxim Application Note 2021: *Specifications and Measurement of Local Oscillator Noise in Integrated Circuit Base Station Mixers*.
Note 12: Measured at IF port at IF frequency. LOSEL may be in either logic state.

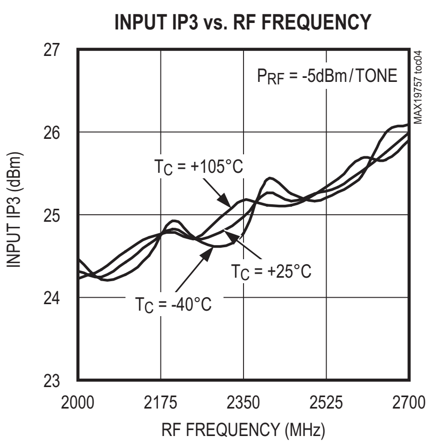
Typical Operating Characteristics

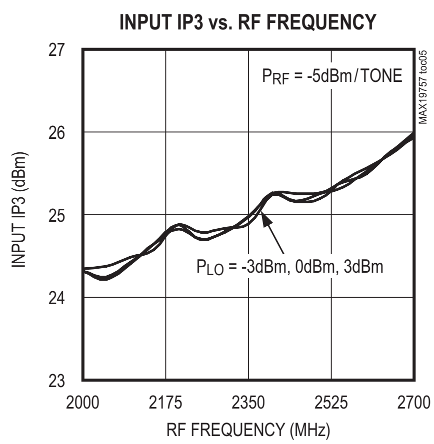
(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

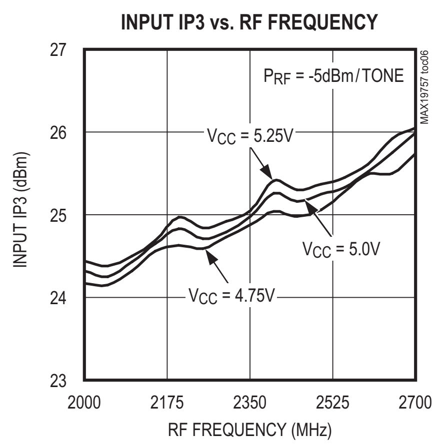


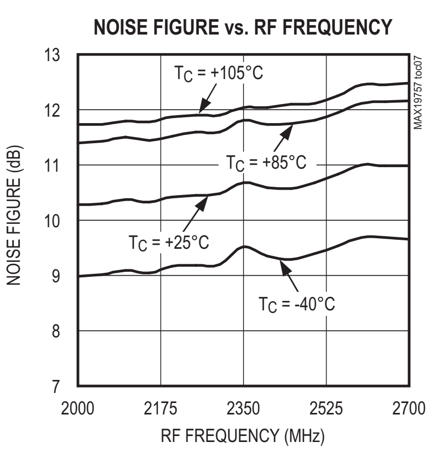


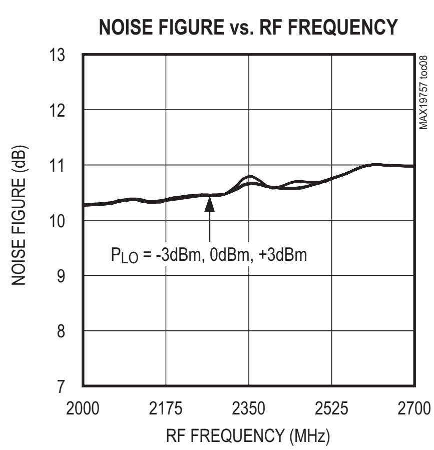


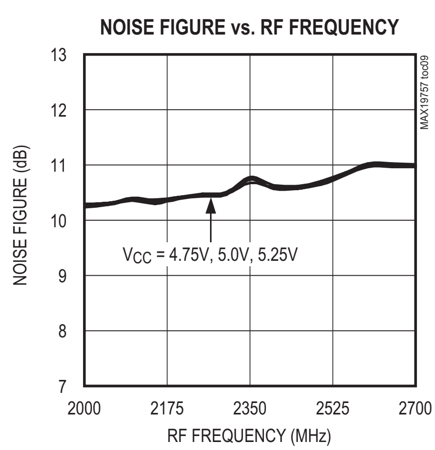






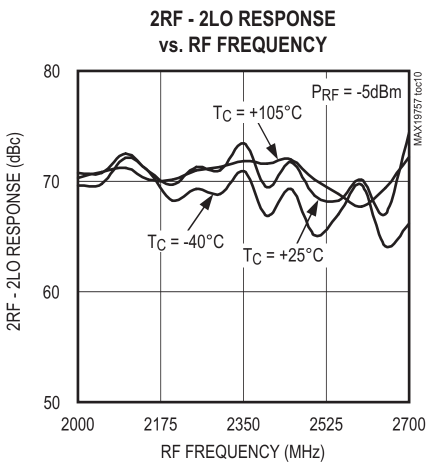


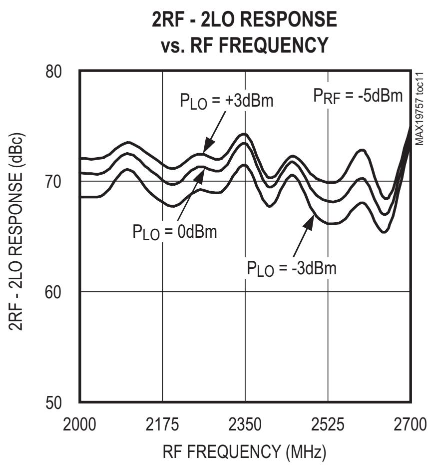


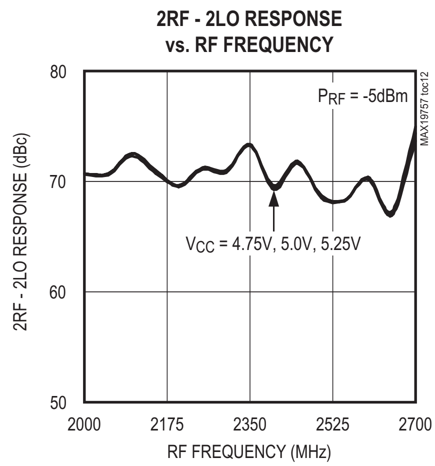


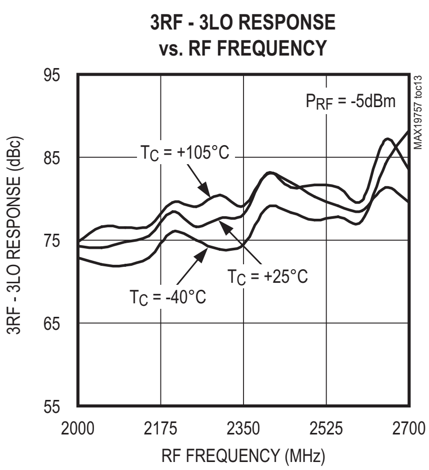
Typical Operating Characteristics (continued)

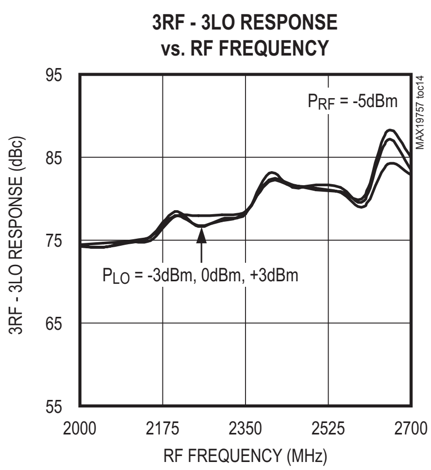
(Typical Application Circuit, **V_{CC} = 5.0V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

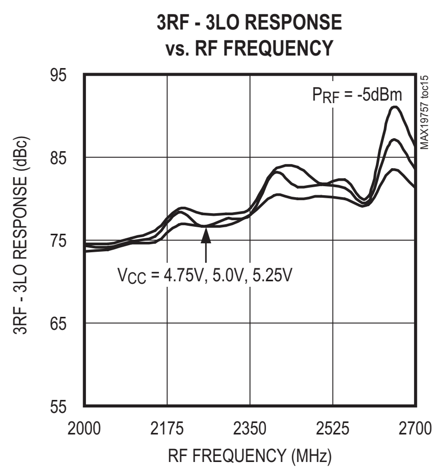


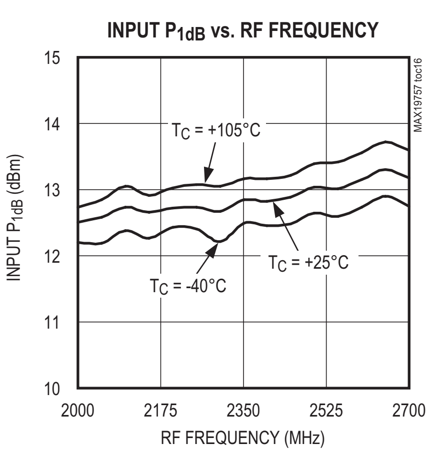


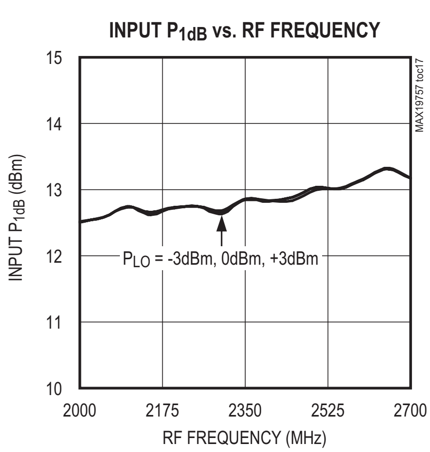


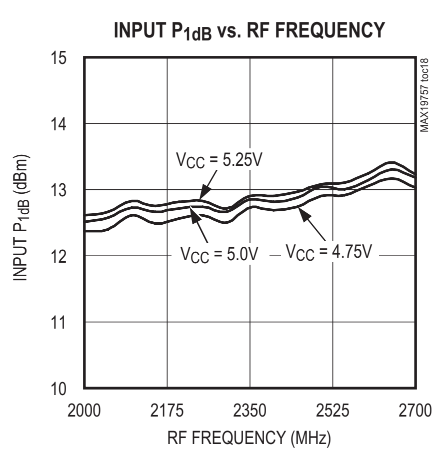








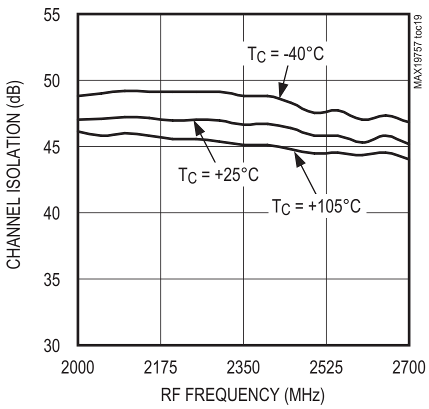




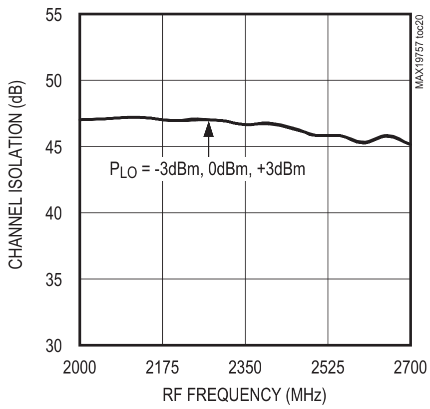
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

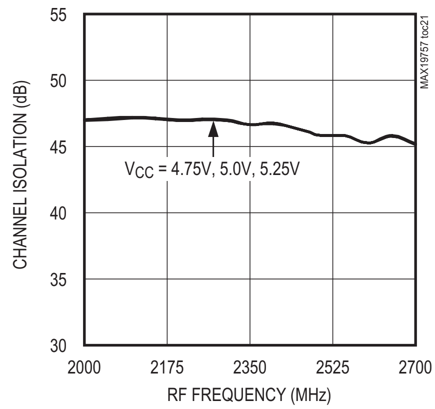
CHANNEL ISOLATION vs. RF FREQUENCY



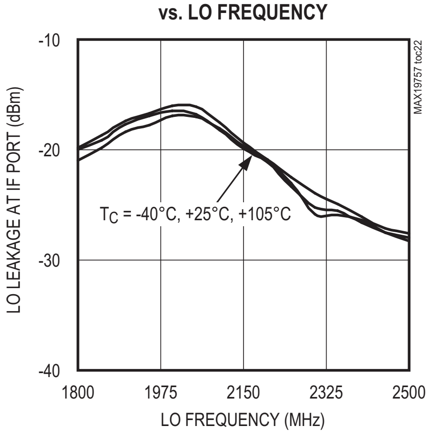
CHANNEL ISOLATION vs. RF FREQUENCY



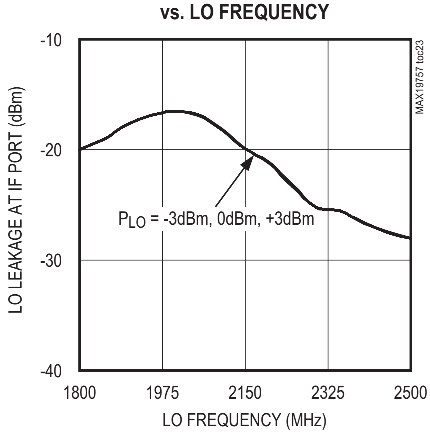
CHANNEL ISOLATION vs. RF FREQUENCY



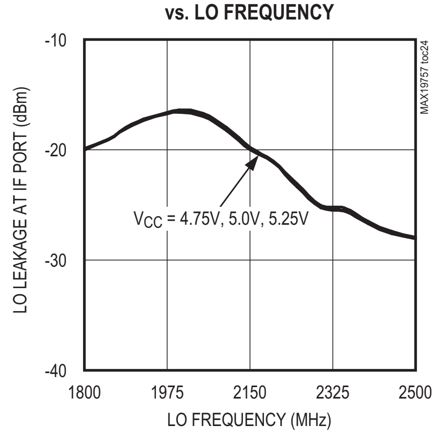
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



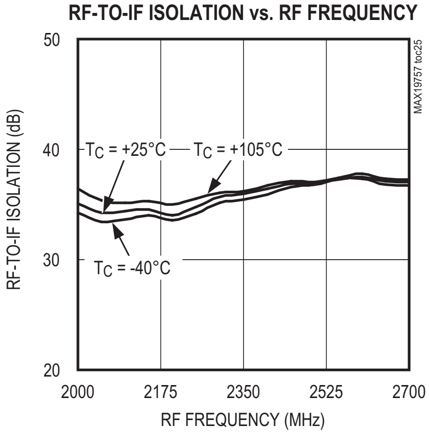
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



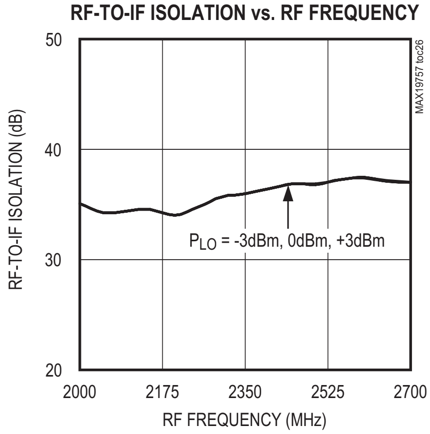
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



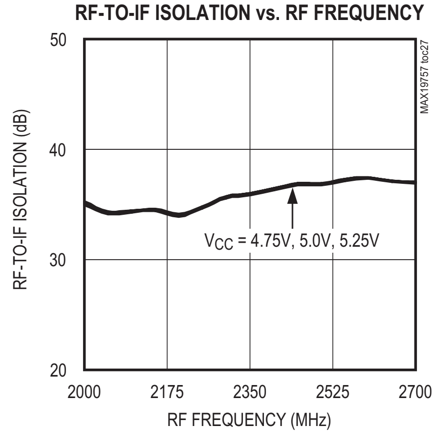
RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY



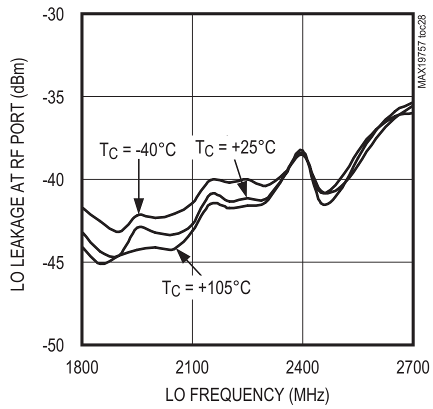
RF-TO-IF ISOLATION vs. RF FREQUENCY



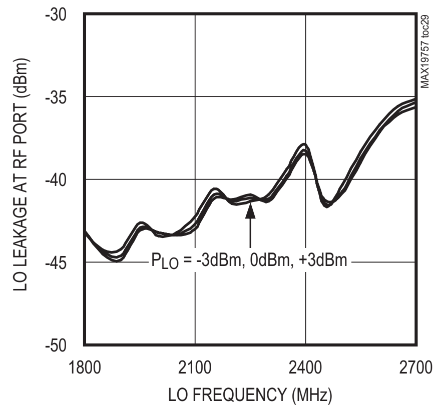
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

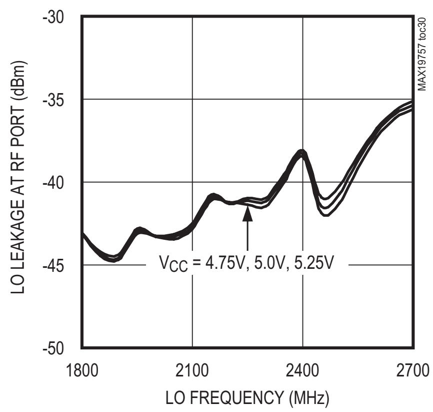
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



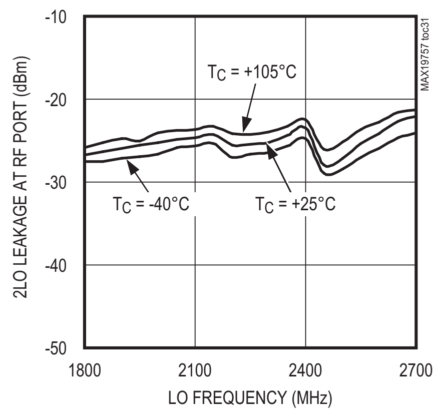
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



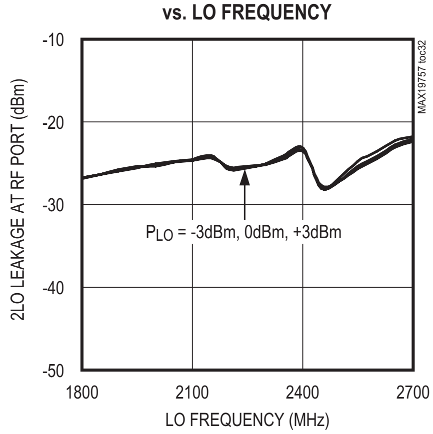
LO LEAKAGE AT RF PORT vs. LO FREQUENCY



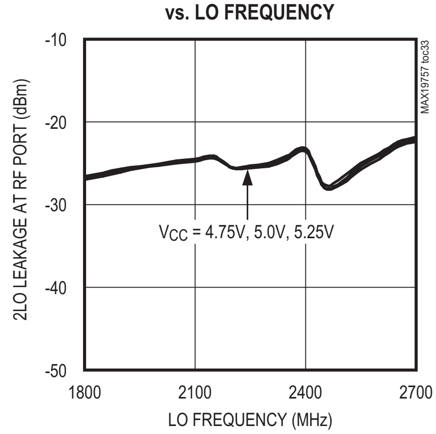
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY



2LO LEAKAGE AT RF PORT vs. LO FREQUENCY

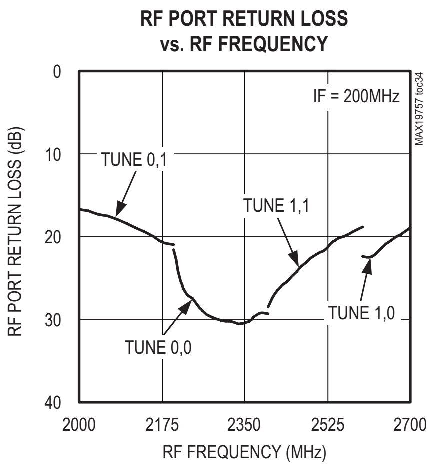


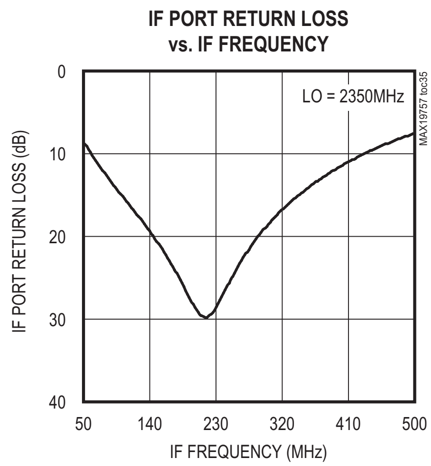
2LO LEAKAGE AT RF PORT vs. LO FREQUENCY

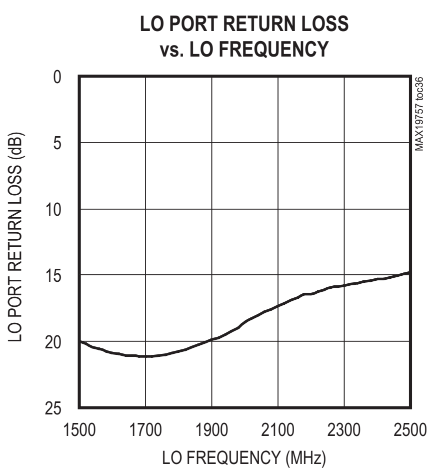


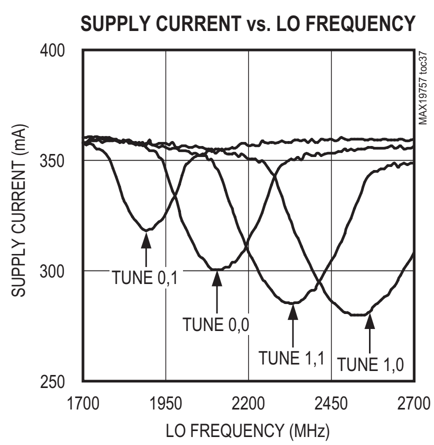
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)





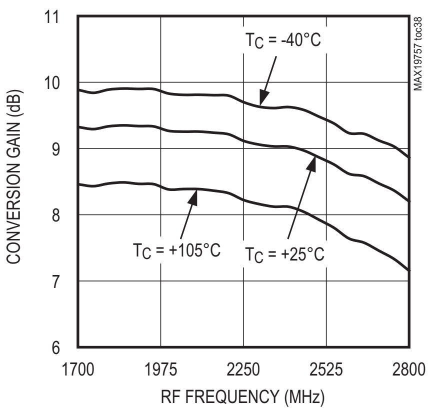




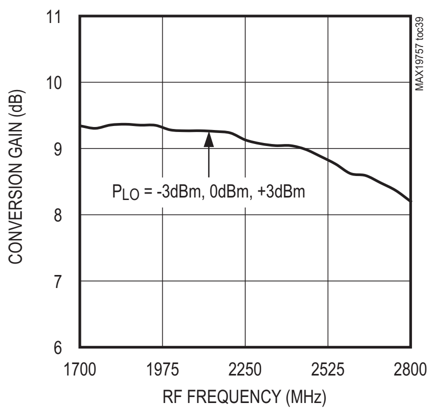
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 1700MHz to 2800MHz, LO is high-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

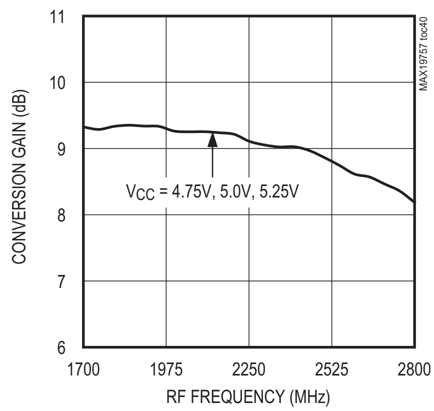
CONVERSION GAIN vs. RF FREQUENCY



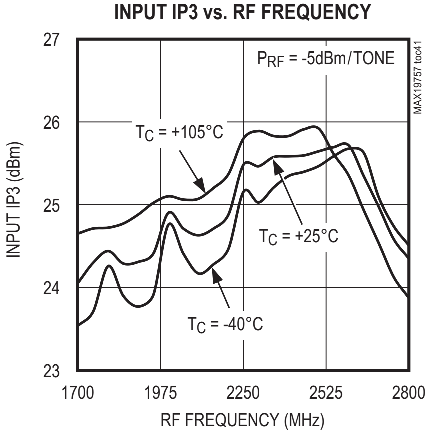
CONVERSION GAIN vs. RF FREQUENCY



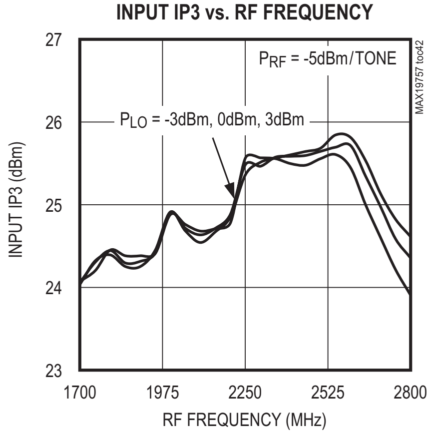
CONVERSION GAIN vs. RF FREQUENCY



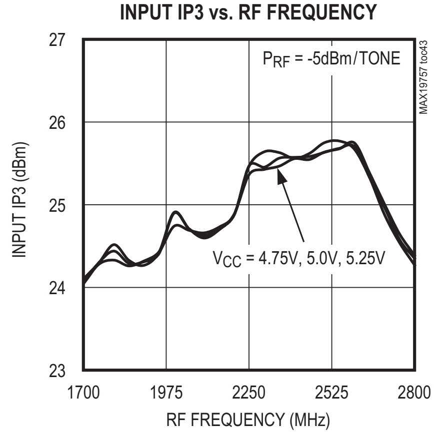
INPUT IP3 vs. RF FREQUENCY



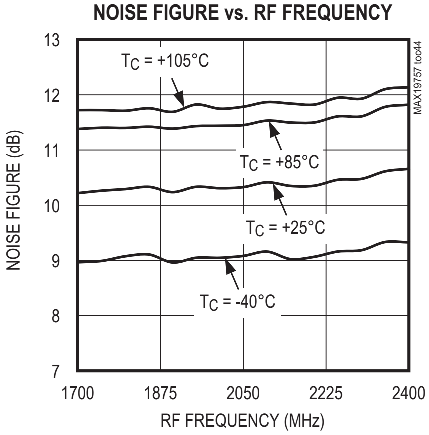
INPUT IP3 vs. RF FREQUENCY



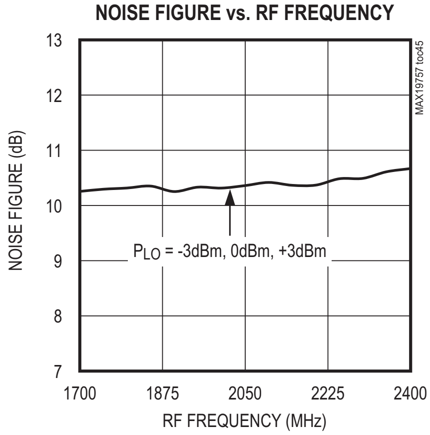
INPUT IP3 vs. RF FREQUENCY



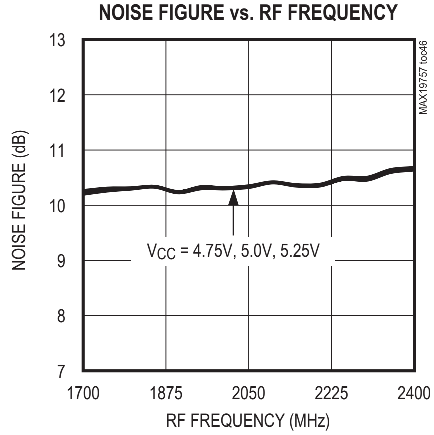
NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



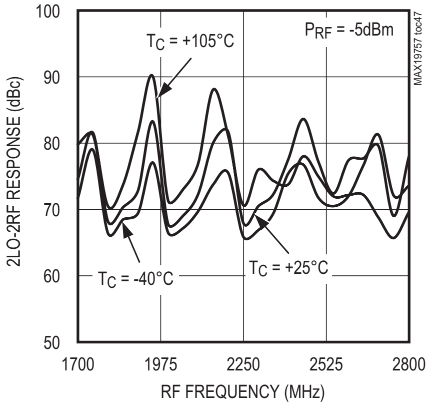
NOISE FIGURE vs. RF FREQUENCY



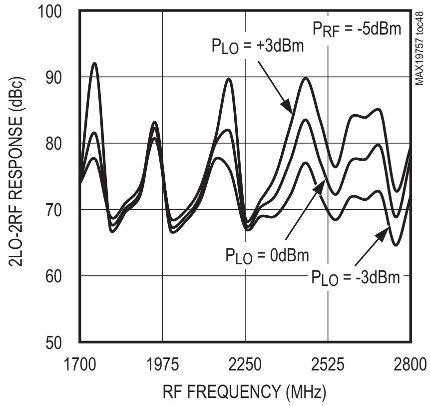
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 1700MHz to 2800MHz, LO is high-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

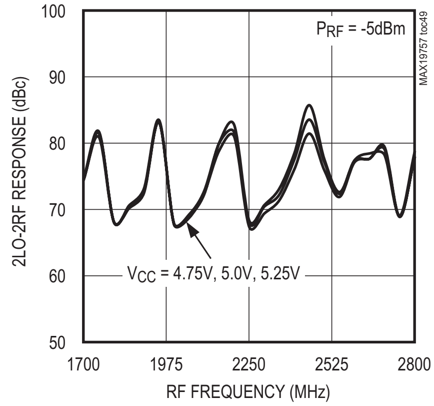
2LO - 2RF RESPONSE vs. RF FREQUENCY



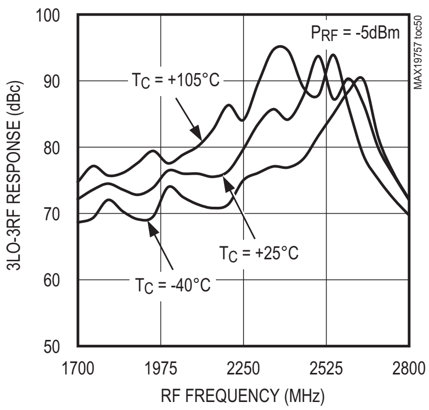
2LO - 2RF RESPONSE vs. RF FREQUENCY



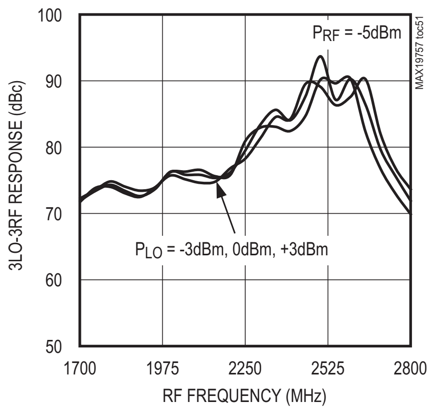
2LO - 2RF RESPONSE vs. RF FREQUENCY



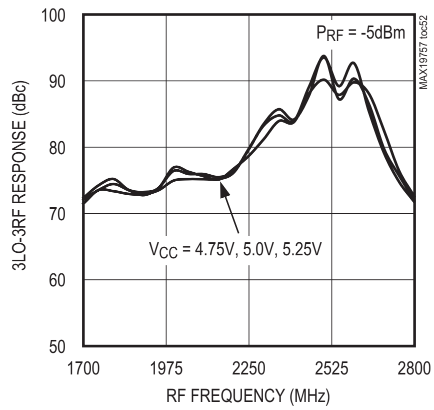
3LO - 3RF RESPONSE vs. RF FREQUENCY



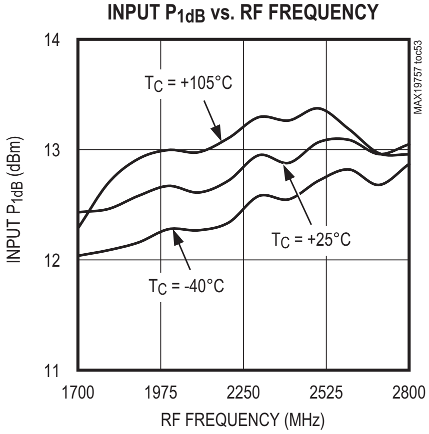
3LO - 3RF RESPONSE vs. RF FREQUENCY



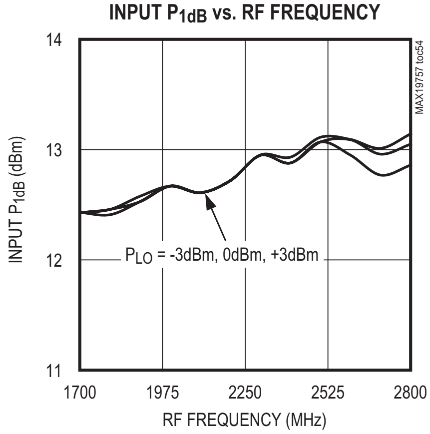
3LO - 3RF RESPONSE vs. RF FREQUENCY



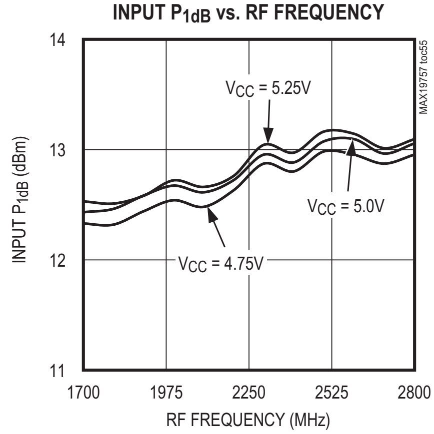
INPUT P_{1dB} vs. RF FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY



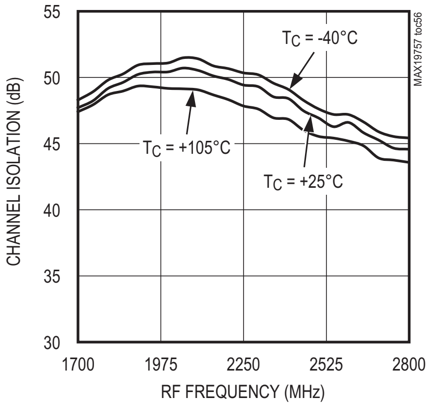
INPUT P_{1dB} vs. RF FREQUENCY



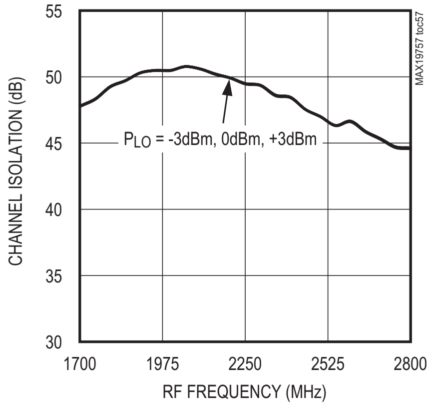
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 1700MHz to 2800MHz, LO is high-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

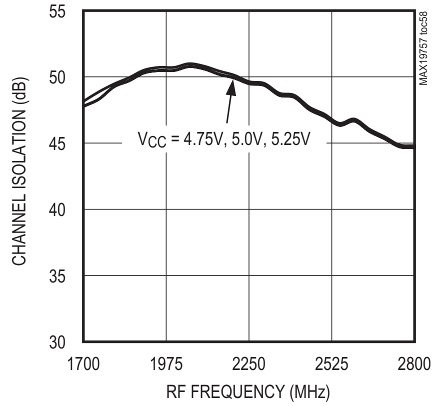
CHANNEL ISOLATION vs. RF FREQUENCYY



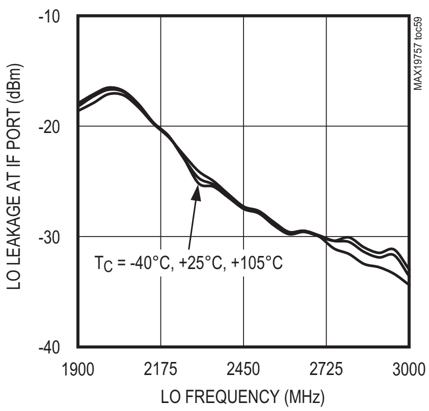
CHANNEL ISOLATION vs. RF FREQUENCY



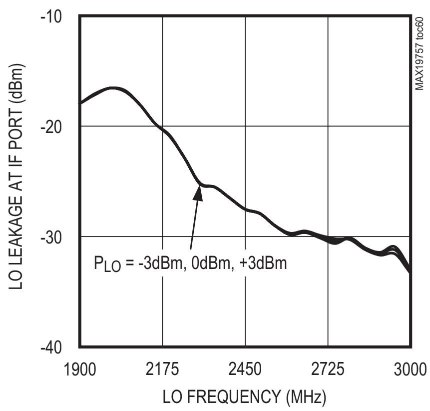
CHANNEL ISOLATION vs. RF FREQUENCY



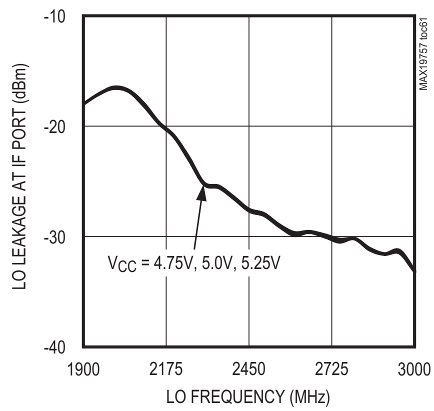
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



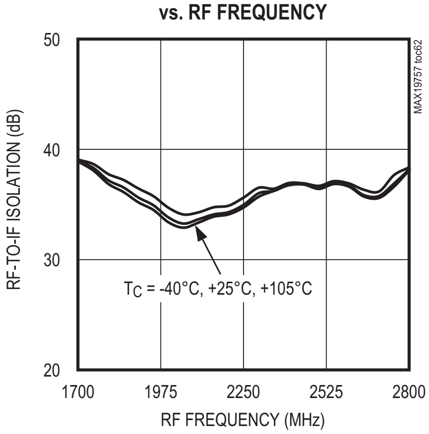
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



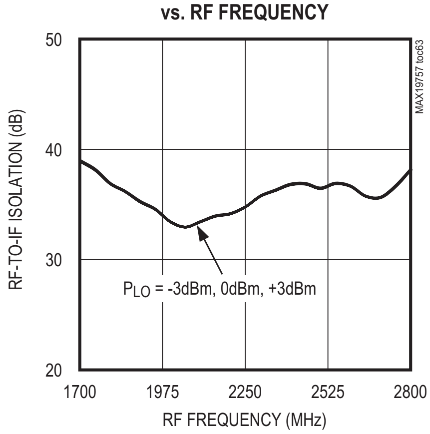
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



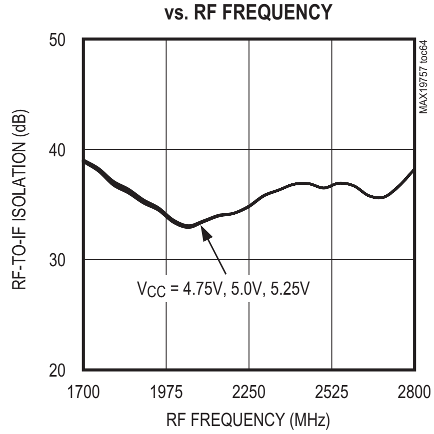
RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY

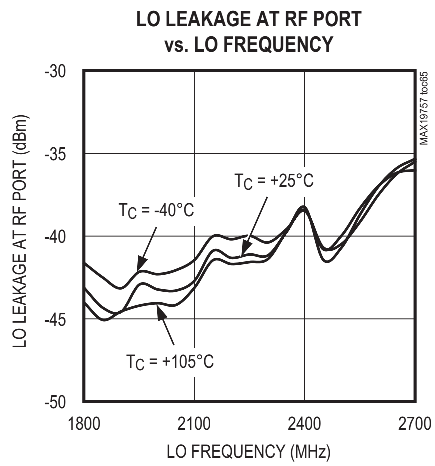


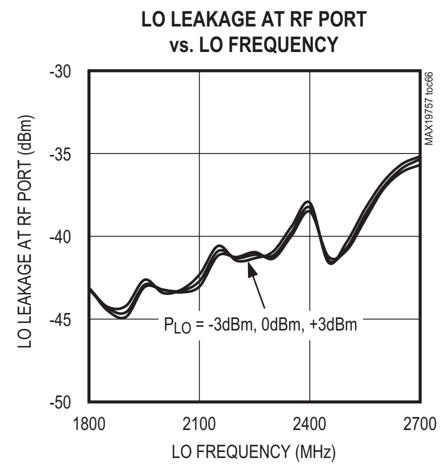
RF-TO-IF ISOLATION vs. RF FREQUENCY

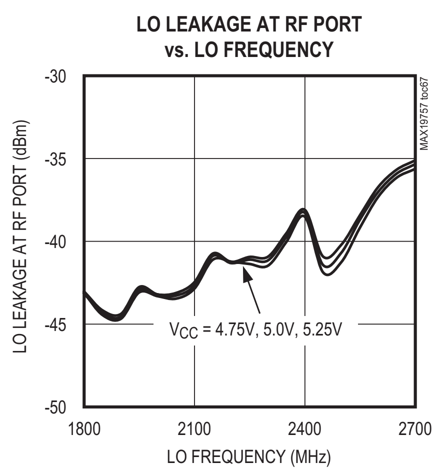


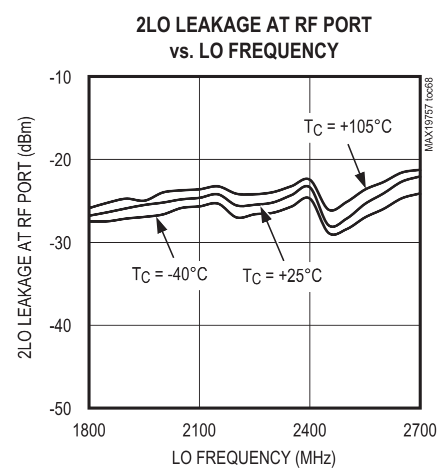
Typical Operating Characteristics (continued)

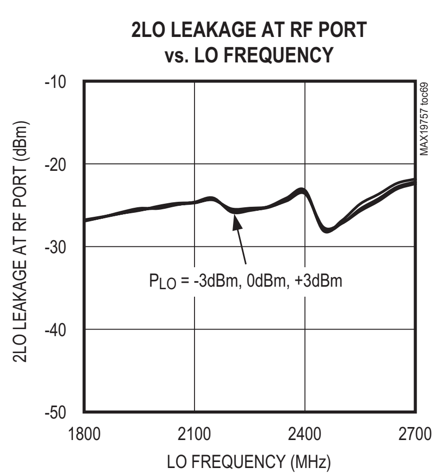
(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 1700MHz to 2800MHz, LO is high-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

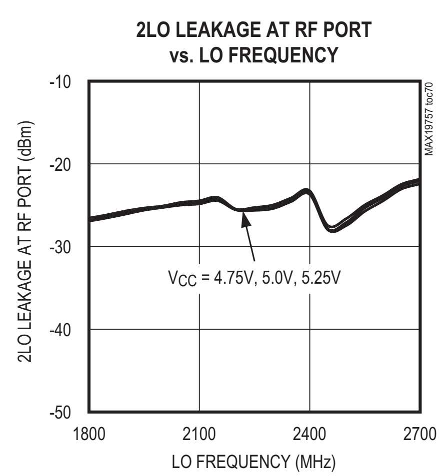






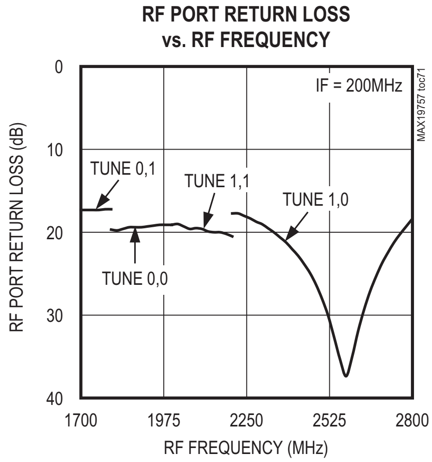


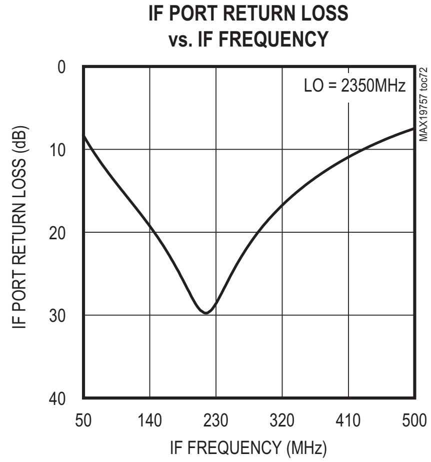


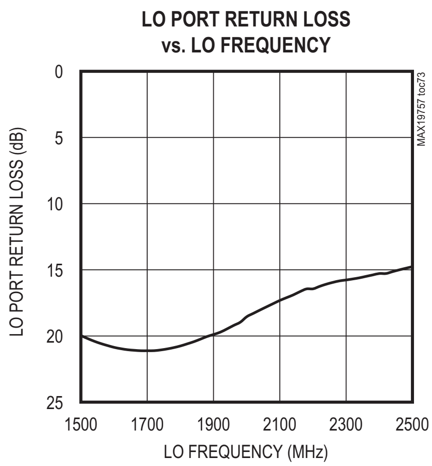


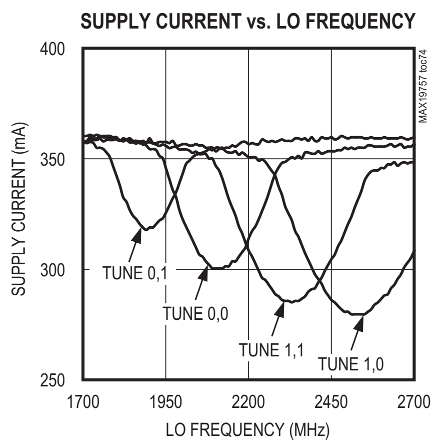
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 5.0V, f_{RF} = 1700MHz to 2800MHz, LO is high-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)





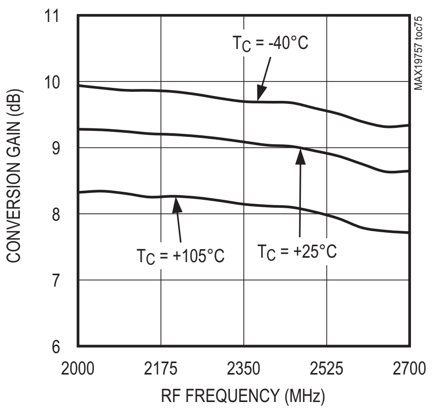




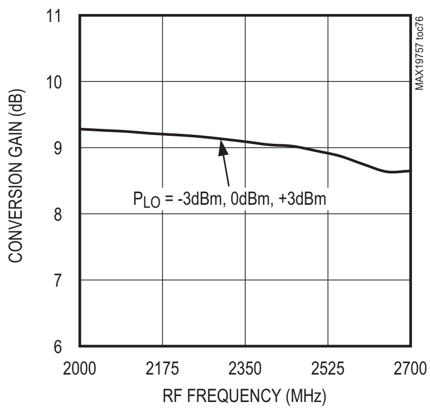
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

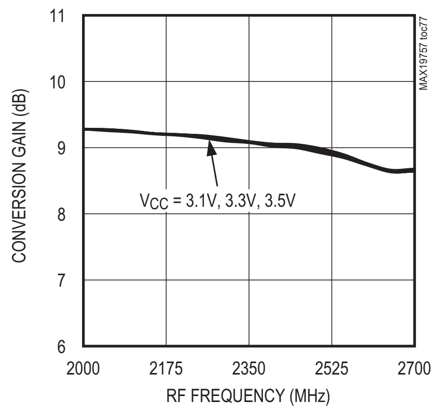
CONVERSION GAIN vs. RF FREQUENCY



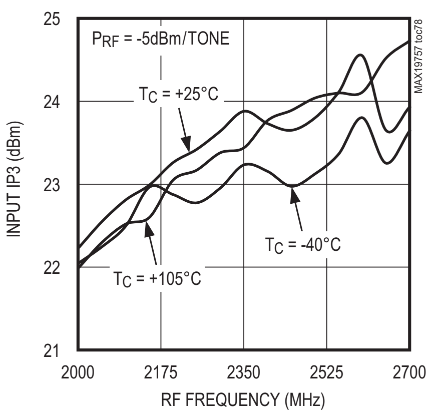
CONVERSION GAIN vs. RF FREQUENCY



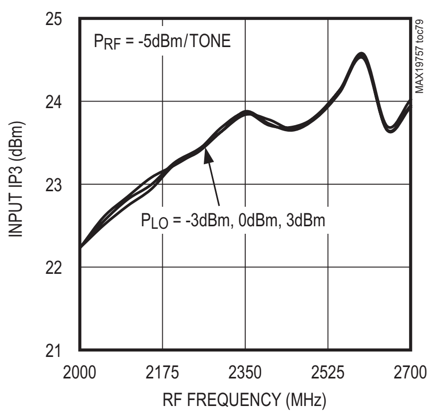
CONVERSION GAIN vs. RF FREQUENCY



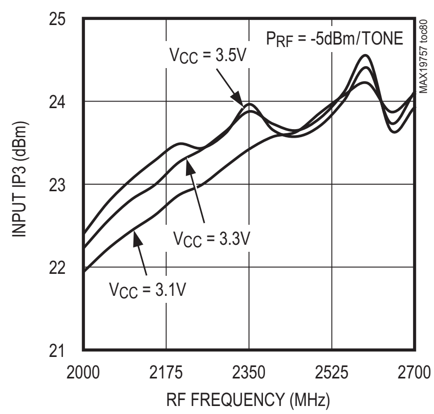
INPUT IP3 vs. RF FREQUENCY



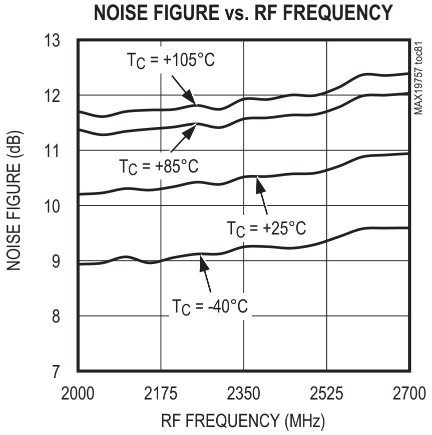
INPUT IP3 vs. RF FREQUENCY



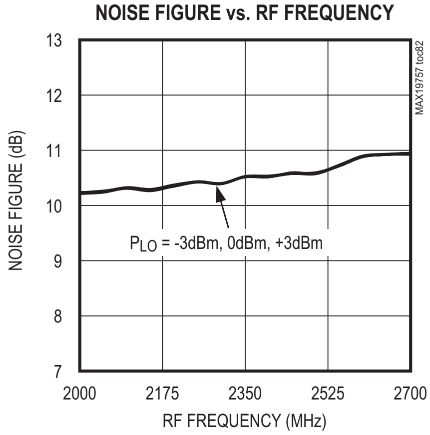
INPUT IP3 vs. RF FREQUENCY



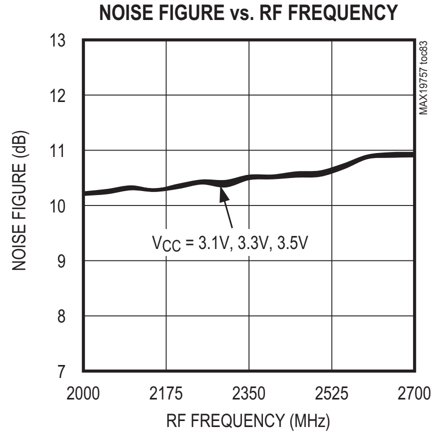
NOISE FIGURE vs. RF FREQUENCY



NOISE FIGURE vs. RF FREQUENCY



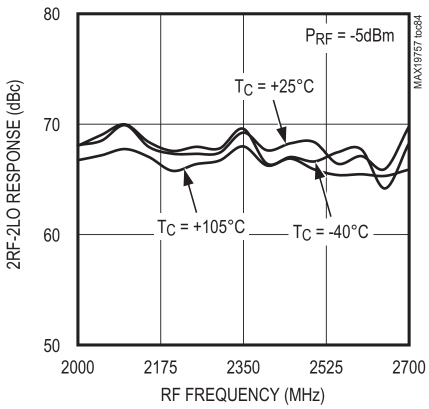
NOISE FIGURE vs. RF FREQUENCY



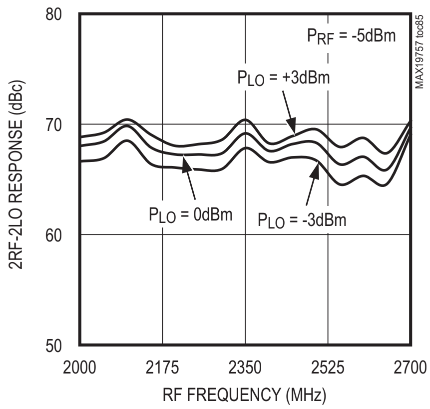
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

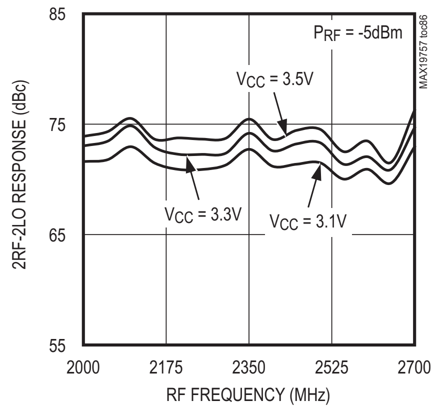
2RF - 2LO RESPONSE vs. RF FREQUENCY



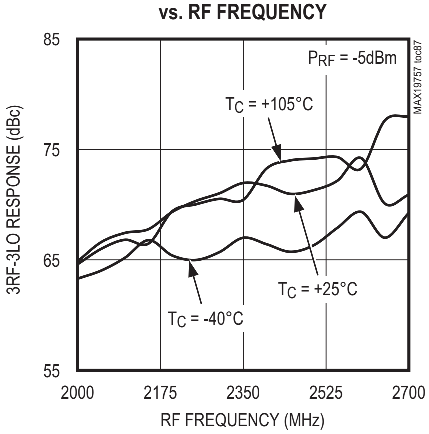
2RF - 2LO RESPONSE vs. RF FREQUENCY



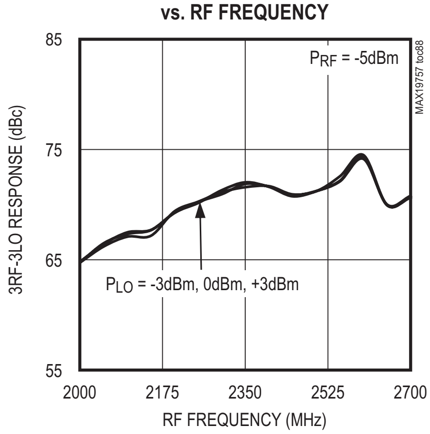
2RF - 2LO RESPONSE vs. RF FREQUENCY



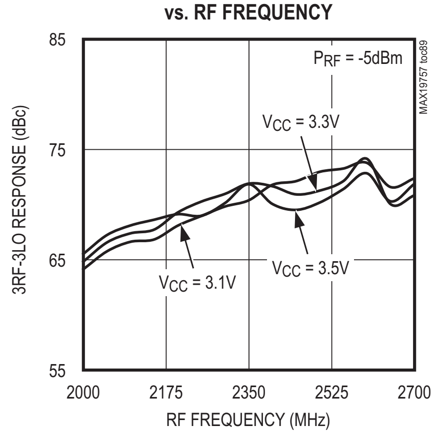
3RF - 3LO RESPONSE vs. RF FREQUENCY



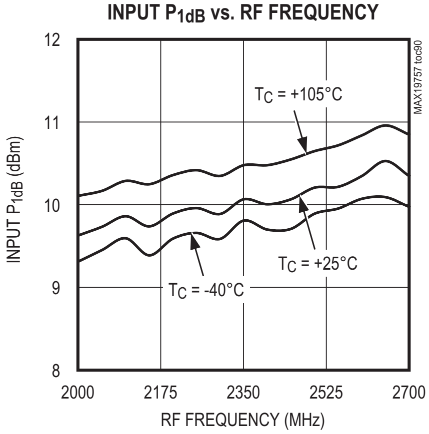
3RF - 3LO RESPONSE vs. RF FREQUENCY



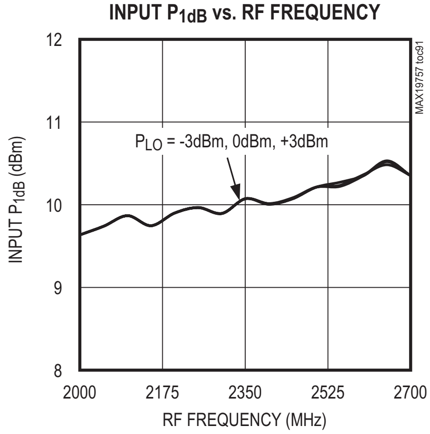
3RF - 3LO RESPONSE vs. RF FREQUENCY



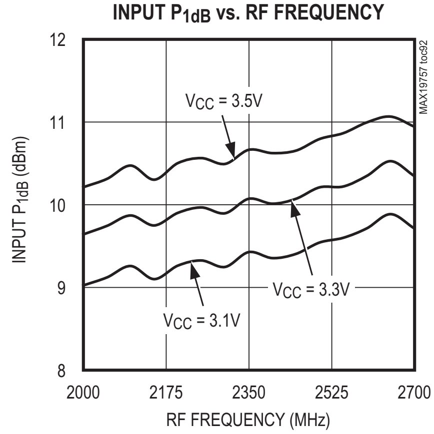
INPUT P_{1dB} vs. RF FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY



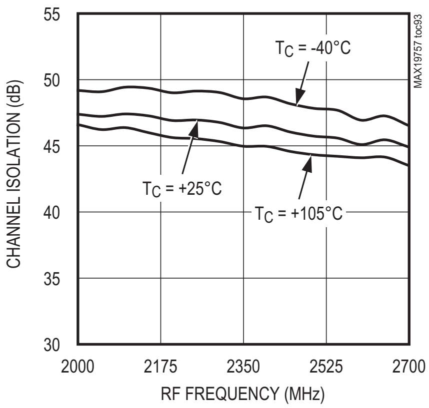
INPUT P_{1dB} vs. RF FREQUENCY



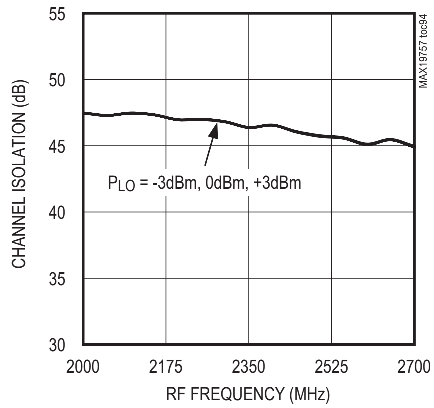
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

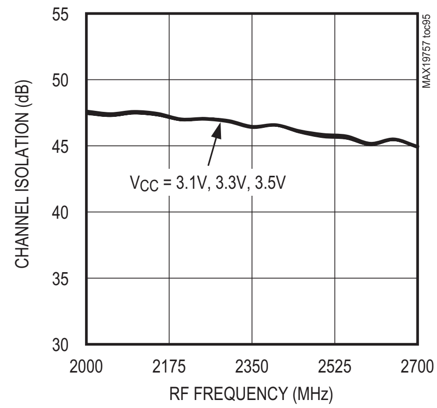
CHANNEL ISOLATION vs. RF FREQUENCY



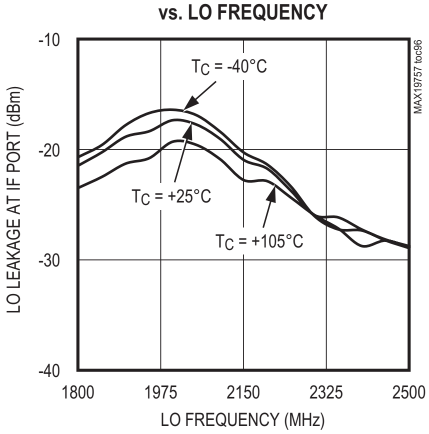
CHANNEL ISOLATION vs. RF FREQUENCY



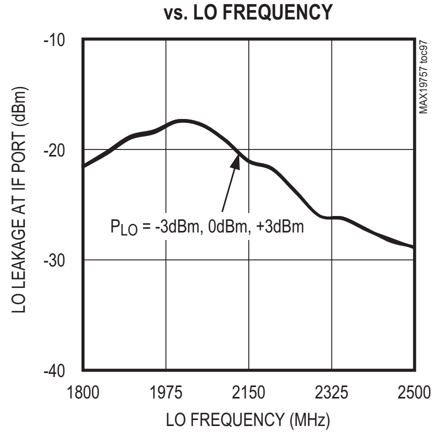
CHANNEL ISOLATION vs. RF FREQUENCY



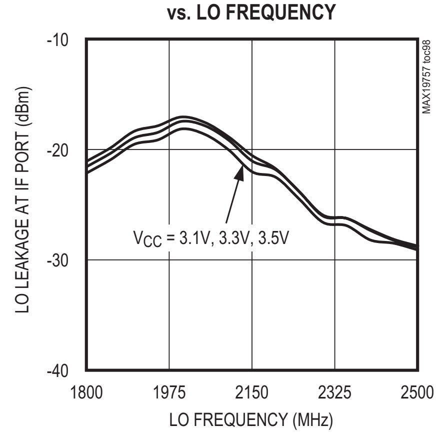
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



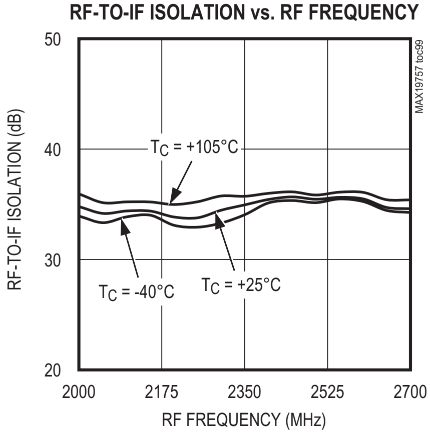
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



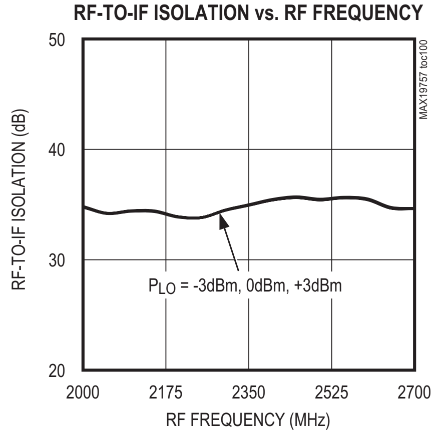
LO LEAKAGE AT IF PORT vs. LO FREQUENCY



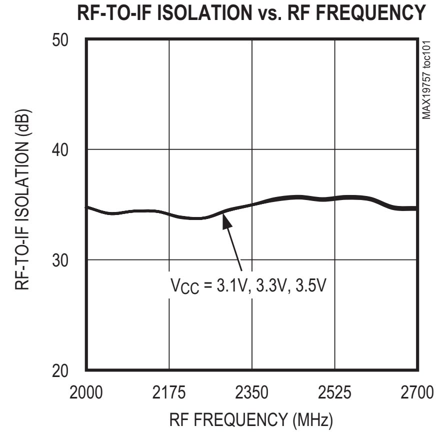
RF-TO-IF ISOLATION vs. RF FREQUENCY



RF-TO-IF ISOLATION vs. RF FREQUENCY

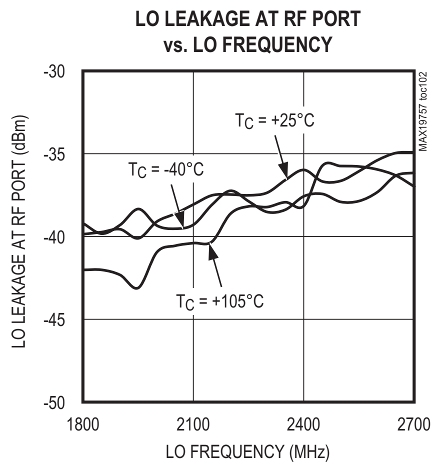


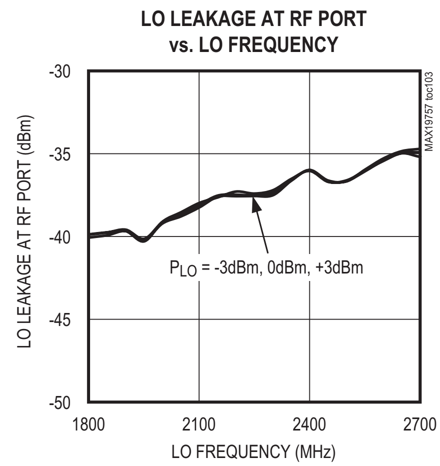
RF-TO-IF ISOLATION vs. RF FREQUENCY

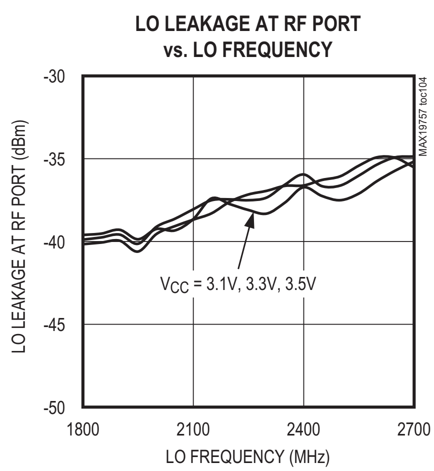


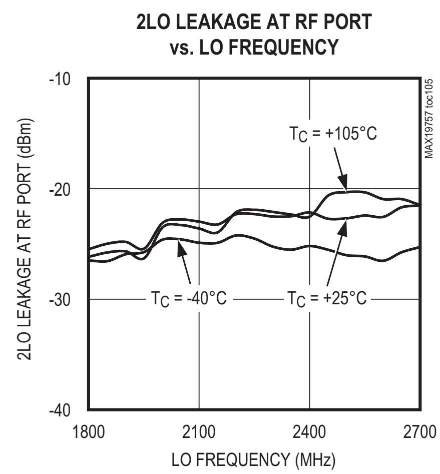
Typical Operating Characteristics (continued)

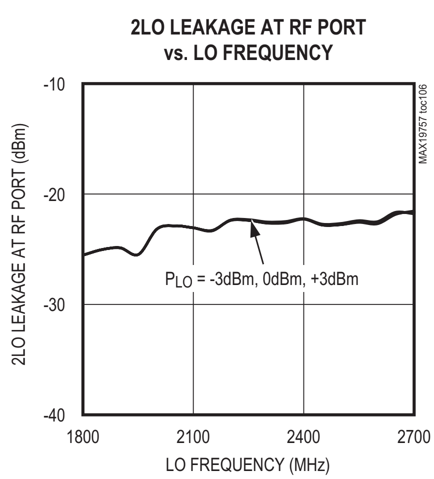
(*Typical Application Circuit*, **V_{CC} = 3.3V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

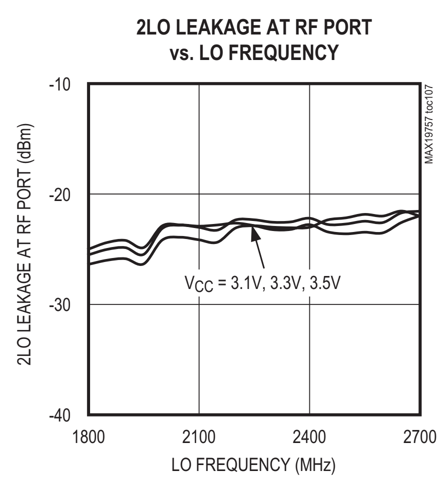






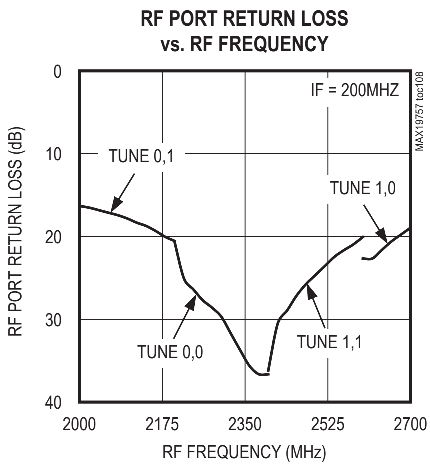


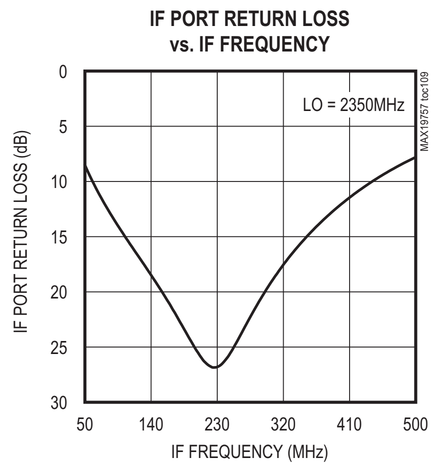


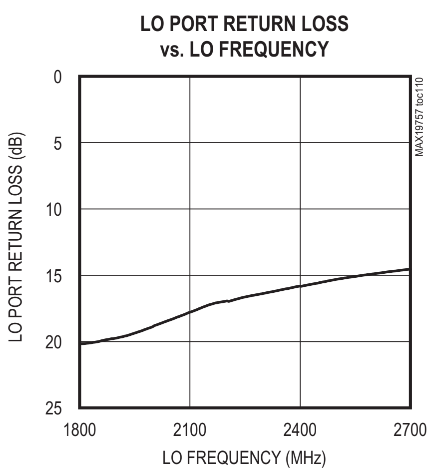


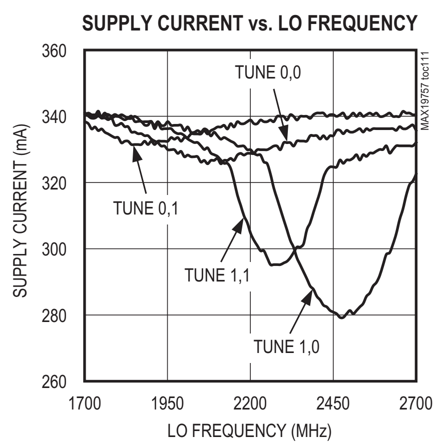
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, **V_{CC} = 3.3V, f_{RF} = 2000MHz to 2700MHz, LO is low-side injected for a 200MHz IF**, P_{RF} = -5dBm, P_{LO} = 0dBm, T_C = +25°C, LO1 driven, LOSEL= 5V, STBY = PD1 = PD2 = GND, LOTUNE1 and LOTUNE2 set per Table 2, unless otherwise noted.)

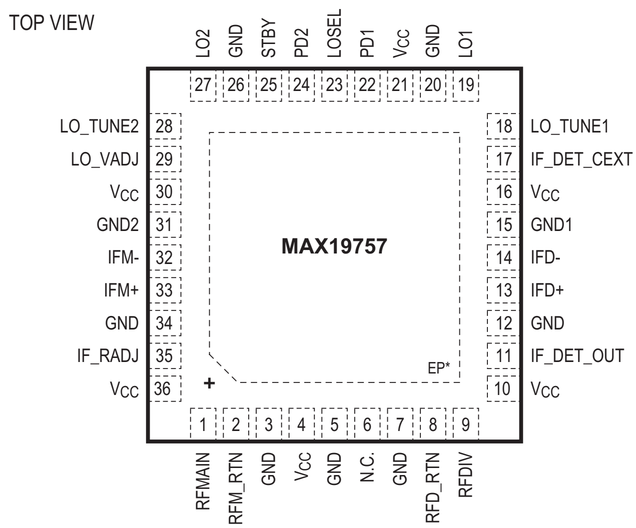








Pin Configuration



TQFN
(6mm x 6mm)

*EXPOSED PAD. INTERNALLY CONNECTED TO GND.

Pin Description

PIN	NAME	FUNCTION
1	RFMAIN	Main Channel RF Input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
2	RFM_RTN	Main Channel RF return. Bypass to GND with capacitor close to the pin.
3, 5, 7, 12, 20, 26, 34	GND	Ground
4, 10, 16, 21, 30, 36	V_{CC}	Power-Supply Input. Connect bypass capacitors as close to the pin as possible.
6	N.C.	No Connection. This pin has no internal connection and can be left open or connected to ground.
8	RFD_RTN	Diversity Channel RF Return. Bypass to GND with capacitor close to the pin.
9	RFDIV	Diversity Channel RF Input. Internally matched to 50Ω; requires an input DC-blocking capacitor.
11	IF_DET_OUT	**If auto-leveling loop is not used leave this pin unconnected.** If auto-leveling is desired connect resistor R2 and R3 to IF_DET_OUT and add a capacitor Cext (Pin 17) to ground (see the *Optional Dynamic Bias Typical Application Circuit*).
13, 14	IFD+, IFD-	Diversity Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC}.
15, 31	GND1, GND2	Connect these pins to a via to ground.
17	IF_DET_CEXT	**If auto-leveling loop is not used leave this pin unconnected.** If auto leveling is used connect a capacitor to ground (see the *Optional Dynamic Bias Typical Application Circuit*). This capacitor sets the detector decay rate.
18, 28	LO_TUNE1, LO_TUNE2	2-Bit LO Tank Tuning. See Table 2 for desired setting internal 50kΩ pulldown resistor.
19	LO1	Local Oscillator 1 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
22, 24	PD1, PD2	Power-Down Control Pin Logic. See Table 1 for desired setting. Internal 50kΩ pulldown resistor.
23	LOSEL	Local Oscillator Select Input. Set LOSEL high to select LO1. Set LOSEL low to select LO2. Internal 50kΩ pulldown resistor.
25	STBY	Standby (Active-High). All Off except Bias and selected LO port. Internal 50kΩ pulldown resistor.
27	LO2	Local Oscillator 2 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
29	LO_VADJ	LO Drive Amplitude Bias Control. Internally biased to V_{REF}. Connect a resistor to VCC.
32, 33	IFM-, IFM+	Main Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC}.
35	IF _RADJ	IF Amplifier Bias Control Mode. Connect a resistor from this pin to ground to set the bias current for the IF amplifiers.
—	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance (see the *Layout Considerations* section.)

Detailed Description

The MAX19757 dual-channel downconverter is designed to provide 8.8dB gain, 25.3dBm input IP3 and 10.4dB NF for a multitude of 1700MHz to 2700MHz basestation receiver applications. With an optimized LO frequency range of 1800MHz to 2600MHz, this mixer supports both high- and low-side LO injection architectures for 1700MHz to 2200MHz and 2000MHz to 2700MHz RF bands, respectively. Independent path shutdown allows the user to save DC power during low-peak usage times or in TDD TX mode.

The device integrates baluns in the RF and LO ports, an LO buffer, two double-balanced mixers, and a pair of differential IF output amplifiers. The MAX19757 requires a typical LO drive of 0dBm and a supply current typically 300mA at band center and 350mA across the RF frequency band to achieve the targeted linearity performance.

Applications Information

Independent Channel Shutdown

Control pins PD1 and PD2 can be used to ***independently*** enable/disable the two mixer channels. Table 1 summarizes the relevant settings for enabling/disabling each channel. Both channels can be switched on and off in unison by tying PD2 to ground and switching PD1. The PD1 and PD2 inputs have an internal 50kΩ pulldown resistor which can be used to set a logic-low if left unconnected.

LO Port Select

As with most of Maxim's Dual Rx mixers, the MAX19757 includes an LO select control (LOSEL) for use in systems with multiple LO synthesizers. LOSEL controls the active LO port selection. Setting LOSEL high (V_{CC}) selects LO port 1 while LOSEL low (ground) selects LO port 2. The LOSEL input has an internal 50kΩ pulldown resistor which can be used to set a logic-low if left unconnected.

LO Buffer Standby Mode (Synthesizer Pulling Prevention Feature)

To minimize LO port disturbances in transceiver systems that reuse the LO for transmit, the active front-end circuitry of the MAX19757 LO port can be left ON while disabling the selected Rx path(s). Toggling the STBY pin high (V_{CC}) will place the selected LO port driver in a constant ON state, ensuring a buffered termination for the external synthesizer during main and/or diversity path shutdowns. Depending on the application, this buffered interface may allow for the elimination of the external buffer that is typically used between the synthesizer and the mixers LO port. The STBY input has an internal 50kΩ pulldown resistor which can be used to set a logic-low if left unconnected.

LO Tune

The MAX19757 employs a resonant LO driver scheme for improved efficiency, as well as an internal leveling control loop (ALC) to hold the internal LO drive level constant. To extend the frequency range of this topology, two bits of tuning are used to adjust the LO tank resonance. Good efficiency is maintained over a typical ±150MHz range around the resonant frequency. Table 2 settings should be used to select the appropriate LO band for best efficiency and performance. DC currents over LO Frequency at the four tune settings can be seen in the *Typical Operating Characteristics* curves. The minimum bias current corresponds to the LO tank resonant point. The internal ALC loop maintains a constant drive amplitude over the range shown in the curves for different settings. The various specifications and guarantees assume that the appropriate LO band is used. The ALC loop includes a bias limit circuit to prevent overdrive when operated at an inappropriate LO frequency. LO_TUNE1 and LO_TUNE2 can be driven dynamically by using external control logic or can be set to Vcc or ground by using a 0Ω resistor on the pins. If driven from external logic, V_{CC} must be applied to the device so as to not overcurrent the on-chip ESD diodes which could damage the part. The LO_TUNE1 and LO_TUNE2 inputs have an internal 50kΩ pulldown resistor which can be used to set a logic-low if left unconnected.

Table 1. Channel Enable/Disable States

Main Channel	Diversity Channel	PD1	PD2
ON	ON	0	0
OFF	OFF	1	0
ON	OFF	0	1
OFF	ON	1	1

Table 2. LO TUNE States

Desired LO Band	LO_TUNE1	LO_TUNE2
< 2000MHz	0	1
≥ 2000MHz to < 2200MHz	0	0
≥ 2200MHz to 2400MHz	1	1
> 2400MHz	1	0

Bias Settings

Since mixer linearity and power are affected by the device's operating points, flexibility was built into the MAX19757 so that the IF and LO bias levels can be adjusted using external resistor sets (see the *Typical Application Circuit*). Customized tradeoffs can thus be made to optimize linearity vs. overall power consumption. The IF quiescent bias is set via the current at pin 35 (the R1 value to ground), and the internal LO drive amplitude by the current at pin 29.

IF Amplifier Bias Adjustments

Pin 35 of the device, IF_RADJ, must have a resistor to ground for the IF amp to function. A nominal IF bias of 80mA is obtained with a 4.87kΩ resistor used for R1. A smaller resistance increases the IF bias. Conversely, a larger resistance decreases the IF quiescent bias; the IF amp bias current through L1/L2 or L4/L5 of the *Typical Application Circuit* should not exceed 130mA.

LO Buffer Bias Adjustments

The internal LO target amplitude can be altered by sinking or sourcing sink current at the LO_VADJ pin. To ***increase*** the static LO drive, remove R3 from V_{CC} and connect it to ground. The value of R3 should be greater than 10KΩ for this increased drive operation. To reduce overall power consumption by ***decreasing*** the LO drive, connect R3 from pin 29 to V_{CC}. The *Typical Application Circuit* is configured for this reduced power consumption mode.

Static Bias Operation

As outlined above, external resistor sets can be chosen to set the bias schemes for the MAX19757's LO and IF amplifier circuits. Select R1 and R3 to set the IF and LO biases per the guidance provided above. See the *Typical Application Circuit* for details surrounding the suggested configurations.

Using the static bias mode will ensure that the mixer delivers a constant level of linearity performance with a constant level of power dissipation, regardless of the signal power present on the mixer's RF ports.

Dynamic Bias Operation

The *static* biasing schemes outlined above provide a constant level of linearity for a given current draw. However, in many base station receiver applications, it may not be necessary to maintain exceptionally high levels of linearity performance at all times. IIP3 linearity is critical for base station receivers when the radio is operating in the presence of interfering blockers. Due to the intermittent nature of these blocking signals, there exists an opportunity to relax the mixer's IIP3 performance when the blockers are not present. This relaxation of linearity implies that the mixer's overall current consumption can be throttled back by a commensurate amount.

The MAX19757 capitalizes on this opportunity by employing a novel dynamic biasing scheme which detects the presence of blockers in the IF domain, and increases the biases to the IF and LO amplifiers automatically. The use of the feature is completely optional (see *Optional Dynamic Bias Typical Application Circuit*). In this figure, a few additional components and connections are added or modified to enable this feature. Omitting these additional components will force the circuit to revert back to the *static* biasing scheme.

The MAX19757 includes a simple log amp detector that senses the presence of a high-level signal on both of the IF paths. **IF_DET_OUT** (pin 11) will yield a signal that swings above or below the internal 1.2V bandgap reference and can therefore be used to source or sink current into the IF and/or LO bias adjust pins. As the IF signal *increases*, the IF_DET_OUT output decreases down to its 0.4V limit. Conversely, as the IF signal *decreases*, the IF_DET_OUT output increases to its upper limit of 1.7V. The nominal bias crossing corresponds to an IF output level of approximately +10dBm.

The **IF_DET CEXT** pin (17) is used to set the attack / decay times of the detector. The effective resistance at this pin is ~ 30KΩ. Select a Cext value appropriate for the slowest system data rate.

Typical values for dynamic control of both the IF and LO are as follows: **R1 = 4.64K, R2 = 5K, R3 = 10K, and Cext = 1µF**. Under small-signal conditions, the chip power will decrease ~25% and increase to about +30% with an IIP3 increase of ~3dBm.

Note that the attack/decay times will be affected when the individual paths are subjected to the shutdown states described in Table 1. Contact the factory for details.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground-pin traces directly to the exposed pad underneath the package. This pad **MUST** be connected to the ground plane of the board by using multiple vias under the device to provide the best RF and thermal conduction path. Solder the exposed pad on the bottom of the device package to a PCB.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high frequency circuit stability. Bypass each VCC pin with capacitors placed as close as possible to the device. Place the smallest capacitor closest to the device. See the *Typical Application Circuit* and Table 3 for details.

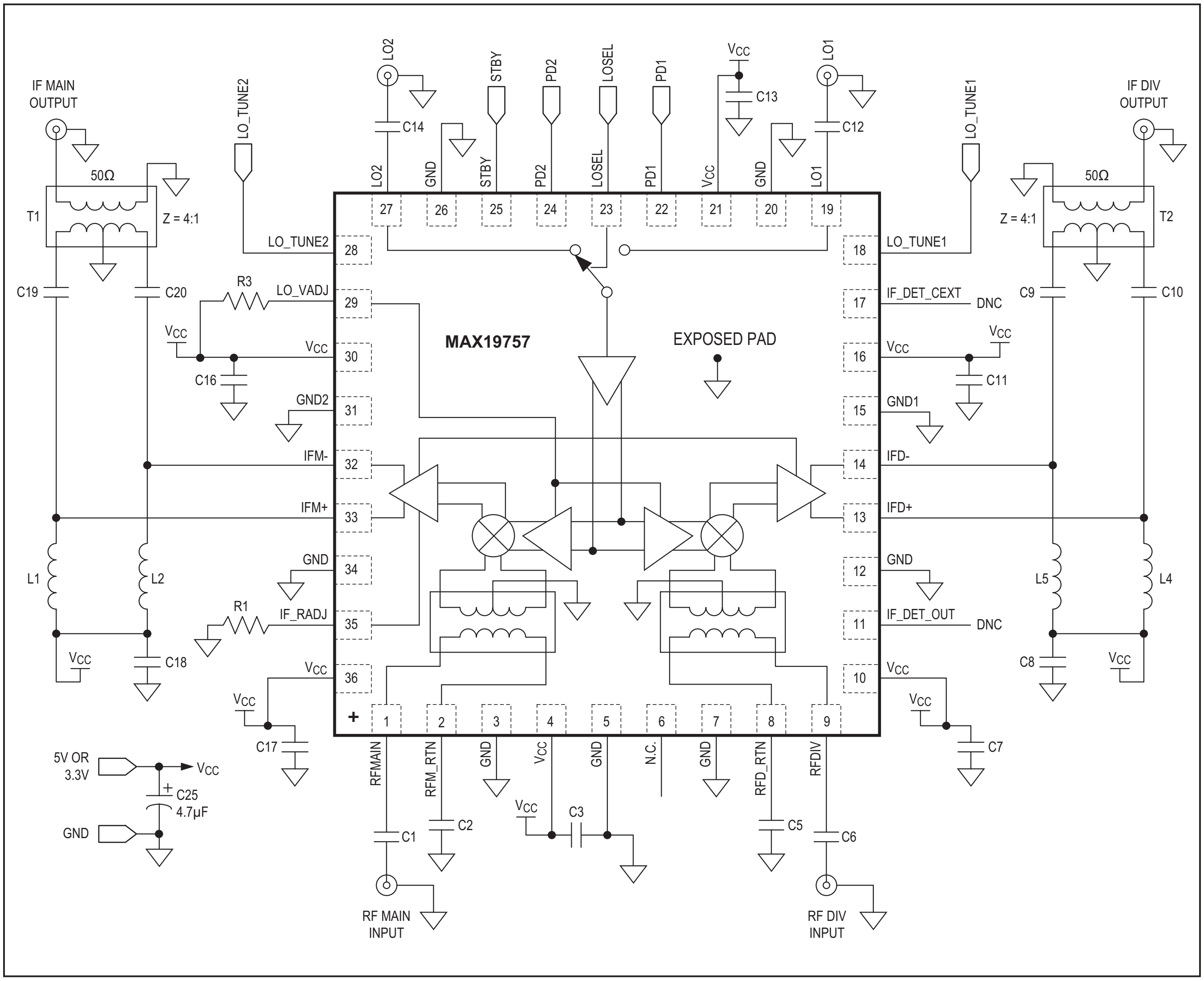
Table 3. Typical Application Circuit Component Values

DESIGNATION	QTY	DESCRIPTION
C1, C6	2	3.0pF ±0.1pF 50V C0G CER CAP (0402) Murata: GRM1555C1H3R0B
C12, C14	2	5.0pF ±0.1pF 50V C0G CER CAP (0402) Murata: GRM1555C1H5R0B
C2, C3, C5, C7–C11, C13, C16–C20	14	0.01µF ±10% 25V X7R CER CAP (0402) Murata: GRM155R71E103K
C25	1	4.7µF ±10% 16V X7R CER CAP (1206) Murata: GRM31CR71C475K
L1, L2, L4, L5	4	330 nH ±5% Wire Wound IND (0805) Coilcraft: 0805CS-331XJLC
R1	1	4.87KΩ ±1% Resistor (0402) Any
R3	1	154KΩ ±1% Resistor (0402) Any
T1, T2	2	Mini Circuits TC4-1W-17
U1	1	Maxim MAX19757ETX+

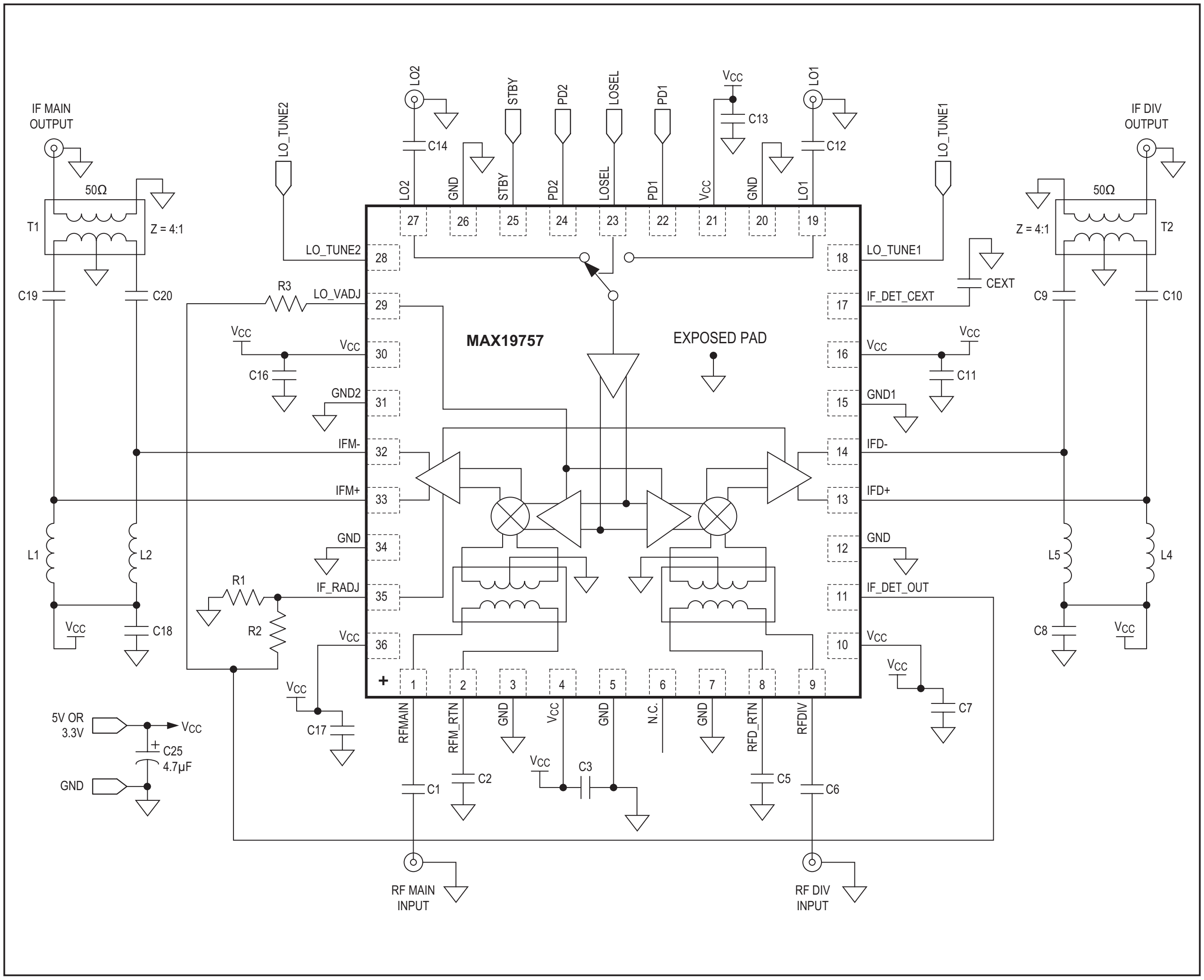
Exposed Pad RF and Thermal Considerations

The exposed pad (EP) of the device’s 36-pin thin QFN package provides a low thermal-resistance path to the die. It is important that the PCB on which the IC is mounted be designed to conduct heat from this contact. In addition, provide the EP with a low-inductance RF ground path for the device. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. Soldering the pad to ground is also critical for efficient heat transfer. Use a solid ground plane wherever possible.

Typical Application Circuit



Optional Dynamic Bias Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX19757ETX+	-40°C to +105°C	36 TQFN-EP*
MAX19757ETX+T	-40°C to +105°C	36 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

T = Tape and reel.

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
36 TQFN	T3666+2	**21-0141**	**90-0049**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.