

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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H5N5006LD, H5N5006LS, H5N5006LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

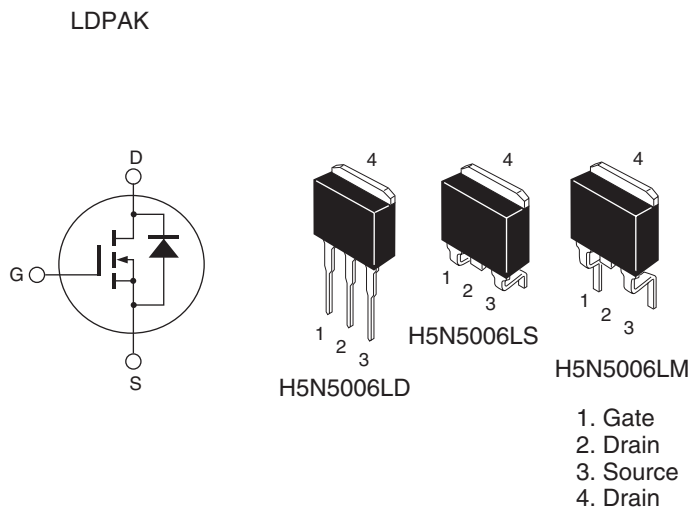
ADE-208-1549 (Z)

Rev.0
Aug.2002

Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge
- Avalanche ratings

Outline



Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Value | Unit |
|--|---------------------------------|-------------|------|
| Drain to source voltage | V_{DSS} | 500 | V |
| Gate to source voltage | V_{GSS} | ±30 | V |
| Drain current | I_D | 3.5 | A |
| Drain peak current | I_D (pulse) ^{Note 1} | 14 | A |
| Body-drain diode reverse drain current | I_{DR} | 3.5 | A |
| Avalanche current | I_{AP} ^{Note 3} | 3.5 | A |
| Channel dissipation | P_{ch} ^{Note 2} | 50 | W |
| Channel to case thermal impedance | θ_{ch-c} | 2.5 | °C/W |
| Channel temperature | T_{ch} | 150 | °C |
| Storage temperature | T_{stg} | -55 to +150 | °C |

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ C$

3. $T_{ch} \leq 150^\circ C$

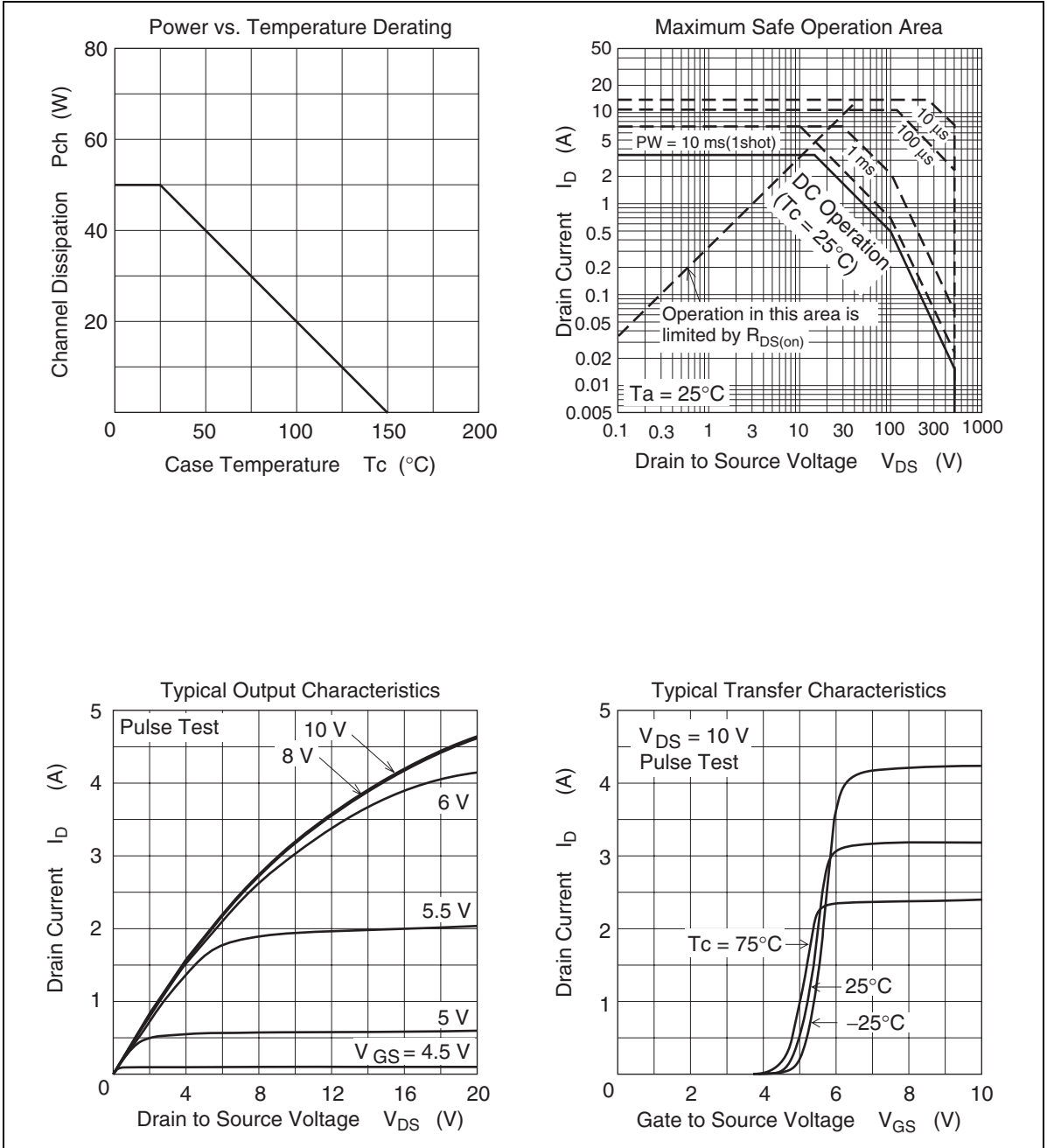
Electrical Characteristics

(Ta = 25°C)

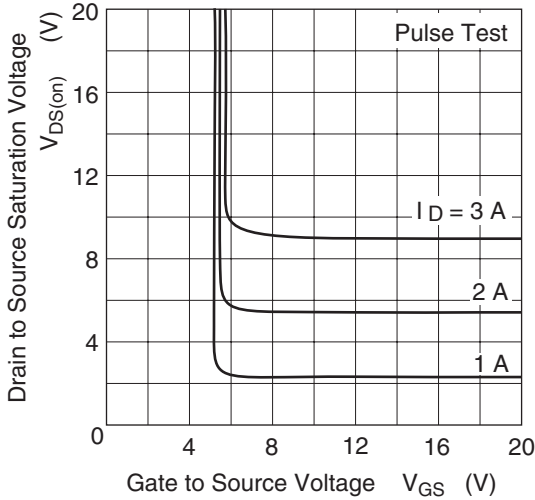
| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|---------------|-----|------|-----------|---------------|--|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | 500 | — | — | V | $I_D = 10 \text{ mA}$, $V_{GS} = 0$ |
| Gate to source leak current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 500 \text{ V}$, $V_{GS} = 0$ |
| Zero gate voltage drain current | I_{GSS} | — | — | ± 0.1 | μA | $V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | 3.0 | — | 4.5 | V | $V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$ |
| Forward transfer admittance | $ y_{fs} $ | 1.8 | 3.0 | — | S | $I_D = 1.75 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4} |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 2.5 | 3.0 | Ω | $I_D = 1.75 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4} |
| Input capacitance | C_{iss} | — | 365 | — | pF | $V_{DS} = 25 \text{ V}$ |
| Output capacitance | C_{oss} | — | 35 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | C_{rss} | — | 8 | — | pF | $f = 1 \text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | — | 20 | — | ns | $V_{DD} \cong 250 \text{ V}$, $I_D = 1.75 \text{ A}$ |
| Rise time | t_r | — | 13 | — | ns | $V_{GS} = 10 \text{ V}$ |
| Turn-off delay time | $t_{d(off)}$ | — | 48 | — | ns | $R_L = 143 \Omega$ |
| Fall time | t_f | — | 14 | — | ns | $R_g = 10 \Omega$ |
| Total gate charge | Q_g | — | 14 | — | nC | $V_{DD} = 400 \text{ V}$ |
| Gate to source charge | Q_{gs} | — | 2 | — | nC | $V_{GS} = 10 \text{ V}$ |
| Gate to drain charge | Q_{gd} | — | 8 | — | nC | $I_D = 3.5 \text{ A}$ |
| Body-drain diode forward voltage | V_{DF} | — | 0.85 | 1.3 | V | $I_F = 3.5 \text{ A}$, $V_{GS} = 0$ |
| Body-drain diode reverse recovery time | t_{rr} | — | 280 | — | ns | $I_F = 3.5 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$ |
| Body-drain diode reverse recovery charge | Q_{rr} | — | 0.8 | — | μC | |

Notes: 4. Pulse test

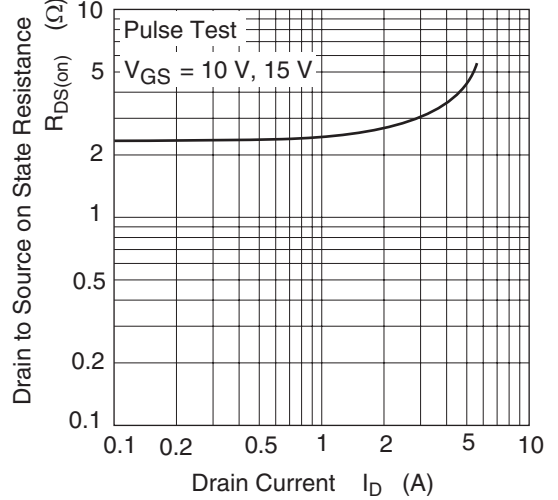
Main Characteristics



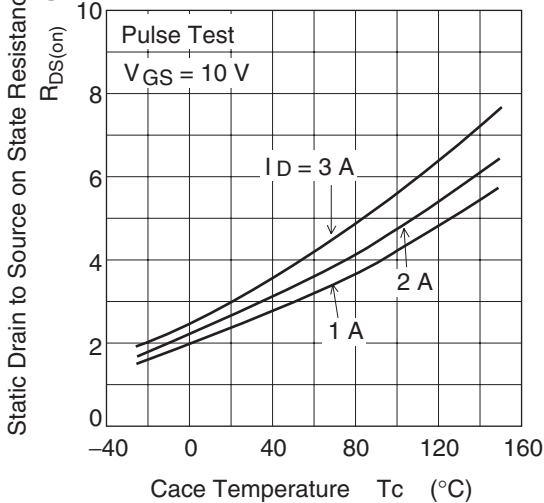
Drain to Source Saturation Voltage vs. Gate to Source Voltage



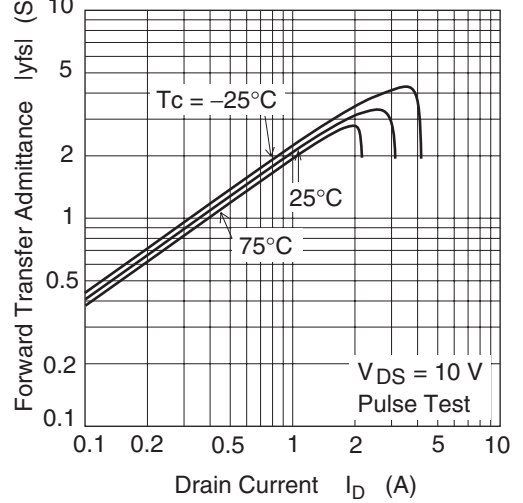
Static Drain to Source on State Resistance vs. Drain Current



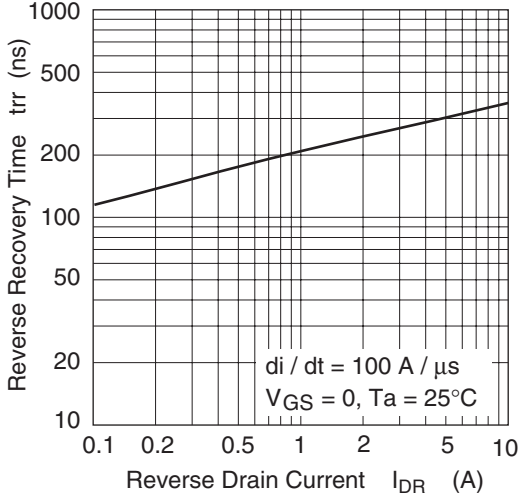
Static Drain to Source on State Resistance VS. Temperature



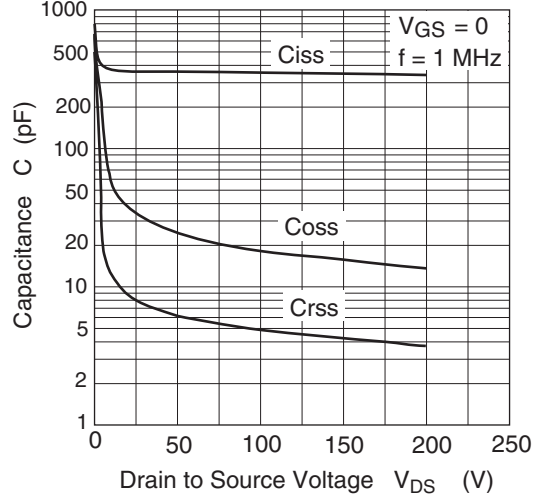
Forward Transfer Admittance vs. Drain Current



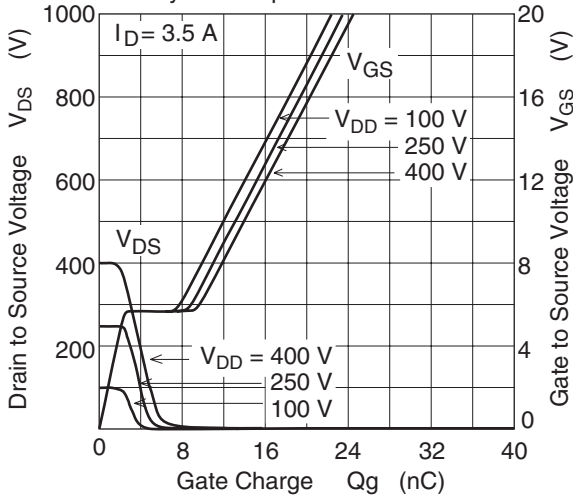
Body-Drain Diode Reverse Recovery Time



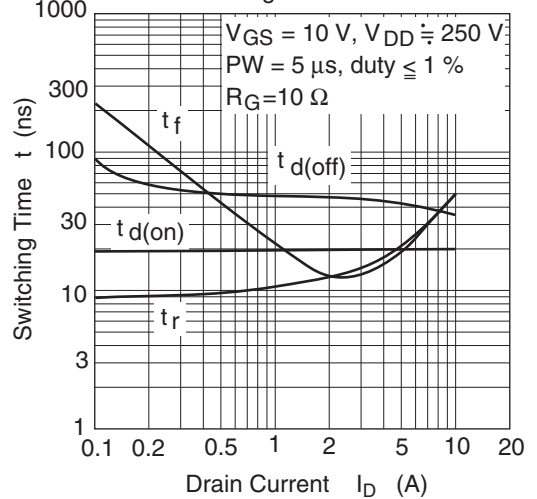
Typical Capacitance vs. Drain to Source Voltage



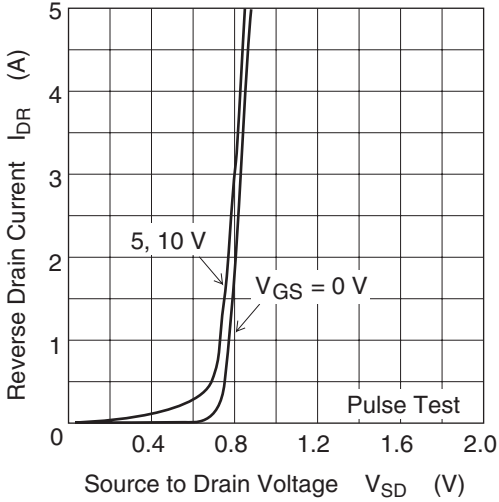
Dynamic Input Characteristics



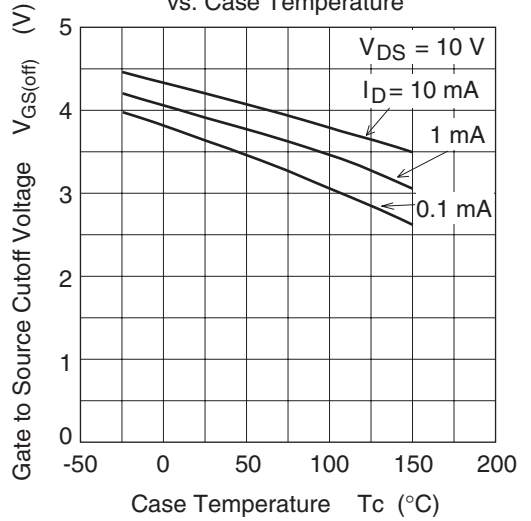
Switching Characteristics



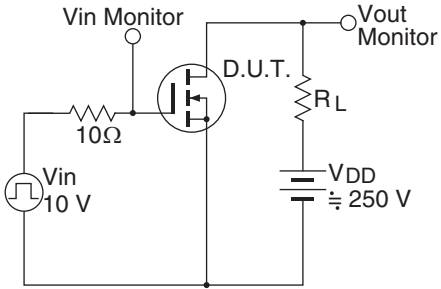
Reverse Drain Current vs. Source to Drain Voltage



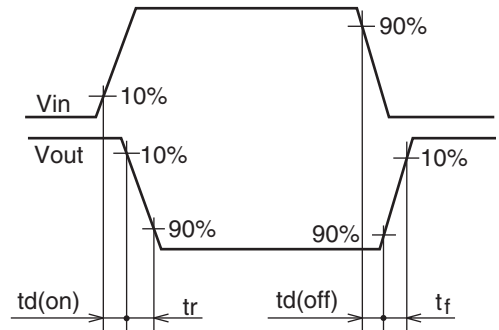
Gate to Source Cutoff Voltage vs. Case Temperature

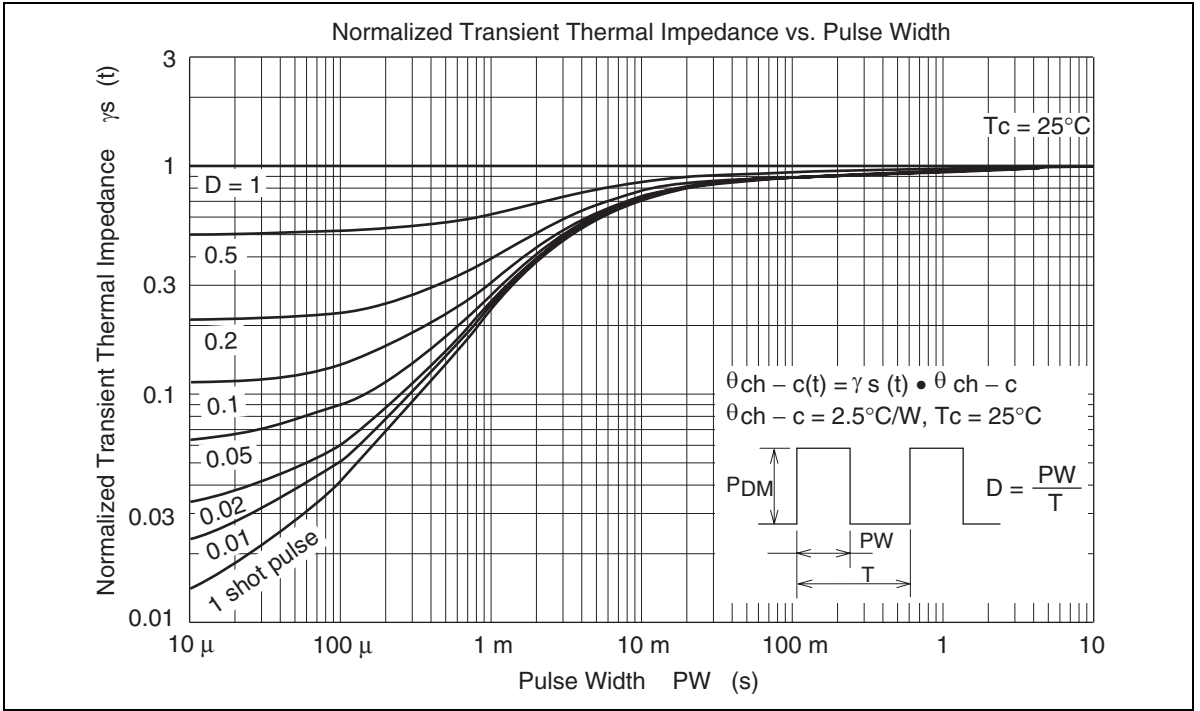


Switching Time Test Circuit



Waveform

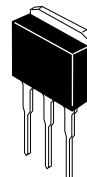
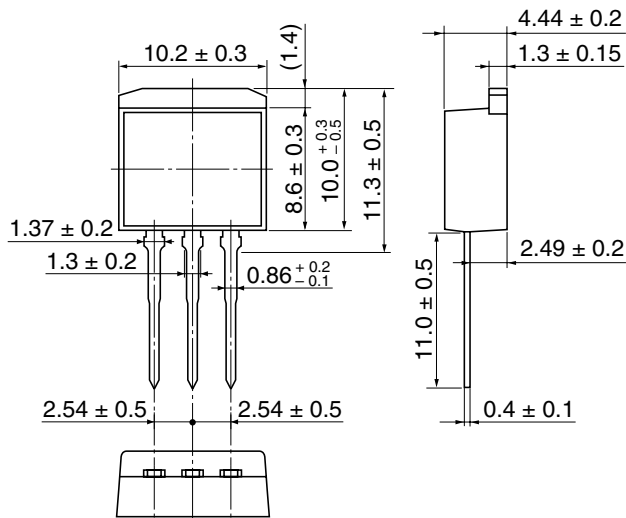




Package Dimensions

• H5N5006LD

Unit: mm

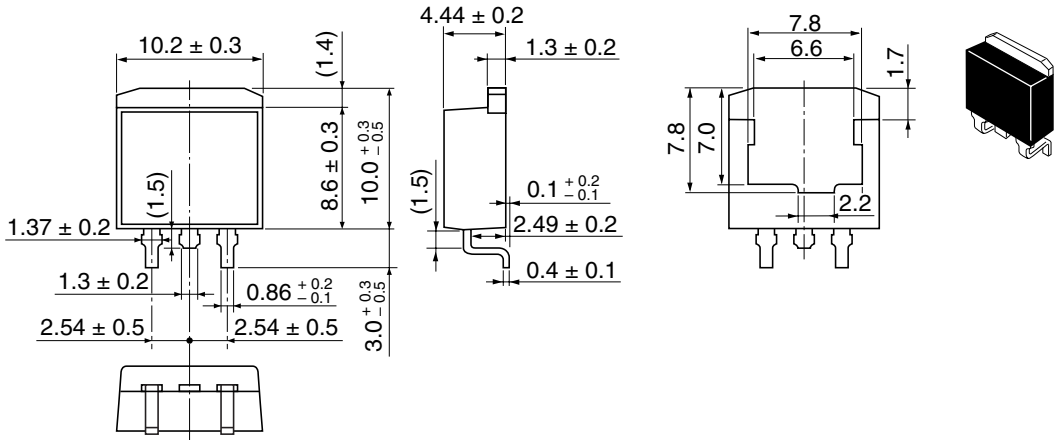


| | |
|------------------------|-----------|
| Hitachi Code | LDPAK (L) |
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 1.4 g |

H5N5006LD, H5N5006LS, H5N5006LM

• H5N5006LS

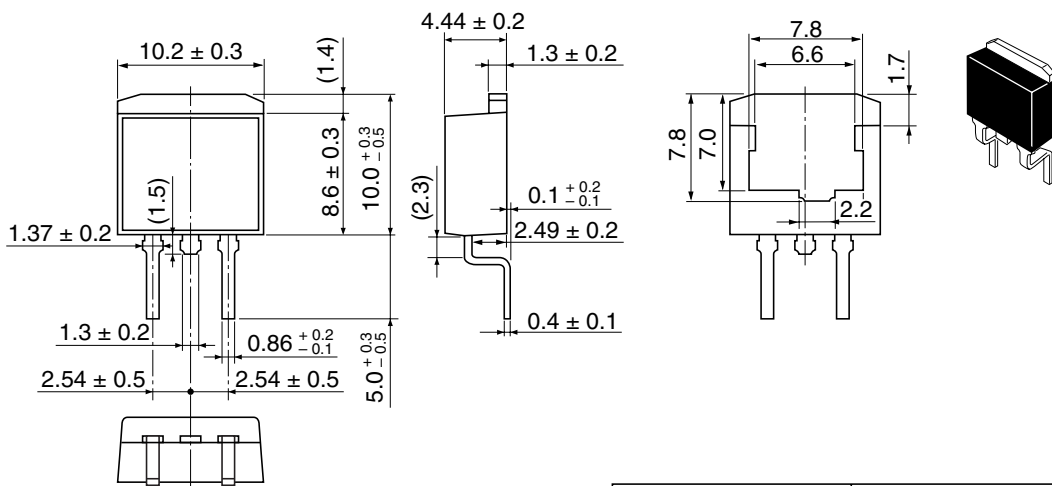
Unit: mm



| | |
|------------------------|----------------|
| Hitachi Code | LDBPAK (S)-(1) |
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 1.3 g |

• H5N5006LM

Unit: mm



| | |
|------------------------|----------------|
| Hitachi Code | LDBPAK (S)-(2) |
| JEDEC | — |
| JEITA | — |
| Mass (reference value) | 1.35 g |

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Sales Offices

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: (03) 3270-2111 Fax: (03) 3270-5109

URL <http://www.hitachisemiconductor.com/>

For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe Ltd.
Electronic Components Group
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585200

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straße 3
D-85622 Feldkirchen
Postfach 201, D-85619 Feldkirchen
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00
Singapore 049318
Tel: <65>-6538-6533/6538-8577
Fax: <65>-6538-6933/6538-3877
URL: <http://semiconductor.hitachi.com.sg>

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road
Hung-Kuo Building
Taipei (105), Taiwan
Tel: <886>-(2)-2718-3666
Fax: <886>-(2)-2718-8180
Telex: 23222 HAS-TP
URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon Hong Kong
Tel: <852>-2735-9218
Fax: <852>-2730-0281
URL: <http://semiconductor.hitachi.com.hk>

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