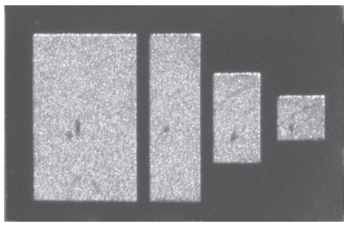
Thin Film Binary MOS Capacitors



Product may not be to scale

The CBA MOS capacitor chips each contain four different capacitors in binary increments allowing the user many choices in value selection. Two versions of CBA capacitors are available: one with a total capacitance of 3.75pF and one with a total capacitance of 15pF.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The CBAs are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- User value selection
- Four capacitors with common connection
- Capacitance range: 0.25pF to 15pF in binary increments
- Dielectric: silicon dioxide
- Chip size: 0.019 x 0.030 inches
- Substrate: silicon with gold backing

APPLICATIONS

Vishay EFI CBA binary MOS multi-value capacitor chips are designed for hybrid packages in which microwave circuits are to be trimmed. This is done on the CBA chips by selecting the bonding pad for the required capacitance and wire-bonding by conventional techniques.

WV (DC) VALUES AND TOLERANCES

CAPACITOR MODEL	CBA 3.75pF	CBA 15pF
Total capacitance	3.75pF	15pF
Individual capacitance	0.25pF, 0.50pF, 1.0pF, 2.0pF	1.0pF, 2.0pF, 4.0pF, 8.0pF
Tolerance	± 25%	± 10%
DC Working voltage	100V	30V

STANDARD ELECTRICAL SPECIFICATIONS

PARAMETER	
Peak voltage at + 25°C	1.5 x working voltage
Dissipation factor 1kHz, $1V_{rms}$, + 25°C	0.1% maximum MOS
Q at 1mHz, $50mV_{rms}$, + 25°C	1000 minimum
TCC, - 55°C to + 150°C	+ 15 ± 25ppm/°C
Insulation resistance at working voltage, + 25°C	10^9 minimum
Operating temperature range	- 55°C to + 150°C
Thermal shock	± 0.25% + 0.25pF maximum ΔC/C
Moisture resistance, MIL-STD-202, Method 106	± 1.0% + 0.25pF maximum ΔC/C
Short time overload, + 25°C, 5 seconds; 1.5 x working voltage	± 0.25% + 0.25pF maximum ΔC/C
High temperature exposure: 100 hours at + 150°C ambient	± 0.25% + 0.25pF maximum
Life, MIL-STD-202, Method 108, Condition D, + 125°C ambient, 1000 hours at working voltage	± 2.0% + 0.25pF maximum ΔC/C

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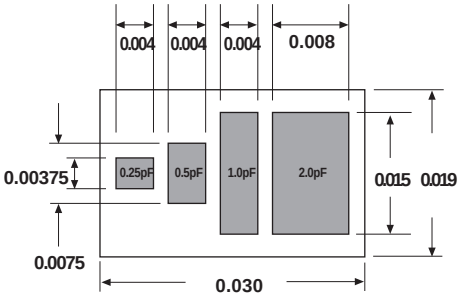
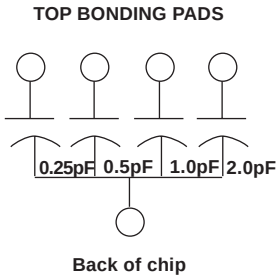
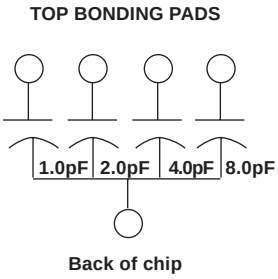
CONFIGURATIONS in inches



SCHEMATIC





MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.019 x 0.030 ± 0.002 (0.48 x 0.75 ± 0.05mm)
Chip thickness	0.010 ± 0.003 (0.25 ± 0.08mm)
Chip substrate material	Semiconductor Silicon
Dielectric	Silicon dioxide (MOS)
Bonding pads	10kÅ minimum aluminum
Backing	3kÅ minimum gold

OPTIONS: Gold bonding pads 15 kÅ minimum
Other value combinations available
Consult Applications Engineer

ORDERING INFORMATION

Example: 100% visualled, 3.75pF ± 25%, Aluminum Pads, Class H

P/N:	**W** INSPECTION /PACKAGING	**CBA** PRODUCT FAMILY	**004** PROCESS CODE	**3750** CAPACITANCE VALUE (pF)	**C** MULTIPLIER CODE	**L** TOLERANCE CODE
	W = 100% visually inspected parts per MIL-STD-883 **X** = Sample, visually inspected loaded in matrix trays (4% AQL)		**004** = CBA	Use first 4 significant digits of the capacitance (C_T)	**C** = 0.001 **B** = 0.01 **A** = 0.1 **0** = 1 **1** = 10	**K** = 10% **M** = 20% **L** = 25% **N** = 50%