Advanced Analog

a division of Intech

RGB DAC 3405S Series

MONOLITHIC CMOS, TRIPLE 4-BIT VIDEO DAC WITH LOOKUP TABLE

DESCRIPTION

The RGB DAC 3405S Series combines three video speed digital-to-analog converters, three static RAM arrays organized 32 x 4, internal temperature compensated reference and all the control lines necessary for a full graphics/color monitor interface. All this is contained in a single monolithic low power CMOS/TTL compatible IC.

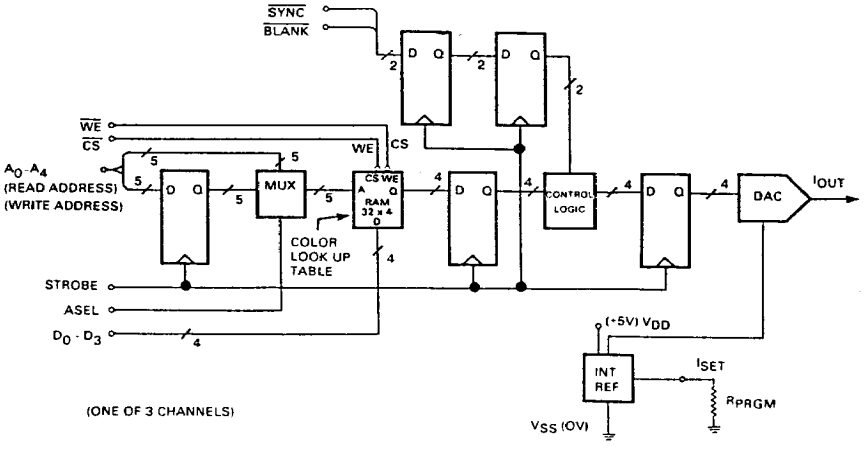
In a typical application, each of three independent red, green and blue analog outputs will drive a 75 ohm source and load terminated coax that supplies a high resolution video monitor with a palette of 4096 colors. Any of 32 colors are available at a 60 MHz rate.

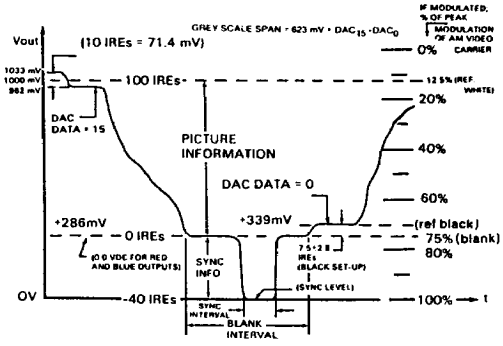
The RGB DAC 3405S Series can be directly interfaced to CMOS, HCT, TTL and advanced TTL logic families. It is also capable of developing signals in conformance with EIA standards 170/343. Features include small size, synchronous data and control lines for minimal skew and glitch, built-in temperature compensated reference, guaranteed linearity, offset, and gain; plus superior temperature coefficients to make the RGB DAC 3405S Series a state-of-the-art industry leader.

FEATURES

- Triple 32 x 4 SRAM lookup table
- Internal reference, temperature compensated
- Small size
- Single +5V operation
- Fully synchronous operation for minimal skew
- Low power CMOS circuitry
- Ideal for videotex systems

BLOCK DIAGRAM





Composite Video Output

NTSC COMPOSITE PICTURE VOLTAGE WAVEFORM DEVELOPED FROM RS170 AND CCIR.

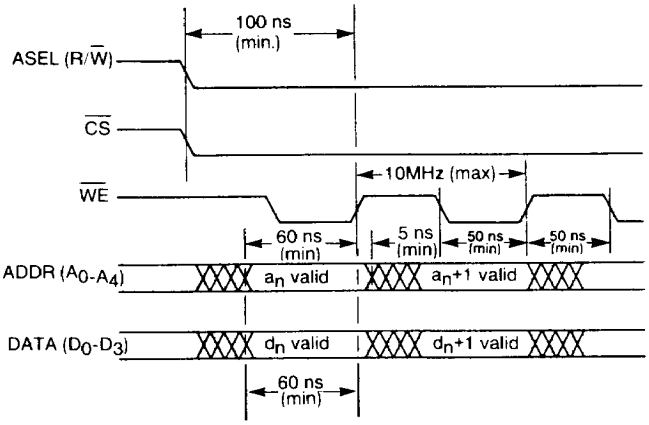
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS	
Supply Voltage (V_{DD}-V_{SS})	6 VDC max.
Supply current (75Ω loads)	60 mA max.
Full Scale output current	40 mA max.
Drive into any digital input (clamped)	±10 mA max.
Output voltage compliance range (each channel)	-0.3 to +2.5 volts instantaneous
Logic input voltage range "0"	V_{SS} -0.3 Vdc min.
Logic input voltage range "1"	V_{DD} +0.3 Vdc max.
Ambient operating temperature range	0°C to +70°C
Ambient storage temperature range	-55°C to +125°C

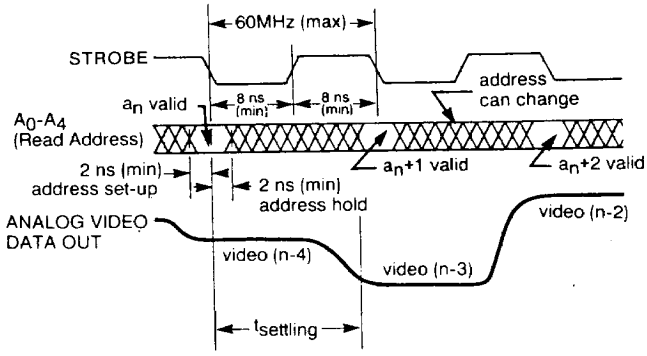
Recommended Operating Conditions	Min	Typ	Max	Units
Supply voltage (V_{DD}-V_{SS})	4.75	5.00	5.25	Vdc
R_L (output load)		37.5		Ω
R_{SET}		2.9		KΩ

Characteristics	Min	Typ	Max	Units
INPUT CHARACTERISTICS				
Digital		4		Bits
Coding		Binary		
Compatibility		TTL or CMOS		
Loading		One equivalent HCT unit load		
Logic "0" @ 10μA max.)	V_{SS}	0.4	0.8	V_{DC}
Logic "1" @ 10μA max.	2.0	2.4	V_{DD}	V_{DC}
OUTPUT CHARACTERISTICS				
Offset all current sources OFF		±1.0	±10.0	μA
Offset - Tc		±5.0	±15.0	ppmFS/°C
Gain (Relative to R_{SET})[1]		±5	±10	%
Gain Tc		±50	±200	ppm/°C
Gain, variance (each channel, relative to the average of all three)		±2.0	±6.0	%
Linearity				
Integral		±0.1	±0.5	LSB
Differential		±0.1	±0.5	LSB
Linearity TC		±20	±100	ppmFS/°C
Monotonicity		Guaranteed		
DYNAMIC CHARACTERISTICS				
Conversion rate - max. over operating temperature & supply	60			MHz
Settling time (to 0.5 LSB)		12		ns
Set-up time	2			ns
Hold time	2			ns
Output transient glitch energy		50		pV-sec
Output transient glitch amplitude		60		mV
GENERAL INFORMATION				
Internal voltage reference	1.26	1.40	1.54	volts
Color palette		4096		colors
Internal static RAM (32 x 4) (x 3 channels)		32		colors
Max. output current drive capability (for combinations of R_{SET} and R_L)	33			mA
Max. output voltage drive capability (for combinations of R_{SET} and R_L)	1.5			volts
Power supply current		30	60	mA
		(-66dB)	(-60dB)	
Power supply rejection ratio		0.0005	0.001	%/%(V_{DD}-V_{SS})
DIGITAL OUTPUT CHARACTERISTICS				
D_0 to D_3 - When $\overline{OE}$ is enabled.				
Coding		Binary		
Compatibility		TTL or CMOS		
Drive		Two "74S" Schottky loads or 10 HCT equiv. loads		
Logic "0" - 0 to 20mA sink	0	0.1	0.4	Vdc
Logic "1" - 0 to 4mA source	2.7	4.9	5.0	Vdc

	BI-DIR Data Bus $\overline{OE}$	$\overline{OVLY}$	WHT CTRL	ASEL	BLANK ADJ	REF RGB	MPLX ADDR	SYNC ADJ
3405SWM	yes	yes	yes	yes	yes	yes	yes	yes
3405SW	yes	no	no	yes	yes	no	no	yes
3405S	no	no	no	yes	no	no	no	no



Write Mode Timing Diagram



Read Mode Timing Diagram

DEVICE OPERATION

The output of the RGB DAC 3405S is a current source whose full scale value is set by an external resistor. This resistor is connected to an internal reference (1.4V nominal), and the current through the resistor represents 7/16 LSBs of output current. Thus, for a full scale current of 15 LSBs, IO = 1.4R x 16 x 15/7 = 48/R, where IO = full scale output current, R = current settling resistor (ohms). This resistor is connected from Iset to ground.

Example: RL = 37.5Ω, IO = .0166 (VO = 637.5 mV from black to white level.)

$$R = \frac{48}{IO} = \frac{48}{0.0166} = 2890 \text{ (ohm)}$$

The value of R would be 5780Ω nominal if RL were 75Ω.

PIN DESCRIPTION

Read Address (A0 - A4)

This provides address information for the lookup tables during read operations through an edge triggered register. This path to the LUT is enabled by a logic "1" level at the ADDRESS SELECT line. The setup and hold times from valid address to the falling edge of strobe are 2 nanoseconds and 2 nanoseconds minimum, respectively. This input also provides address information for the LUT during write operations. This path to the LUT is enabled by a logic "0" level at the ADDRESS SELECT line. These lines are buffered internally and provide asynchronous access to the LUT.

Address Select (ASEL)

A logic "1" enables the READ ADDRESS path to the LUT. A logic "0" enables the WRITE ADDRESS path to the LUT. This input does not modify the contents of the LUT and is used to select between display mode (READ ADDRESS) and modify mode (WRITE ADDRESS) operations.

DATA (D0 - D3)

This input provides LUT data in nibble form during write operations when used in conjunction with WRITE ADDRESS, WE and CSR, CSG or CSB.

CHIP SELECT ($\overline{CSR}$, $\overline{CSG}$, $\overline{CSB}$)

The active portion of the LUT is selected with these inputs. During write mode operations the desired LUT location may be modified by a logic "0"at the appropriate CS line, enabling the WRITE ADDRESS lines with the correct LUT address with the new value on the DATA lines and activating the WE line.

During display mode, all three CS lines are held at logic "0" to enable all three channel outputs to the DAC internal registers.

WRITE ENABLE ($\overline{WE}$)

A logic "1" selects read or display mode, a logic "0" selects write mode. When used in conjunction with the WRITE ADDRESS, CS and DATA inputs a modification of a location in the LUT may be made.

BLANK ($\overline{BLANK}$)

A logic "0" on this input synchronously sets all three channels to the blank level. This input overrides data from the LUT and is used to blank the screen. This input may be overridden by the OVERLAY and REF combination. This input is latched into an edge triggered register on the falling edge of STROBE.

SYNC ($\overline{SYNC}$)

The sync amplitude (40 IRE units) is synchronously subtracted from the green DAC output when a logic "0" appears at this input. This input is used to generate composite sync and blank signals to the monitor. This input is latched into an edge triggered register on the falling edge of STROBE.

STROBE

This is the main clock input of which the falling edge is used to strobe the data and control inputs into an edge triggered register, as well as move this information in a synchronous pipeline fashion.

ISET (programs gain)

An external resistor connected from this point to Vss programs the DAC full scale outputs in the following manner: Iout = 48/R mA, where R is the external resistor value in kΩ.

BIAS

This is the control amplifier output and should be bypassed to VDD with 0.1μF capacitor. External loading at this point is not recommended.

RED, GRN, BLU OUTPUT
These are the current outputs for the three channels and are normally resistively connected to Vss with either 75 or 37.5 ohms.

VDD
This is the most positive supply pin and is normally connected to +5V.

VSS
This is the most negative supply pin and is normally connected to ground.

BLANK ADJ (RGBDAC3405SW/SWM)
This input may be used to adjust the black level of the three DAC channels and is normally left unconnected. The nominal black value is 7.5 IRE units above the blank level. To adjust this level, connect a 10kΩ potentiometer from VDD to Vss and a 10kΩ resistor from the wiper of the potentiometer to the BLANK ADJ pin.

SYNC ADJ (RGBDAC3405SW/SWM)
In precision applications, this input may be used to adjust the sync amplitude (nominally 40 IREs) on the green DAC channel. It is normally left unconnected. To adjust this level, connect a 10kΩ potentiometer from VDD to Vss and a 10kΩ resistor from the wiper of the potentimeter to the SYNC ADJ pin.

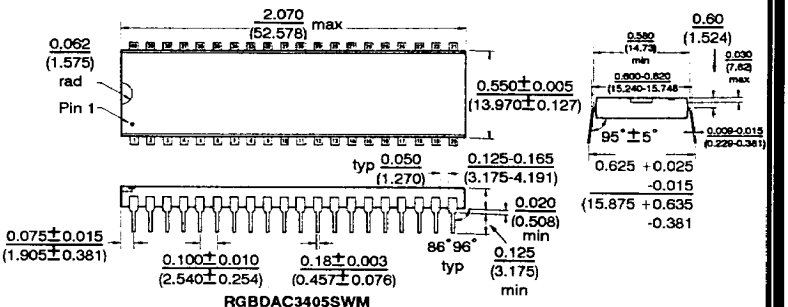
OUTPUT ENABLE ($\overline{OE}$) (RGBDAC3405SW/SWM)
A logic "0" at this input enables output buffers from the selected LUT color channel to the DATA lines during read back operation. If more than one CS line is at logic "0" the output buffers will be disabled to avoid a bus conflict.

WHT CONTROL, REF WHITE FUNCTION (RGBDAC3405SWM)
When enabled by both OVLY and REF being active; a logic "0" at this input sets reference white to the DAC full scale and a logic "1" sets reference white to the DAC full scale value plus 10 IREs.

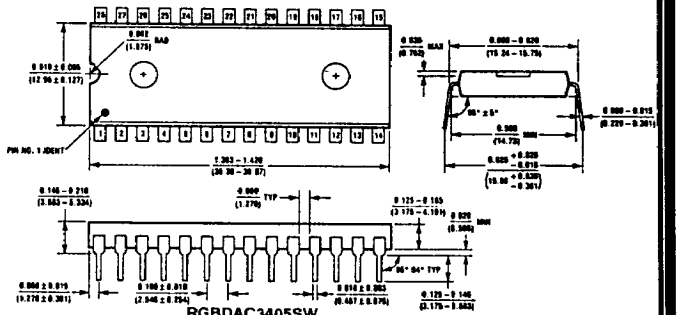
OVERLAY ($\overline{OVLY}$) (RGBDAC3405SWM)
A logic "0" on this line synchronously forces all three DAC outputs to the black level unless the REF line for that channel is active. A logic "1" on this line synchronously disables the REF input for all three channels. This input is latched into an edge triggered register on the falling edge of STROBE.

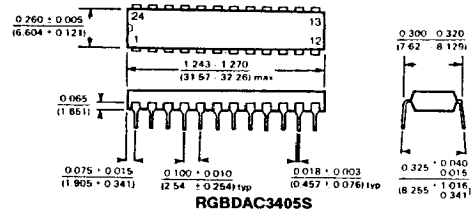
REFERENCE ($\overline{REF}$ RED, $\overline{GRN}$, $\overline{BLU}$) (RGBDAC3405SWM)
These inputs are inactive if the OVERLAY line is held at logic "1." If the OVERLAY line is at logic "0" then a logic "0" at any of these inputs synchronously sets the corresponding channel to the reference white level as defined by the WHT CONTROL input. The OVERLAY and REF inputs combine to synchronously override all LUT and control (blank and sync) inputs to the DAC. These inputs are normally used as a 4-bit data bus to overlay text on the graphics display. These inputs are latched into an edge triggered register on the falling edge of STROBE.

MECHANICAL OUTLINE



RGBDAC3405SWM


RGBDAC3405SW



RGBDAC3405S

PIN DESIGNATIONS

Function	SWM	SW	S	Function	SWM	SW	S
Blank Adj	1	1	-	VDD	21	-	-
Grn Out	2	2	1	Wo	22	17	15
Blu Out	3	3	2	Ao	23	17	15
Red Out	4	4	3	W1	24	18	16
Vss	5	-	-	A1	25	18	16
Strobe	6	5	4	W2	26	19	17
$\overline{OE}$	7	6	-	A2	27	19	17
$\overline{WE}$	8	7	5	W3	28	20	18
$\overline{Ref\ Grn}$	9	-	-	A3	29	20	18
$\overline{Ref\ Blu}$	10	-	-	W4	30	21	19
$\overline{Ref\ Red}$	11	-	-	A4	31	21	19
$\overline{CSG}$	12	8	6	$\overline{OVLY}$	32	-	-
$\overline{CSB}$	13	9	7	Wht Ctl	33	22	-
$\overline{CSR}$	14	10	8	$\overline{Blank}$	34	23	20
Do	15	11	9	$\overline{Sync}$	35	24	21
D1	16	12	10	Vss	36	-	-
D2	17	13	11	ISET (VRef)	37	25	22
D3	18	14	12	Bias	38	26	23
Addr Sel	19	15	13	Sync Adj	39	27	-
Vss	20	16	14	VDD	40	28	24

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