

MN4030B/S, MN4070B/S

Quad Exclusive-OR Gates

■ Description

The MN4030B/S and MN4070B/S are EXCLUSIVE-OR gates and have 4 circuits in a package.

The outputs are fully buffered to improve the propagation characteristics between the input and output which are affected by increasing load capacitance and minimizes propagation delay time. Their primary use is where low power dissipation and/or high noise immunity is desired.

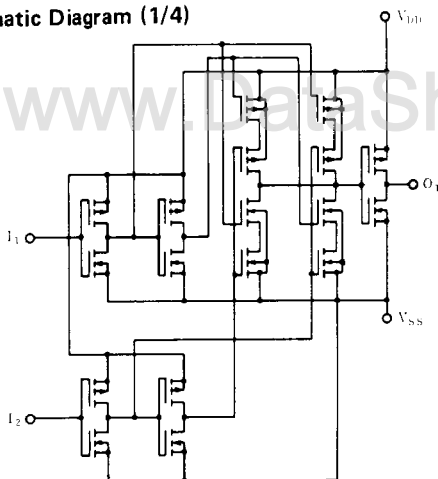
Typical applications include digital comparators and parity checkers.

These are equivalent to MOTOROLA MC14070B and RCA CD4070B.

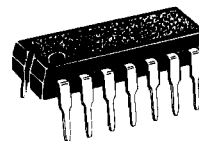
■ Truth Table

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

■ Schematic Diagram (1/4)



P- 1



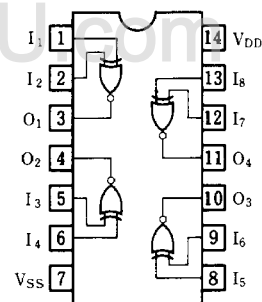
14-Pin • Plastic DIL Package

P- 2



14-Pin • Panafiat Package (SO-14D)

Pin Configuration



■ Maximum Ratings ($T_a=25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	$-0.5 \sim +18$	V
Input Voltage	V_i	$-0.5 \sim V_{DD} + 0.5^*$	V
Output Voltage	V_o	$-0.5 \sim V_{DD} + 0.5^*$	V
Peak Input - Output Current	$\pm I_i$	max. 10	mA
Power Dissipation (per package)	$T_a = -40 \sim +60^\circ\text{C}$	max. 400	mW
	$T_a = +60 \sim +85^\circ\text{C}$	Decrease up to 200mW rating at $8\text{mW}/^\circ\text{C}$	
Power Dissipation (per output terminal)	P_D	max. 100	mW
Operating Ambient Temperature	T_{opr}	$-40 \sim +85$	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-65 \sim +150$	$^\circ\text{C}$

* $V_{DD} + 0.5\text{V}$ should be under 18V

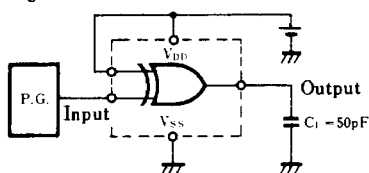
■ DC Characteristics ($V_{SS}=0V$)

Item	V_{DD} (V)	Symbol	Conditions	$T_a = -40^\circ C$		$T_a = 25^\circ C$		$T_a = 85^\circ C$		Unit
				min.	max.	min.	max.	min.	max.	
Quiescent Power Supply Current	5	I_{DD}	$V_i = V_{SS}$ or V_{DD}	—	1	—	1	—	7.5	μA
	10			—	2	—	2	—	15	
	15			—	4	—	4	—	30	
Output Voltage Low Level	5	V_{OL}	$V_i = V_{SS}$ or V_{DD} $ I_o < 1\mu A$	—	0.05	—	0.05	—	0.05	V
	10			—	0.05	—	0.05	—	0.05	
	15			—	0.05	—	0.05	—	0.05	
Output Voltage High Level	5	V_{OH}	$V_i = V_{SS}$ or V_{DD} $ I_o < 1\mu A$	4.95	—	4.95	—	4.95	—	V
	10			9.95	—	9.95	—	9.95	—	
	15			14.95	—	14.95	—	14.95	—	
Input Voltage Low Level	5	V_{iL}	$ I_o < 1\mu A$ $V_o = 0.5V$ or $4.5V$	—	1.5	—	1.5	—	1.5	V
	10			—	3	—	3	—	3	
	15			—	4	—	4	—	4	
Input Voltage High Level	5	V_{iH}	$ I_o < 1\mu A$ $V_o = 0.5V$ or $4.5V$	3.5	—	3.5	—	3.5	—	V
	10			7	—	7	—	7	—	
	15			11	—	11	—	11	—	
Output Current Low Level	5	I_{oL}	$V_o = 0.4V, V_i = 0$ or $5V$ $V_o = 0.5V, V_i = 0$ or $10V$ $V_o = 1.5V, V_i = 0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{oH}$	$V_o = 4.6V, V_i = 0$ or $5V$ $V_o = 9.5V, V_i = 0$ or $10V$ $V_o = 13.5V, V_i = 0$ or $15V$	0.52	—	0.44	—	0.36	—	mA
	10			1.3	—	1.1	—	0.9	—	
	15			3.6	—	3	—	2.4	—	
Output Current High Level	5	$-I_{oH}$	$V_o = 2.5V, V_i = 0$ or $5V$	1.7	—	1.4	—	1.1	—	mA
Input Leakage Current	15	$\pm I_i$	$V_i = 0$ or $15V$	—	0.3	—	0.3	—	1	μA

■ Switching Characteristics ($T_a = 25^\circ C, V_{SS} = 0V, C_L = 50pF$)

Item	V_{DD} (V)	Symbol	min.	typ.	max.	Unit
Output Rise Time	5	t_{TLH}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Output Fall Time	5	t_{THL}	—	60	180	ns
	10		—	30	90	
	15		—	20	60	
Propagation Delay Time	5	t_{PLH}	—	75	225	ns
	10		—	30	90	
	15		—	25	75	
Propagation Delay Time	5	t_{PHL}	—	85	255	ns
	10		—	35	105	
	15		—	30	90	
Input Capacitance		C_i	—	—	7.5	pF

1. Switching Time Test Circuit



2. Waveforms

