# SC531

# Triple Low-side FET Driver with Digitally Controlled Current Limit

**POWER MANAGEMENT**

## Features

- Dual 2A Source, 4A Sink FET Drivers
- Second Channel Enable
- Independent Drive Supplies
- Auxiliary 2A Source, 4A Sink FET Driver
- Precision Reference Output
- Current Limit Reference Output (Analog) Integrated Current Sense Blanking (Digital Input)
- Digitally Controlled High Precision Current Limit
- Current Limit Flag
- Current Input ZVS Comparator
- SPI Communications — 25 MHz
- Thermally Enhanced 4x4 (mm) MLPQ-UT-28 Package
- Lead-free, Halogen free, and RoHS/WEEE compliant

## Applications

- Digitally Controlled Power Supplies
- Flyback Converter
- Boost Converter
- Forward Converter
- DC-DC and AC-DC Converters With Active Clamp
- PFC Converters With ZVT
- Constant Current Converter

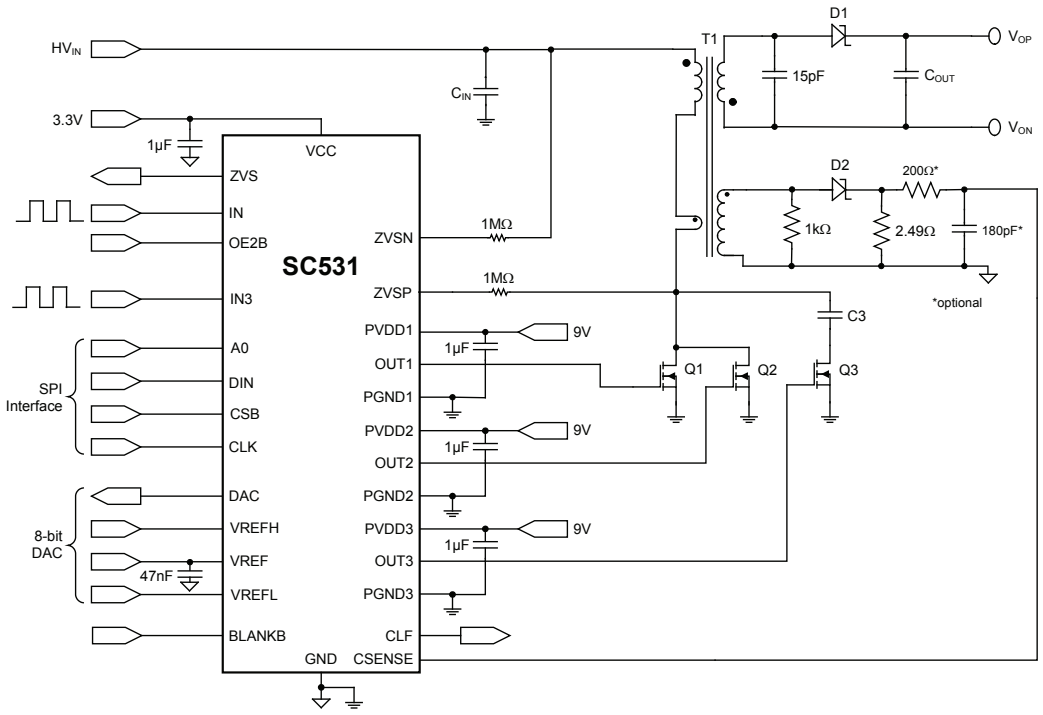
## Description

The SC531 combines three low side drivers with a high speed digitally programmable current limit and a zero voltage switching (ZVS) comparator. Two drivers are normally used to operate the FETs for the power stage. They can operate separately to drive individual power FETs or can be combined to drive a single device. A third, auxiliary, gate drive is controlled by an independent input and can be used to drive the FET for an active clamp or ZVT switching. All three drivers have an independent supply which allows each drive voltage to be optimized for high efficiency.

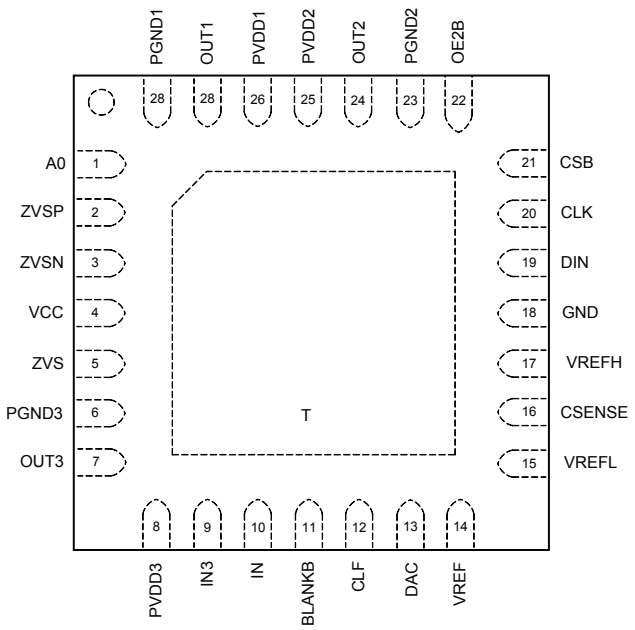
In addition, the SC531 has an SPI interface, 8-bit DAC, and current limit comparator to provide a high-speed digitally programmable current limit. This circuitry can be used for cycle by cycle current limiting or current waveform shaping. A digital output current limit flag is available for monitoring by the host controller.

The SC531 also has a current-input ZVS comparator that can be used to sense changes in high voltage nodes, such as the power FET drain and inductor node (LX) versus the power stage supply, ($HV_{IN}$ in the typical application circuit).

## Typical Application Circuit



## Pin Configuration




**TOP VIEW**

**MLPQ-UT-28; 4x4, 28 LEAD**

**$\theta_{JA}$ = 32.5°C/W**

## Ordering Information

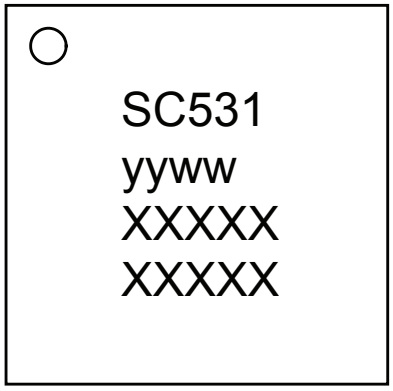
| Device | Package |
|---|---|
| SC531ULTRT[1][2] | MLPQ-UT-28 4×4 |
| SC531EVB | Evaluation Board |

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen free.

## Marking Information




**yyww = Date Code**

**XXXXX = Semtech Lot Number**

**XXXXX = Semtech Lot Number**

## Absolute Maximum Ratings

PVDD1, PVDD2, PVDD3 (V) ..... -0.3 to +15.0
VCC (V) ..... -0.3 to +3.6
VREFH, CSENSE (V) ..... -0.3 to +(VCC + 0.3)
ZVS, ZVSP, ZVSN(V) ..... -0.3 to +(VCC + 0.3)
DIN, CS, CLK, A0 (V) ..... -0.3 to +(VCC + 0.3)
VREF, IN3, CLF, OE2B (V) ..... -0.3 to +(VCC + 0.3)
BLANKB, IN, DAC, CSB (V) ..... -0.3 to +(VCC + 0.3)
OUT1, OUT2, OUT3 (V) ..... -1 to +PVDD
ESD Protection Level[1] (kV) ..... 2 kV
PGND1, PGND2, PGND3, VREFL to GND (V) ... -0.3 to +0.3

NOTES: Voltages are all referenced to GND (Pin 18).

## Recommended Operating Conditions

Ambient Temperature Range (°C) ..... $-40 \leq T_A \leq +115$
PVDD1, PVDD2, PVDD3 (V) ..... $6 \leq PV_{DD} \leq 12$
$V_{CC}$ (V) ..... $3.15 \leq V_{cc} \leq 3.46$
Maximum input Current for ZVSP, ZVSN (µA) ..... ≤40

NOTES: PGND1, PGND2, PGND3 must be tied to GND.

## Thermal Information

Thermal Resistance, Junction to Ambient[2] (°C/W) ... 32.5
Maximum Junction Temperature (°C) ..... +125
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (10s to 30s) (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

## Electrical Characteristics

Unless otherwise noted, $T_A$ = +25°C for Typ, -40°C to +115°C for Min and Max, $T_{J(MAX)}$ = 125°C, $PV_{DD}$ = 6V to 12V, $V_{cc}$ = 3.15V to 3.46V, bypass capacitor on $PV_{DD}$, $V_{CC}$ = 2.2µF, $V_{REF}$ = $V_{REFH}$ = 0.1µF

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Supply Section** | | | | | | |
| Combined PVDD Quiescent Current | $I_{PVDDL}$ | Not switching, CSB=1, IN = IN3 = OE2B = low | | 1.5 | 2.5 | mA |
| Combined PVDD Quiescent Current | $I_{PVDDH}$ | Not switching, CSB=1, IN = IN3 = VCC, OE2B = low | | 2.2 | 3.5 | mA |
| $V_{CC}$ Quiescent Current | $I_{VCC}$ | Not switching, CSB=1 | | 0.8 | 1.4 | mA |
| PVDD UVLO Enable Voltage | $PV_{ENABLE}$ | PVDD rising: UVLO sensing on PVDD1 only | 4.25 | 4.5 | 4.75 | V |
| PVDD UVLO Hysteresis | $PV_{HYS}$ | UVLO sensing on PVDD1 only | | 250 | | mV |
| $V_{CC}$ UVLO Threshold | $VCC_{UVLO(TH)}$ | $V_{CC}$ rising | 2.65 | 2.8 | 2.95 | V |
| $V_{CC}$ UVLO Hysteresis | $VCC_{UVLO(HYS)}$ | $V_{CC}$ falling | | 100 | | mV |
| **Digital Section** | | | | | | |
| Digital Input High | $V_{IH}$ | IN, DIN, CSB, CLK, A0, IN3, OE2B | 2.1 | | | V |
| Digital Input Low | $V_{IL}$ | IN, DIN, CSB, CLK, A0, IN3, OE2B | | | 0.8 | V |
| Digital Input High (BLANKB) | $V_{IH\_BLNK}$ | | 2.1 | | | V |
| Digital Input Low (BLANKB) | $V_{IL\_BLNK}$ | | | | 0.4 | V |

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## Electrical Characteristics (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital Section (continued)** | | | | | | |
| Digital Output High | $V_{OH}$ | CLF, ZVS, ILOAD=7mA | 2.64 | | | V |
| Digital Output Low | $V_{OL}$ | CLF, ZVS, ILOAD=-7mA | | | 0.66 | V |
| BLANKB pull-up resistance | $R_{BLANKB}$ | internal pull-up to $V_{CC}$ | 2.1 | 3.3 | 4.5 | kΩ |
| SPI CLK Frequency | $f_{CLK}$ | | | 25 | | MHz |
| SPI CLK High & Low Time | $t_{SPI}$ | | 15 | | | ns |
| CSB, DIN to Clock Falling Edge Setup and Hold Time | $t_{SH}$ | | | | 5 | ns |
| Chip Select Reset Time | $t_{CSB}$ | | 10 | | | ns |
| **DAC Section** | | | | | | |
| DAC Response Time | $t_{RESPONSE}$ | Settling to within 1LSB | | 0.5 | | µs |
| DAC INL | INL | | -1 | | 1 | LSB |
| DAC DNL | DNL | | -0.2 | | 0.2 | LSB |
| Voltage Reference | $V_{REF}$ | VREF/VREFH, HiZ voltmeter | 0.245 | | 0.255 | V/V |
| Voltage Reference Buffer Offset | $V_{BOFFSET}$ | | -5 | | 5 | mV |
| Voltage Ref Divider Resistance | $R_{REF}$ | | 384 | 640 | 896 | kΩ |
| **Current Sense Comparator Section** | | | | | | |
| Current Sense Voltage Range | $V_{SENSE}$ | | 0 | | 1.2 | V |
| Comparator Offset Voltage | $V_{COFFSET}$ | | -6 | | 6 | mV |
| CSENSE to CLF Propagation Delay | $t_{CLF}$ | | | 25 | 40 | ns |
| CSENSE to Driver Output Propagation Delay | $t_{DRIV}$ | 1nF load, 60mV overdrive, 10% to 90% of drive output | | 45 | 70 | ns |
| **Driver Section** | | | | | | |
| Driver OUT1, OUT2, OUT3 Resistance (Sourcing) | $R_{DSP1,2,3}$ | | | 1.5 | 3 | Ω |
| Driver OUT1, OUT2, OUT3 Resistance (Sinking) | $R_{DSN1,2,3}$ | | | 0.7 | 1.5 | Ω |
| Rise Time — OUT1, OUT2, OUT3 | $t_{RISE1,2,3}$ | PVDD=8V, load capacitance=1nF | | 10 | | ns |
| Fall Time — OUT1, OUT2, OUT3 | $t_{FALL1,2,3}$ | PVDD=8V, load capacitance=1nF | | 5 | | ns |
| Propagation Delay from IN to OUT1, OUT2 | $t_{PROP1,2}$ | PVDD=8V, load capacitance=1nF | | 25 | 45 | ns |

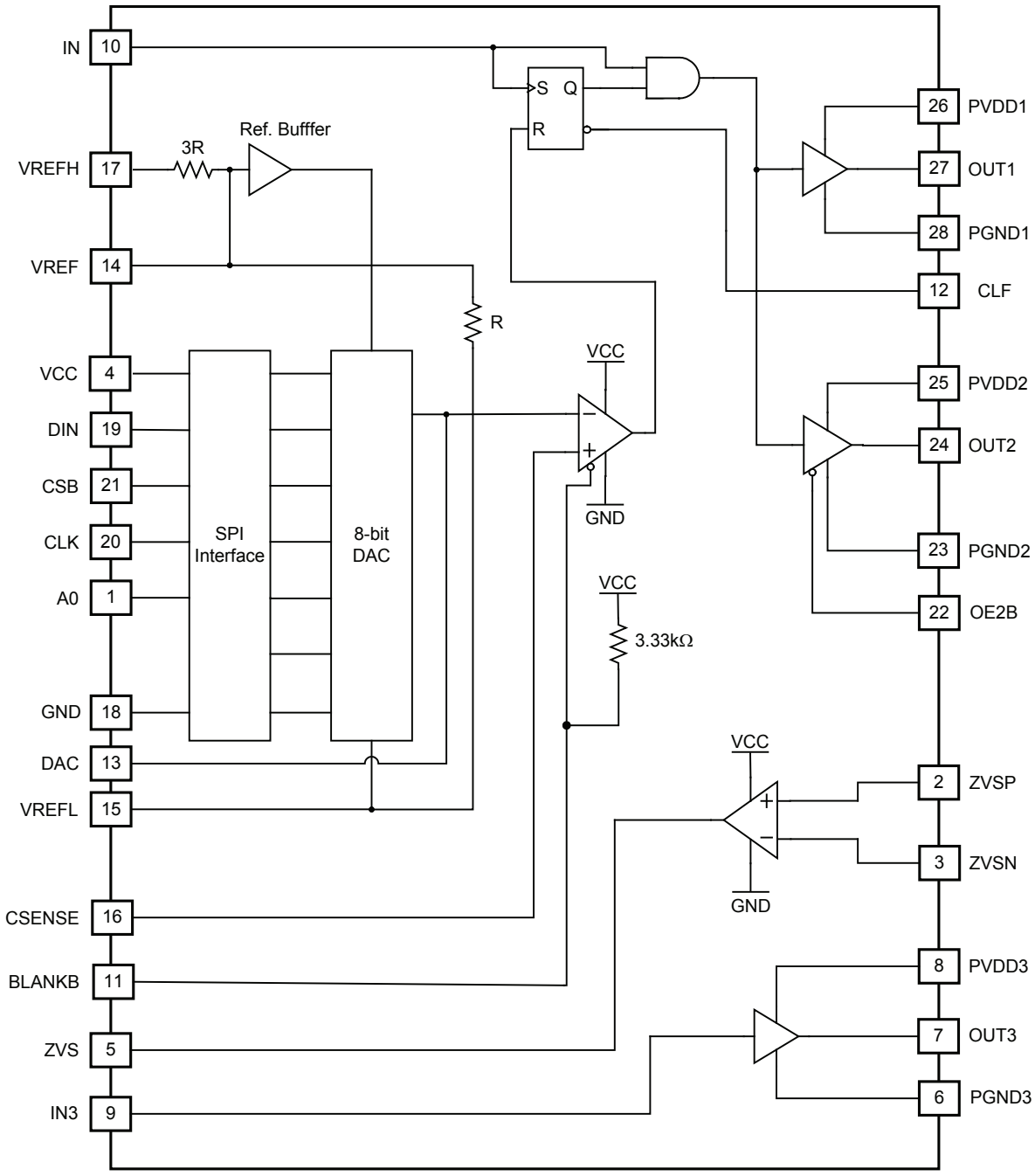
## Electrical Characteristics (continued)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Driver Section (continued)** | | | | | | |
| Propagation Delay from IN3 to OUT3 | $t_{PROP3}$ | No load | | 25 | 45 | ns |
| $OUT_X$ Minimum On-time | | $PVDD_X$ = 8V, COUT = 1nF | 25 | | 100 | ns |
| Driver 1,2,3 Switching Frequency | $f_{1,2,3}$ | | | | 800 | kHz |
| **ZVS Section** | | | | | | |
| ZVSP, ZVSN Offset Current | $I_{ZVS}$ | 10µA < Input current < 40µA | -3 | 0 | 3 | µA |
| ZVSP, ZVSN to GND Voltage | $V_{ZVS}$ | 0µA < Input current < 40µA | | | 5 | V |
| Response Time (ZVS falling) | $t_{ZVS\_falling}$ | 10µA<Input Current< 40µA, 5µA overdrive | | 25 | 40 | ns |
| Response Time (ZVS rising) | $t_{ZVS\_rising}$ | 10µA<Input Current< 40µA, 10µA overdrive | | | 0.5 | µs |

## Pin Descriptions

| Pin # | Pin Name | Signal Type | Pin Function |
|---|---|---|---|
| 1 | A0 | Digital input | Address for SPI interface |
| 2 | ZVSP | Analog input | ZVS comparator positive input |
| 3 | ZVSN | Analog input | ZVS comparator negative input |
| 4 | VCC | Power input | Input supply voltage. Connect a 2.2uF bypass capacitor from VCC to GND. |
| 5 | ZVS | Digital output | ZVS comparator output |
| 6 | PGND3 | GROUND | Driver 3 power ground. |
| 7 | OUT3 | Power output | Driver 3 output |
| 8 | PVDD3 | Power input | Driver 3 supply voltage. Connect a 2.2uF bypass capacitor from PVDD3 to PGND3. |
| 9 | IN3 | Digital input | Driver 3 signal input |
| 10 | IN | Digital input | Driver 1 and 2 signal input |
| 11 | BLANKB | Digital input | Current limit blanking input |
| 12 | CLF | Digital output | Current limit flag |
| 13 | DAC | Analog output | DAC output |
| 14 | VREF | Analog input/output | Reference Voltage |
| 15 | VREFL | Analog input | Low reference for VREF resistor divider and DAC. Typically connected to GND. |
| 16 | CSENSE | Analog input | Current sense input |
| 17 | VREFH | Analog input | High reference for top of VREF resistor divider |
| 18 | GND | GROUND | IC Ground |
| 19 | DIN | Digital input | SPI data input |
| 20 | CLK | Digital input | SPI clock input |
| 21 | CSB | Digital input | SPI chip select input |
| 22 | OE2B | Digital input | Driver 2 enable |
| 23 | PGND2 | GROUND | Driver 2 power ground |
| 24 | OUT2 | Power output | Driver 2 output |
| 25 | PVDD2 | Power input | Driver 2 supply voltage. Connect a 2.2uF bypass capacitor from PVDD2 to PGND2. |
| 26 | PVDD1 | Power input | Driver 1 supply voltage. Connect a 2.2uF bypass capacitor from PVDD1 to PGND2. |
| 27 | OUT1 | Power output | Driver 1 output |
| 28 | PGND1 | GROUND | Driver 1 power ground |
| T | Thermal Pad | GROUND | Connected to GND, use multiple thermal vias for heatsinking purposes |

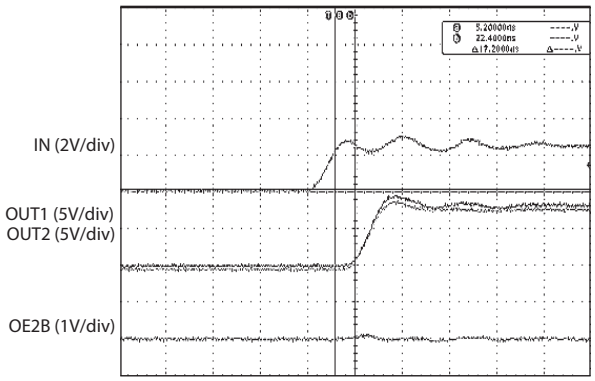
## Block Diagram



## Typical Characteristics

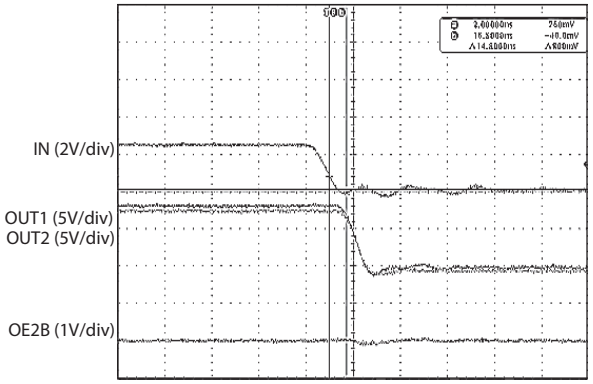
### OUT1, OUT2 Rise Time

VCC = 3.3V, PVDD1/2/3 = 7.8V, Load = BSC190N15NS3G



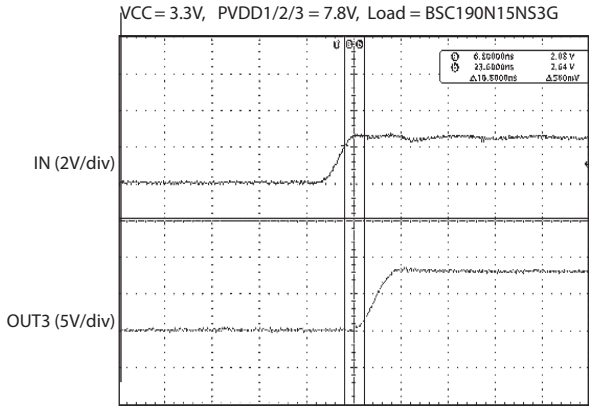

### OUT1, OUT2 Fall Time

VCC = 3.3V, PVDD1/2/3 = 7.8V, Load = BSC190N15NS3G



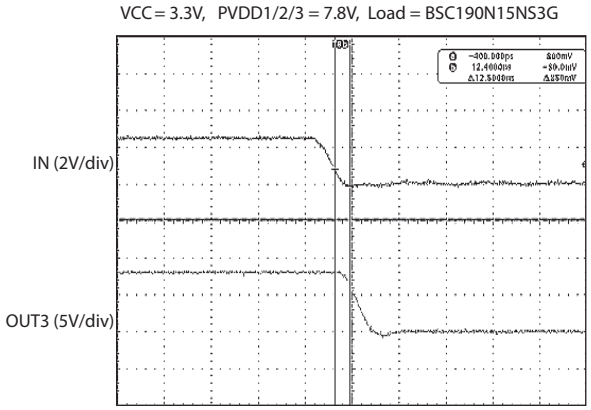

### OUT3 Rise Time

VCC = 3.3V, PVDD1/2/3 = 7.8V, Load = BSC190N15NS3G



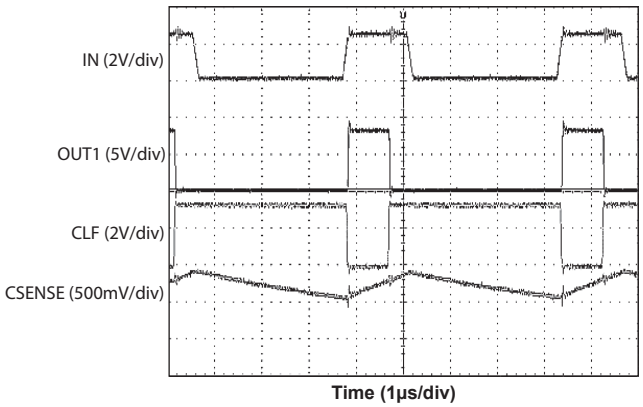

### OUT3 Fall Time

VCC = 3.3V, PVDD1/2/3 = 7.8V, Load = BSC190N15NS3G



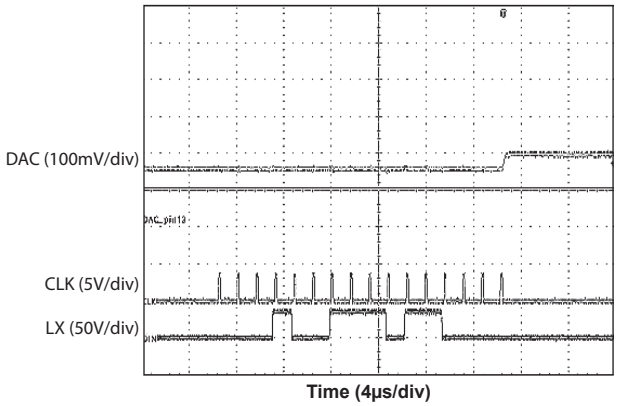

### OUT1 Current Limit With CLF Flag

VCC = 3.3V, PVDD1/2/3 = 7.8V, Emulated CSENSE input




### SPI to DAC Response Time

VCC = 3.3V, PVDD1/2/3 = 7.8V



## Applications Information

### Gate Drivers 1 and 2

The high-current output stage in the SC531 is capable of providing 2A source, 4A sink peak current and voltage swings from PVDD to PGND for both OUT1 and OUT2. These outputs can drive individual power FETs which can be used in parallel or can be combined to drive one larger device. The second output (OUT2) can be disabled to save power by setting OE2B input to a logic high. If OE2B is set high during normal switching operation, the OUT2 output is not disabled until the next falling edge of IN.

The driver outputs follow the state of the IN pin. When IN is high OUT1 and OUT2 (if OE2B is low) are high. The outputs will be pulled low when IN goes low or when the current limit is reached.

### Reference Divider, Buffer, DAC, and Current Limit Comparator

The SC531 contains a reference divider, buffer, DAC, and current limit comparator that combine to provide a high-speed and high-accuracy programmable current limit. The reference voltage is generated by a resistive divide by four from VREFH to VREFL. This voltage is referenced at the VREF pin. Alternatively, an external reference can drive the VREF pin if a different value is desired. The equation for the VREF voltage is shown below.

$$VREF = \frac{VREFH + 3 \cdot VREFL}{4}$$

The VREFL input must be within +/-300mV of the GND pin and is typically connected to analog ground.

The VREF voltage is buffered and then used as the reference for the 8-bit DAC. The 8-bit DAC is controlled by the SPI (see next section for protocol information). The output of the DAC connects to the DAC pin and to the negative input of the current limit comparator.

The positive input of the current limit comparator is connected to the CSENSE pin through blanking circuitry. When the BLANKB pin is held low the CSENSE pin is disconnected from the comparator and the positive input is shorted to ground. The BLANKB pin has an internal pull-up resistance of 3.3 kΩ to $V_{CC}$. If the BLANKB pin is not held low, then the output of the current limit comparator will be determined by the CSENSE and DAC voltages. If the DAC voltage is greater than CSENSE then the output of the comparator will be low. If the CSENSE voltage is greater than the DAC voltage then the output of the comparator will go high causing the CLF flag to go high and OUT1 and OUT2 to be driven low. This event is latched and will not be released until CSENSE goes below DAC and the IN pin goes from low to high.

### SPI Interface

A write sequence begins by bringing CSB low. Once CSB is low, the data on the DIN line is clocked into the 16-bit shift register on the falling edges of CLK. On the 16th falling clock edge, the last data bit is clocked in and the DAC is updated. CSB can be held low or high at this point and any data or clock pulses following the 16th falling clock edge are ignored. CSB must be brought high for the minimum specified time before the next write sequence is initiated with the falling edge of CSB. Figure 3 shows the Serial Timing Diagram and Figure 4 shows the Input Register Contents.

### ZVS Comparator

The ZVS comparator is a current-input (Norton) comparator that provides information that the ZVS condition has been reached by comparing the LX node to $HV_{IN}$. The falling edge of the power FET LX node going below $HV_{IN}$ (ZVS output going low) is the faster edge. The structure of the comparator allows fast detection with a large voltage range. Series resistors are placed from LX to ZVSP and $HV_{IN}$ to ZVSN. The resistor value should be chosen based on the voltage levels that are being compared and should be optimized to produce input currents in the 10-40µA range. The ZVSP and ZVSN pins can vary from 2-4V based on this normal input current range.

The ZVSN and ZSVP input pins can tolerate currents up to 300µA, but the accuracy and speed specifications are only valid in the 10-40µA range.

## Applications Information (continued)

### Gate Driver 3

Gate Driver 3 is a third auxiliary gate drive that is controlled by the IN3 pin, an independent input. It has a separate power supply (PVDD3) and ground (PGND3) connection. The output OUT3 is 2A source, 4A sink capable. This output can be used as a general purpose driver which can be used to drive the FET for an active clamp or active snubber. Other uses include driving the FET for soft-switching ZVT or to drive a secondary PWM output.

### Applications

The SC531 is suited for applications which contain a micro-controller or DSP to control PWM switching. The auxiliary OUT3 output and the DAC controlled current limit can be used to implement a variety of switching topologies.

By driving the IN3 input with a signal that is inverted from the IN1 input, the OUT3 driver can be used to drive an external P-channel FET for an active clamp converter. In addition, the DAC can be programmed to vary in real-time as a function of the main error voltage from the system microcontroller. This causes each OUT1/2 pulse to terminate when the peak current reaches the real-time DAC setting, resulting in current-mode operation. Combining the DAC control with the external P-channel FET circuitry results in an Active Clamp Current Mode Converter. Refer to Figure 1.

The above converter can also be used to provide a programmable constant current output by setting the DAC to a constant value. The IN input has a longer duty cycle than is required to maintain the output, but each OUT1/2 pulse is terminated early by the current limit function. The average current to the load will equal the peak inductor current reduced by 50% of the inductor ripple current.

The OUT3 output can be used to drive the FET for a ZVT switch such as is used in PFC boost converters. The ZVS comparator can be used to detect when the ZVT FET has completed its discharge of the main FET by connecting two additional resistors to the ZVS inputs, $R_{Z1}$ and $R_{Z2}$, and resistors RZ3 and RZ4 should be selected to keep the keep the ZVSP/N input current below 300uA at maximum VIN. Refer to Figure 2.

### PCB Layout Guidelines

Any switch-mode converter requires a good PCB layout to achieve best performance. The following guidelines should be followed to produce an optimum PCB layout.

All bypass capacitors should be located close to the pins which they connect to. Use short, direct copper traces to connect between the capacitor and the IC pins. Bypass capacitors should be placed on the same side of the PCB as the IC. Use a 2.2µF minimum capacitor for all bypassing. The pins which require bypass capacitors are shown below:

- VCC, GND
- PVDD1, PGND1
- PVDD2, PGND2
- PVDD3, PGND3

The connections between the PGND pins and the power FETs should be short and direct, using a ground plane if available. If vias are required use multiple vias to reduce impedance between the IC and the FETs. The gate traces should be short and direct. Use wide, short gate traces to reduce susceptibility to noise generated by nearby FET switching. The gate trace routings should avoid any of the FET drain nodes.

The CSENSE signal should be referenced to GND (analog ground). A capacitor on the CSENSE input should be located near the CSENSE pin and connected to GND, and connected to the IC with short direct traces.

Any VREFH, VREFL, or VREF bypass capacitors should be placed close to the pins, routed with direct traces, and connected to GND.

## Applications Information (continued)

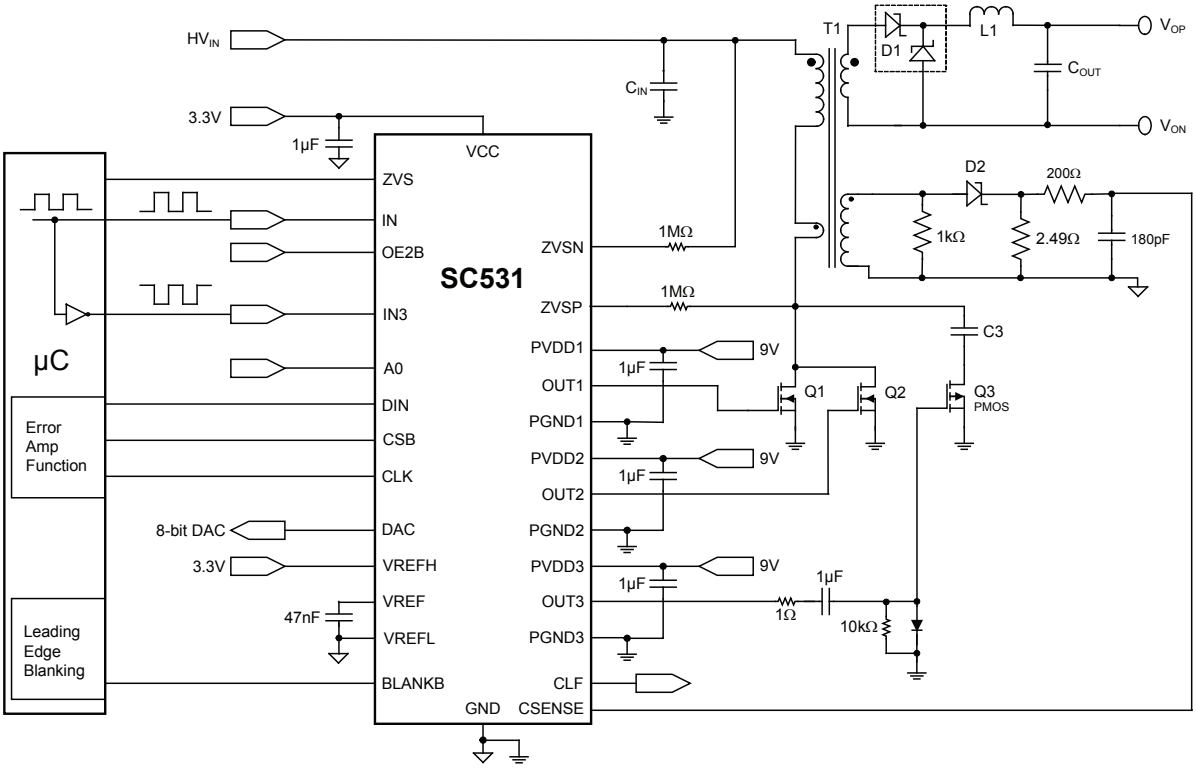



**Figure 1 — Current-Mode Forward Converter With Active Clamp**

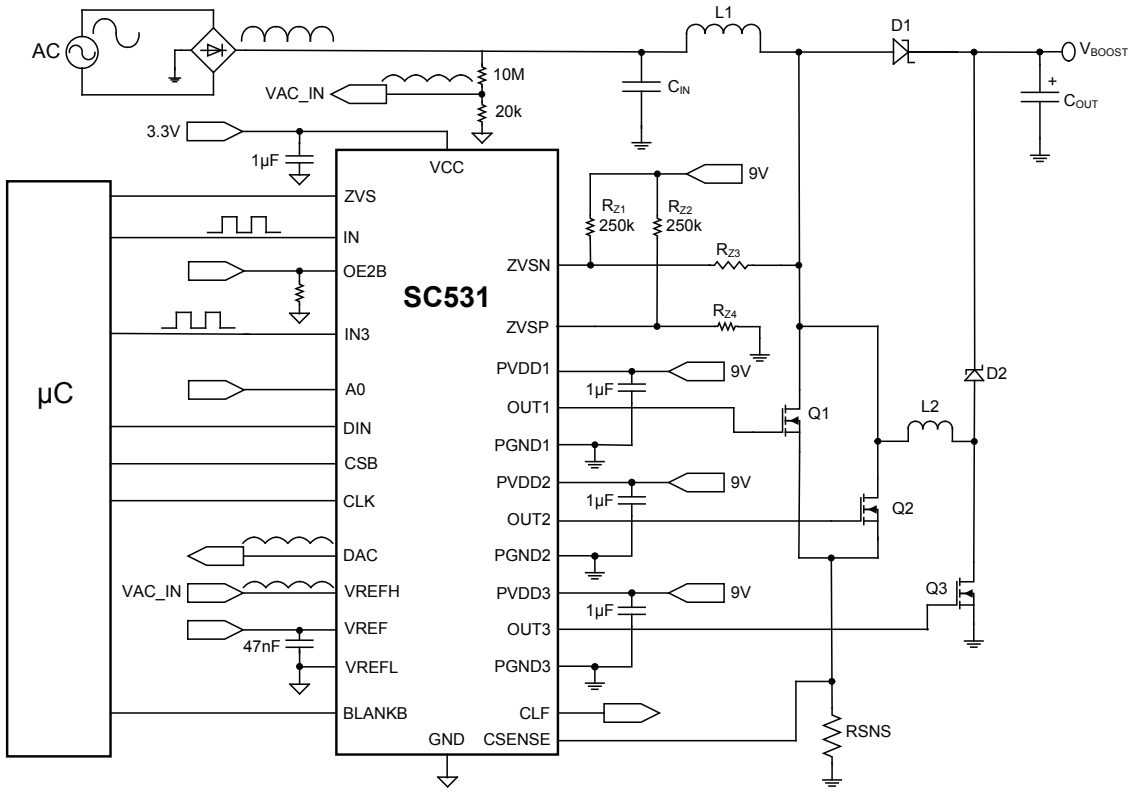



**Figure 2 — ZVT Switching PFC Boost Converter**

## Applications Information (continued)

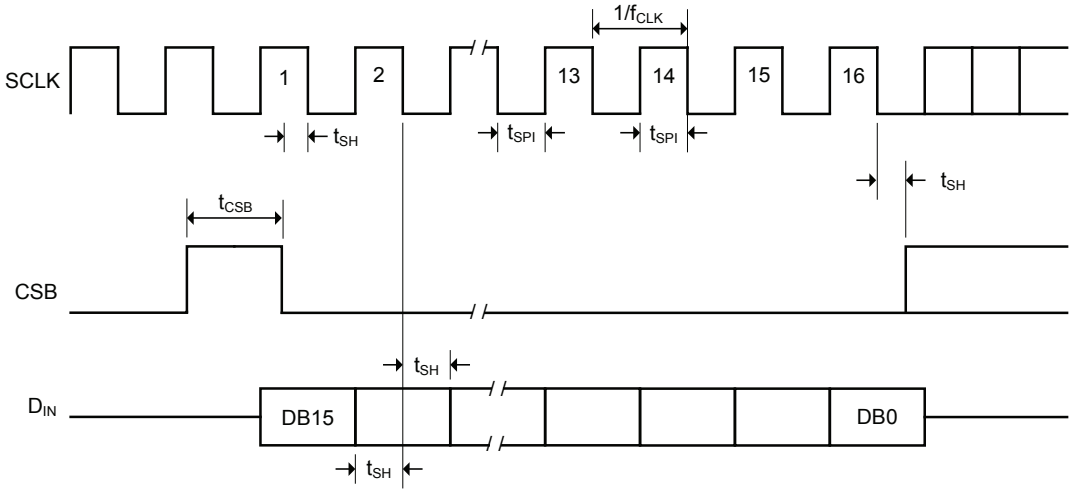



**Figure 3 — Serial Timing Diagram**

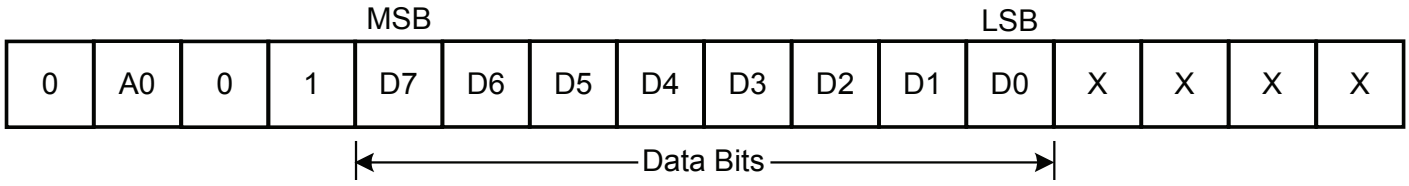
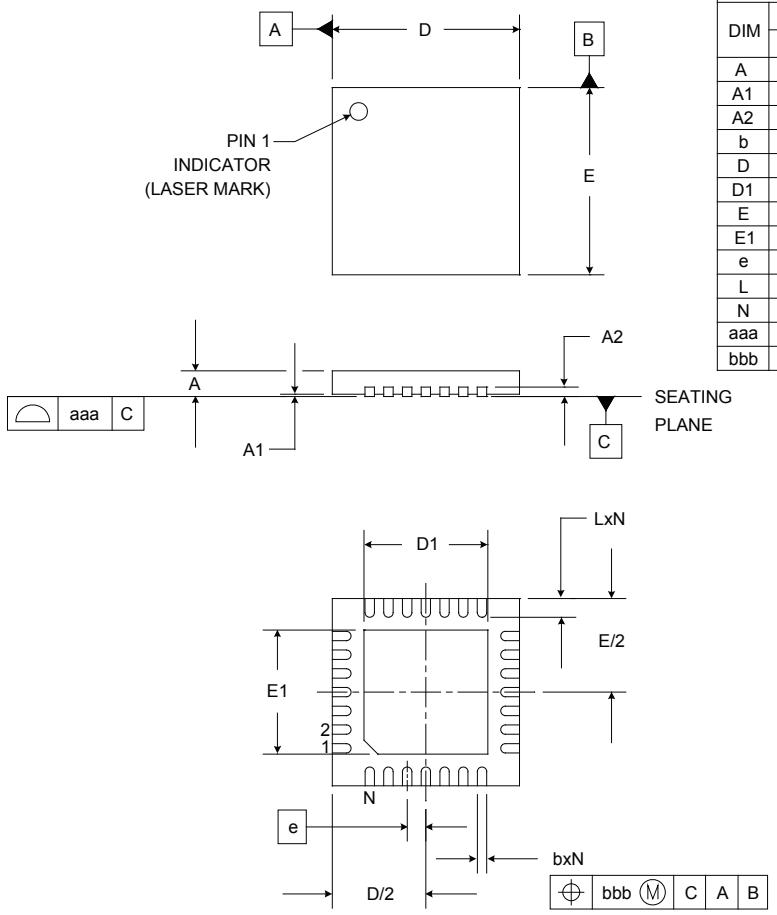



**Figure 4 — Input Register Contents**

## Outline Drawing – 4x4 MLPQ-UT28

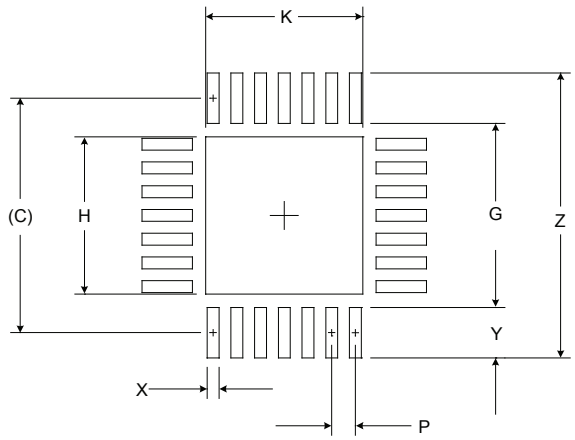



| DIMENSIONS | | | | | | |
|---|---|---|---|---|---|---|
| DIM | INCHES | | | MILLIMETERS | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | .020 | - | .024 | 0.50 | - | 0.60 |
| A1 | .000 | - | .001 | 0.00 | - | 0.02 |
| A2 | | (.006) | | | (0.152) | |
| b | .006 | .008 | .010 | 0.15 | 0.20 | 0.25 |
| D | .154 | .157 | .161 | 3.90 | 4.00 | 4.10 |
| D1 | .100 | .104 | .108 | 2.55 | 2.65 | 2.75 |
| E | .154 | .157 | .161 | 3.90 | 4.00 | 4.10 |
| E1 | .100 | .104 | .108 | 2.55 | 2.65 | 2.75 |
| e | | .016 BSC | | | 0.40 BSC | |
| L | .012 | .016 | .020 | 0.30 | 0.40 | 0.50 |
| N | | 28 | | | 28 | |
| aaa | | .003 | | | 0.08 | |
| bbb | | .004 | | | 0.10 | |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. CENTER PAD IS CONNECTED TO PIN 18(GROUND).

## Land Pattern – 4x4 MLPQ-UT28




| DIMENSIONS | | |
|---|---|---|
| DIM | INCHES | MILLIMETERS |
| C | (.156) | (3.95) |
| G | .122 | 3.10 |
| H | .104 | 2.65 |
| K | .104 | 2.65 |
| P | .016 | 0.40 |
| X | .008 | 0.20 |
| Y | .033 | 0.85 |
| Z | .189 | 4.80 |

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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