

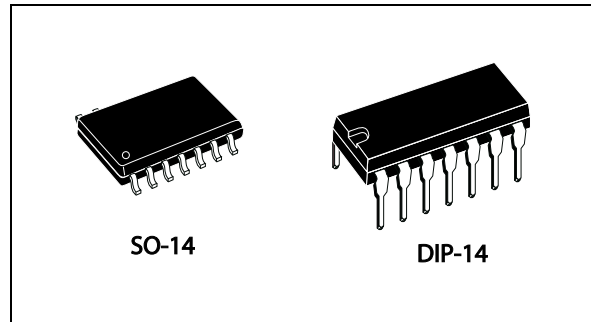
High-voltage high and low side driver

Features

- High voltage rail up to 600 V
- dV/dt immunity ± 50 V/nsec in full temperature range
- Driver current capability:
 - 290 mA source,
 - 430 mA sink
- Switching times 75/35 nsec rise/fall with 1 nF load
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Integrated bootstrap diode
- Comparator for fault protections
- Smart shut-down function
- Adjustable dead-time
- Interlocking function
- Compact and simplified layout
- Bill of material reduction
- Effective fault protection
- Flexible, easy and fast design

Applications

- Motor driver for home appliances, factory automation, industrial drives and fans.
- HID ballasts, power supply units.



Description

The L6391 is a high-voltage device manufactured with the BCD “OFF-LINE” technology. It is a single chip half-bridge gate driver for N-channel power MOSFET or IGBT.

The high side (floating) section is designed to stand a voltage rail up to 600 V. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing microcontroller/DSP.

An integrated comparator is available for protections against overcurrent, overtemperature, etc.

Table 1. Device summary

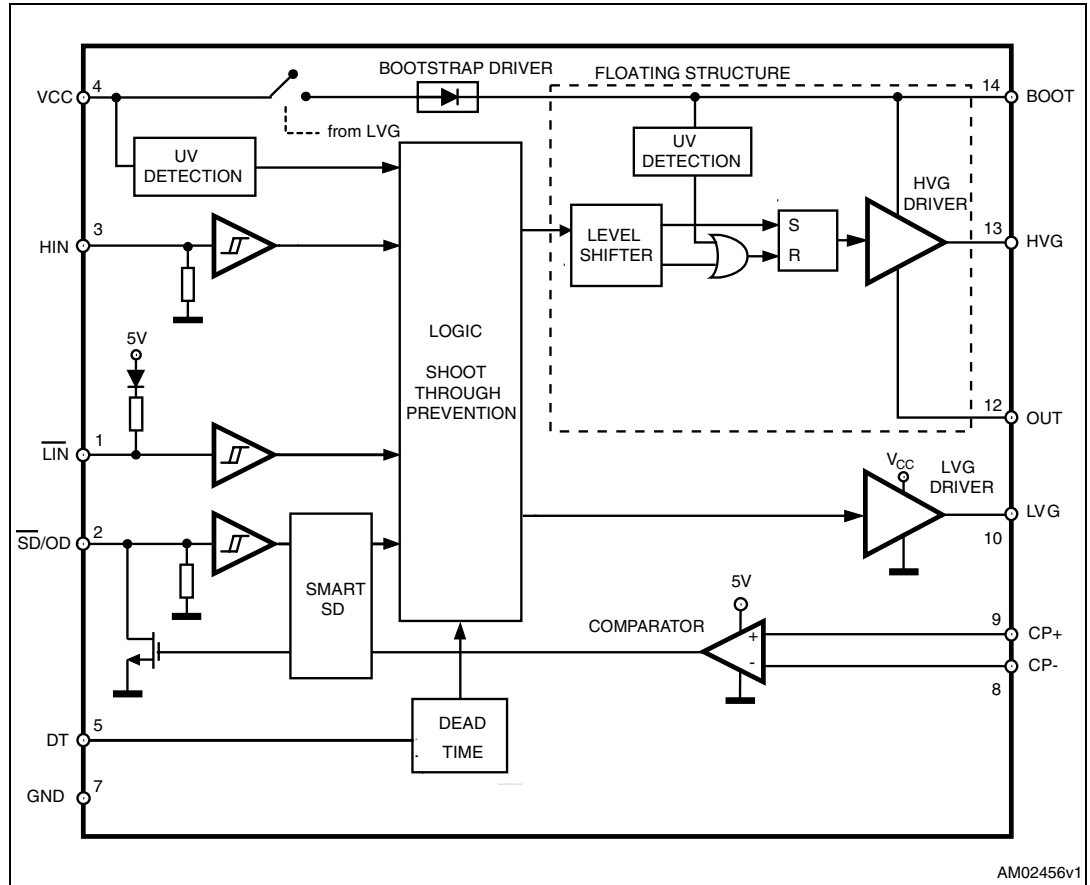
| Order codes | Package | Packaging |
|-------------|---------|---------------|
| L6391N | DIP-14 | Tube |
| L6391D | SO-14 | Tube |
| L6391DTR | SO-14 | Tape and reel |

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1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Pin connection (top view)

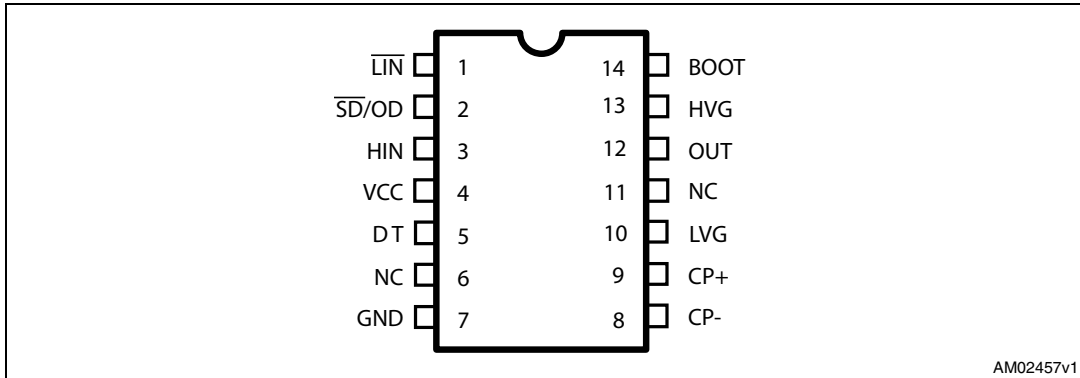


Table 2. Pin description

| Pin n # | Pin name | Type | Function |
|---------|----------------------|------|-----------------------------------------------------------------|
| 1 | LIN | I | Low side driver logic input (active low) |
| 2 | SD/OD ⁽¹⁾ | I/O | Shut down logic input (active low)/open drain comparator output |
| 3 | HIN | I | High side driver logic input (active high) |
| 4 | VCC | P | Lower section supply voltage |
| 5 | DT | I | Dead time setting |
| 6 | NC | | Not connected |
| 7 | GND | P | Ground |
| 8 | CP- | I | Comparator negative input |
| 9 | CP+ | I | Comparator positive input |
| 10 | LVG ⁽¹⁾ | O | Low side driver output |
| 11 | NC | | Not connected |
| 12 | OUT | P | High side (floating) common voltage |
| 13 | HVG ⁽¹⁾ | O | High side driver output |
| 14 | BOOT | P | Bootstrapped supply voltage |

1. The circuit guarantees less than 1 V on the LVG and HVG pins (@ Isink = 10 mA), with V_{CC} > 3 V. This allows omitting the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

3 Truth table

Table 3. Truth table

| Input | | | Output | |
|-----------------|------------------|-----|--------|-----|
| \overline{SD} | \overline{LIN} | HIN | LVG | HVG |
| L | X | X | L | L |
| H | H | L | L | L |
| H | L | H | L | L |
| H | L | L | H | L |
| H | H | H | L | H |

Note: X: don't care

4 Electrical data

4.1 Absolute maximum ratings

Table 4. Absolute maximum rating

| Symbol | Parameter | Value | | Unit |
|---------------|--------------------------------------|-----------------|------------------|------|
| | | Min | Max | |
| V_{cc} | Supply voltage | -0.3 | 21 | V |
| V_{out} | Output voltage | $V_{boot} - 21$ | $V_{boot} + 0.3$ | V |
| V_{boot} | Bootstrap voltage | -0.3 | 620 | V |
| V_{hvg} | High side gate output voltage | $V_{out} - 0.3$ | $V_{boot} + 0.3$ | V |
| V_{lvg} | Low side gate output voltage | -0.3 | $V_{cc} + 0.3$ | V |
| V_{cp-} | Comparator negative input voltage | -0.3 | $V_{cc} + 0.3$ | V |
| V_{cp+} | Comparator positive input voltage | -0.3 | $V_{cc} + 0.3$ | V |
| V_i | Logic input voltage | -0.3 | 15 | V |
| V_{OD} | Open drain voltage | -0.3 | 15 | V |
| dV_{out}/dt | Allowed output slew rate | | 50 | V/ns |
| P_{tot} | Total power dissipation (TA = 25 °C) | | 800 | mW |
| T_J | Junction temperature | | 150 | °C |
| T_{stg} | Storage temperature | -50 | 150 | °C |

Note: ESD immunity for pins 12, 13 and 14 is guaranteed up to 1 kV (human body model)

4.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | SO-14 | DIP-14 | Unit |
|--------------|----------------------------------------|-------|--------|------|
| $R_{th(JA)}$ | Thermal resistance junction to ambient | 165 | 100 | °C/W |

4.3 Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Pin | Parameter | Test condition | Min | Max | Unit |
|----------------|-------|-----------------------------------|----------------------------|--------------------|----------------|------|
| V_{CC} | 4 | Supply voltage | | 12.5 | 20 | V |
| $V_{BO}^{(1)}$ | 14-12 | Floating supply voltage | | 12.4 | 20 | V |
| V_{out} | 12 | DC output voltage | | - 9 ⁽²⁾ | 580 | V |
| V_{CP-} | 8 | Comparator negative input voltage | $V_{CP+} \leq 2.5$ V | | $V_{CC}^{(3)}$ | V |
| V_{CP+} | 9 | Comparator positive input voltage | $V_{CP-} \leq 2.5$ V | | $V_{CC}^{(3)}$ | V |
| f_{sw} | | Switching frequency | HVG, LVG load $C_L = 1$ nF | | 800 | kHz |
| T_J | | Junction temperature | | -40 | 125 | °C |

1. $V_{BO} = V_{boot} - V_{out}$

2. LVG off. $V_{CC} = 12.5$ V
Logic is operational if $V_{boot} > 5$ V

3. At least one of the comparator's input must be lower than 2.5 V to guarantee proper operation.

5 Electrical characteristics

5.1 AC operation

Table 7. AC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ °C}$)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|-----------|-------------|--------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| t_{on} | 1 vs 10 | High/low side driver turn-on propagation delay | $V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$ $C_L = 1\text{ nF}$ $V_i = 0\text{ to }3.3\text{ V}$ See Figure 3 . | 50 | 125 | 200 | ns |
| t_{off} | 3 vs 13 | High/low side driver turn-off propagation delay | | 50 | 125 | 200 | ns |
| t_{sd} | 2 vs 10, 13 | Shutdown to high/low side driver propagation delay | | 50 | 125 | 200 | ns |
| t_{isd} | | Comparator triggering to high/low side driver turn-off propagation delay | Measured applying a voltage step from 0 V to 3.3 V to pin CP+; CP-=0.5 V | | 200 | 250 | ns |
| MT | | Delay matching, HS and LS turn-on/off | | | 30 | ns | |
| DT | 5 | Dead time setting range ⁽¹⁾ | $R_{DT} = 0\Omega, C_L = 1\text{ nF}$ | 0.1 | 0.18 | 0.25 | μs |
| | | | $R_{DT} = 37\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | 0.48 | 0.6 | 0.72 | μs |
| | | | $R_{DT} = 136\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | 1.35 | 1.6 | 1.85 | μs |
| | | | $R_{DT} = 260\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | 2.6 | 3.0 | 3.4 | μs |
| MDT | | Matching dead time ⁽²⁾ | $R_{DT} = 0\Omega, C_L = 1\text{ nF}$ | | | 80 | ns |
| | | | $R_{DT} = 37\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | | | 120 | ns |
| | | | $R_{DT} = 136\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | | | 250 | ns |
| | | | $R_{DT} = 260\text{k}\Omega, C_L = 1\text{ nF}, C_{DT} = 100\text{ nF}$ | | | 400 | ns |
| t_r | 10,13 | Rise time | $C_L = 1\text{ nF}$ | | 75 | 120 | ns |
| t_f | | Fall time | $C_L = 1\text{ nF}$ | | 35 | 70 | ns |

1. See [Figure 4 on page 9](#)

2. $MDT = |DT_{LH} - DT_{HL}|$ see [Figure 5 on page 12](#)

Figure 3. Timing

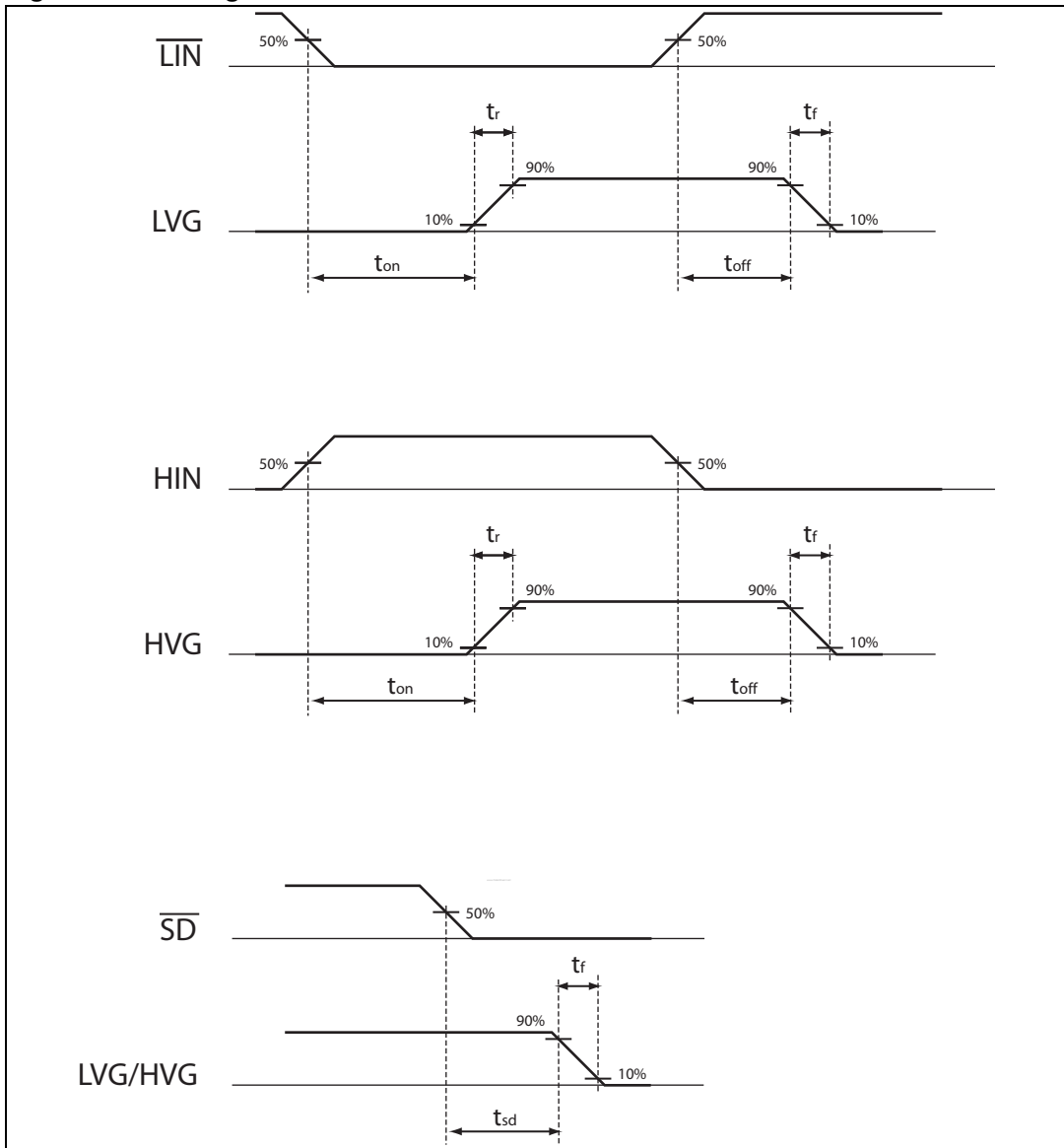
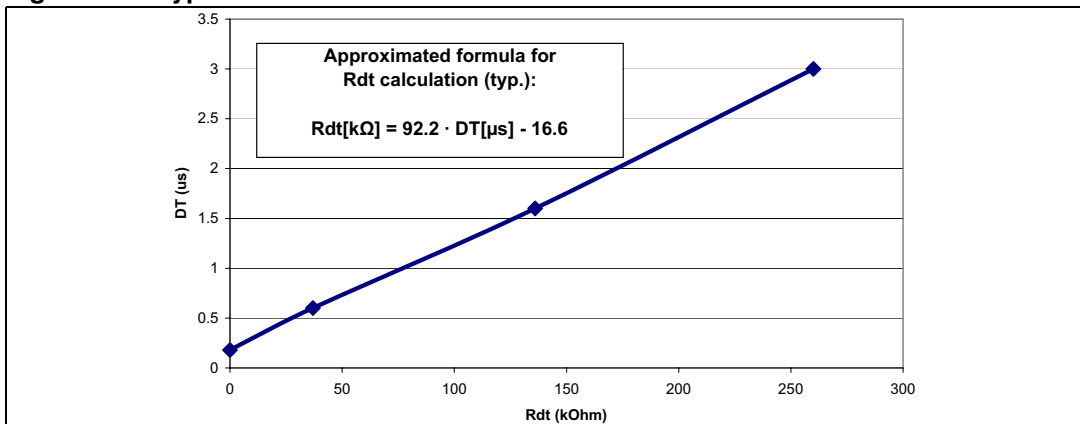


Figure 4. Typical dead time vs. DT resistor value



5.2 DC operation

Table 8. DC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^\circ\text{C}$)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|-----------------------------------------------------------|-----------|-----------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| V_{CC_hys} | 4 | V_{CC} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{CC_thON} | | V_{CC} UV turn ON threshold | | 11.5 | 12 | 12.5 | V |
| V_{CC_thOFF} | | V_{CC} UV turn OFF threshold | | 10 | 10.5 | 11 | V |
| I_{qccu} | 4 | Undervoltage quiescent supply current | $V_{CC} = 9.5\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = GND$; $R_{DT} = 0\ \Omega$; $CP+=GND$; $CP-=5\text{ V}$ | | 100 | 150 | μA |
| I_{qcc} | | Quiescent current | $V_{CC} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = GND$; $R_{DT} = 0\ \Omega$; $CP+=GND$; $CP-=5\text{ V}$ | | 500 | 1000 | μA |
| Bootstrapped supply voltage section ⁽¹⁾ | | | | | | | |
| V_{BO_hys} | 14-12 | V_{BO} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{BO_thON} | | V_{BO} UV turn ON threshold | | 10.6 | 11.5 | 12.4 | V |
| V_{BO_thOFF} | | V_{BO} UV turn OFF threshold | | 9.1 | 10 | 10.9 | V |
| I_{QBOU} | 14-12 | Undervoltage V_{BO} quiescent current | $V_{BO} = 9\text{ V}$ $\overline{SD} = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $R_{DT} = 0\ \Omega$; $CP+=GND$; $CP-=5\text{ V}$ | | 70 | 110 | μA |
| I_{QBO} | | V_{BO} quiescent current | $V_{BO} = 15\text{ V}$ $\overline{SD} = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $R_{DT} = 0\ \Omega$; $CP+=GND$; $CP-=5\text{ V}$ | | 200 | | μA |
| I_{LK} | | High voltage leakage current | $V_{hvg} = V_{out} = V_{boot} = 600\text{ V}$ | | | 10 | μA |
| $R_{DS(on)}$ | | Bootstrap driver on resistance ⁽²⁾ | LVG ON | | 120 | | Ω |
| Driving buffers section | | | | | | | |
| I_{so} | 10, 13 | High/low side source short circuit current | $V_{IN} = V_{ih} (t_p < 10\ \mu\text{s})$ | 200 | 290 | | mA |
| I_{si} | | High/low side sink short circuit current | $V_{IN} = V_{il} (t_p < 10\ \mu\text{s})$ | 250 | 430 | | mA |

Table 8. DC operation electrical characteristics ($V_{CC} = 15\text{ V}$; $T_J = +25\text{ }^\circ\text{C}$) (continued)

| Symbol | Pin | Parameter | Test condition | Min | Typ | Max | Unit |
|---------------------|---------|-----------------------------------------------|----------------------------------------------------------|------|-----|-----|---------------|
| Logic inputs | | | | | | | |
| V_{il} | 1, 2, 3 | Low logic level voltage | | | | 0.8 | V |
| V_{ih} | | High logic level voltage | | 2.25 | | | V |
| V_{il_S} | 1, 3 | Single input voltage | \overline{LIN} and HIN connected together and floating | | | 0.8 | V |
| I_{HINH} | 3 | HIN logic "1" input bias current | HIN = 15 V | 110 | 175 | 260 | μA |
| I_{HINI} | | HIN logic "0" input bias current | HIN = 0 V | | | 1 | μA |
| I_{LINI} | 1 | \overline{LIN} logic "0" input bias current | $\overline{LIN} = 0\text{ V}$ | 3 | 6 | 20 | μA |
| I_{LINh} | | \overline{LIN} logic "1" input bias current | $\overline{LIN} = 15\text{ V}$ | | | 1 | μA |
| I_{SDh} | 2 | \overline{SD} logic "1" input bias current | $\overline{SD} = 15\text{ V}$ | 10 | 40 | 100 | μA |
| I_{SDI} | | \overline{SD} logic "0" input bias current | $\overline{SD} = 0\text{ V}$ | | | 1 | μA |

1. $V_{BO} = V_{boot} - V_{out}$

2. R_{DSON} is tested in the following way:

$$R_{DSON} = [(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})] / [I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})]$$

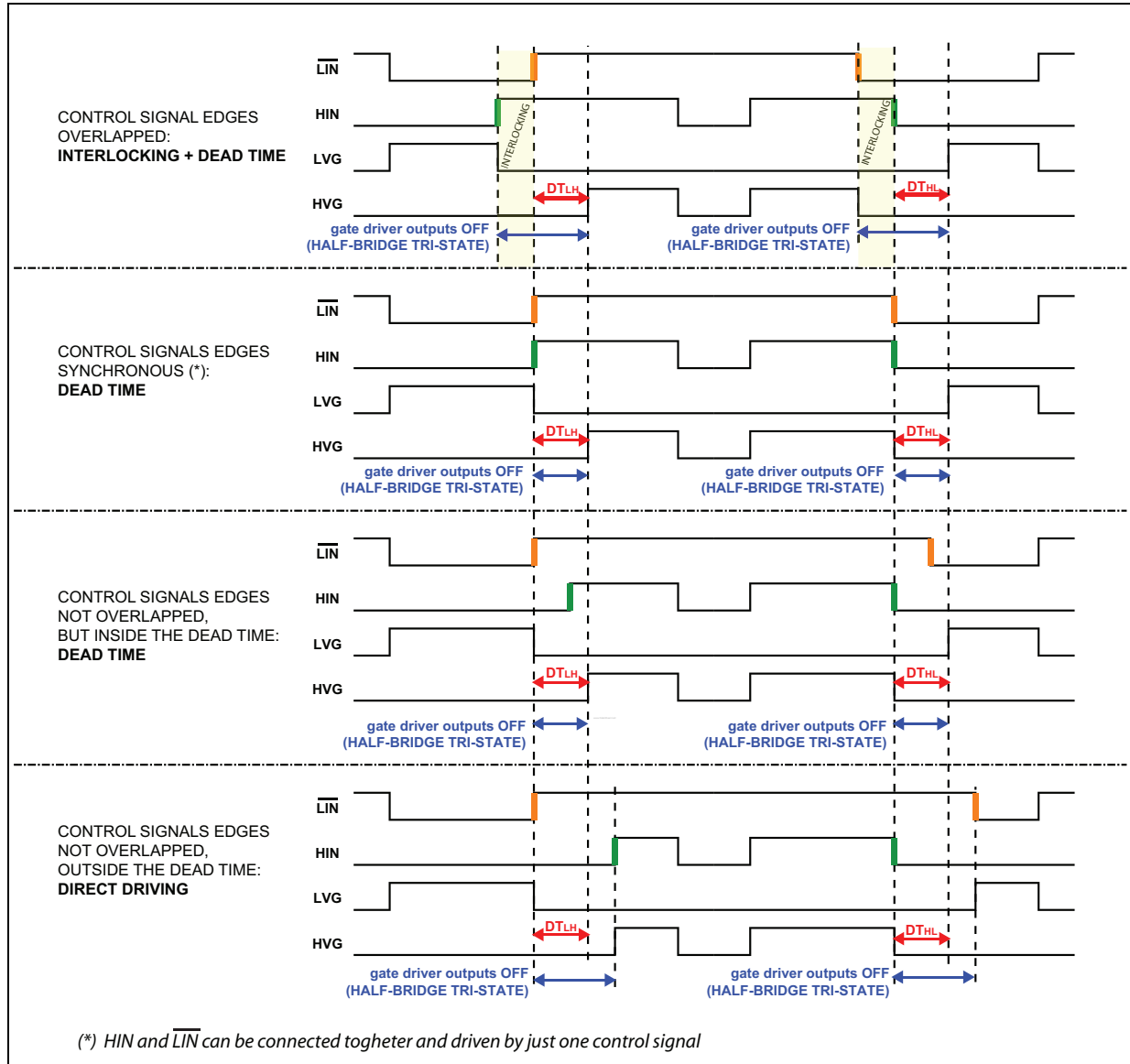
where I_1 is pin 14 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$.

Table 9. Sense comparator ($V_{CC} = 15\text{ V}$, $T_J = +25\text{ }^\circ\text{C}$)

| Symbol | Pin | Parameter | Test conditions | Min | Typ | Max | Unit |
|---------------|------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------------------|
| V_{io} | 8, 9 | Input offset voltage | | -15 | | 15 | mV |
| I_{ib} | 8, 9 | Input bias current | $V_{CP+} = 1\text{ V}$, $V_{CP-} = 0.5\text{ V}$ | | | 1 | μA |
| V_{ol} | 2 | Open drain low level output voltage | $I_{od} = -3\text{ mA}$ $V_{CP+}=1\text{V}$; $V_{CP-}=0.5\text{V}$; | | | 0.5 | V |
| t_{d_comp} | | Comparator delay | $R_{pull}=100\text{ k}\Omega$ to 5 V on \overline{SD}/OD pin; $V_{CP-}=0.5\text{V}$; voltage step on $CP+ = 0 \div 3.3\text{V}$, | | 90 | 130 | ns |
| SR | 2 | Slew rate | $C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$ | | 60 | | V/ μs |

6 Waveforms definitions

Figure 5. Dead time and interlocking waveforms definitions

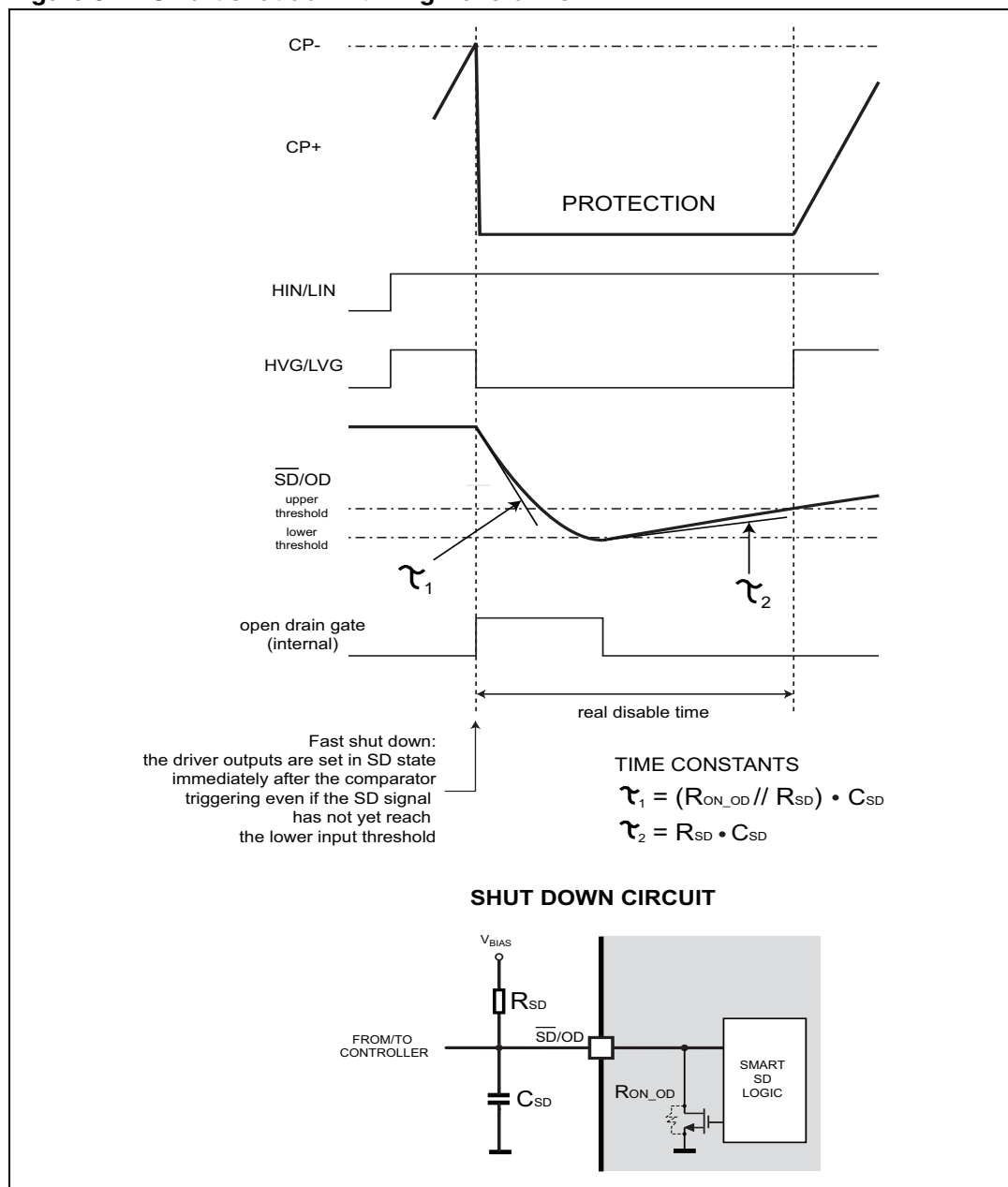


7 Smart shut down function

L6391 integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple over-current detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on pin 2, shared with the \overline{SD} input. When the comparator triggers, the device is set in shut down state and both its outputs are set to low level leaving the half-bridge in tri-state.

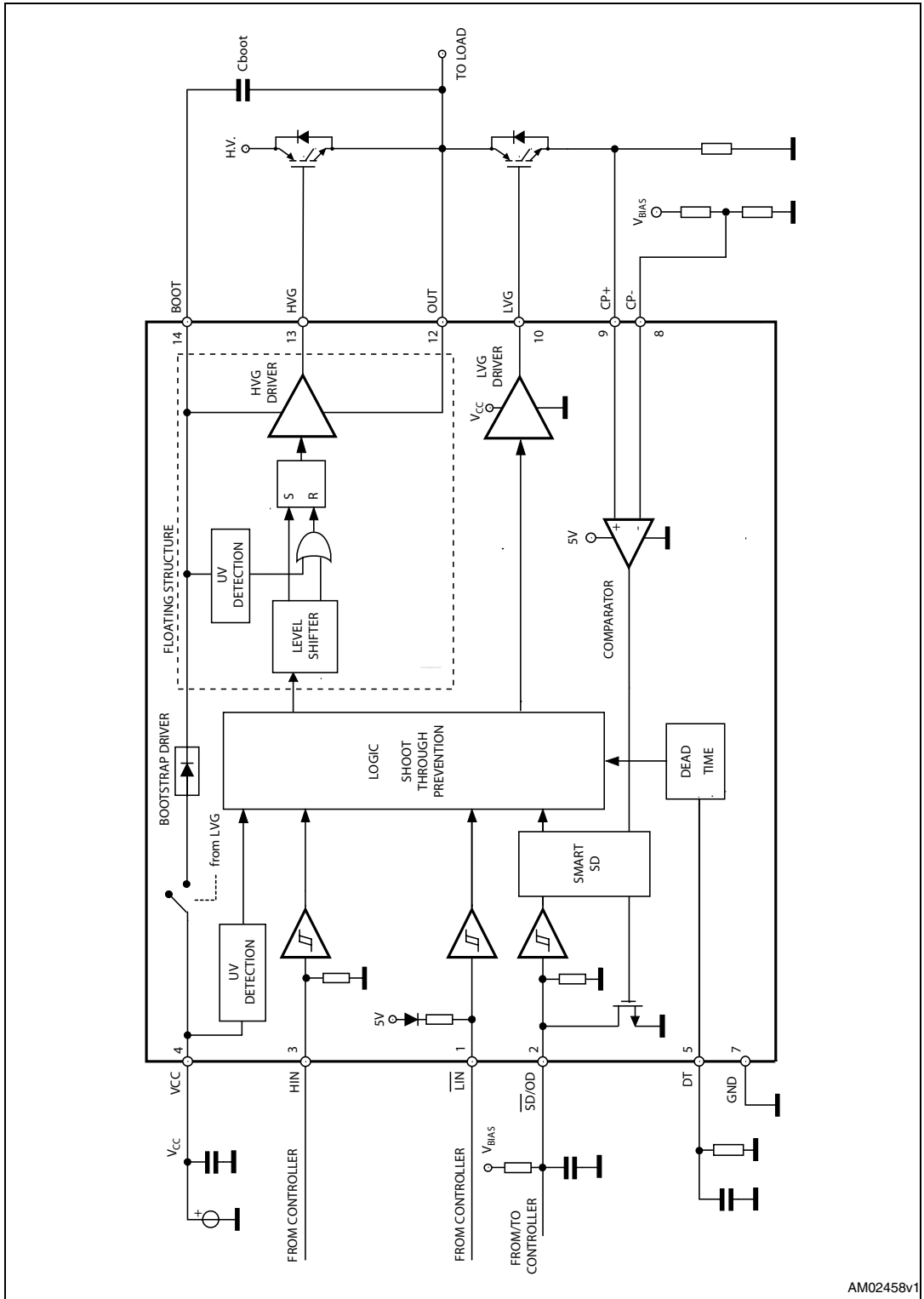
Figure 6. Smart shut down timing waveforms



In common over-current protection architectures the comparator output is usually connected to the \overline{SD} input and an RC network is connected to this \overline{SD}/OD line in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Differently from the common fault detection systems, L6391 Smart shut down architecture allows to immediately turn-off the outputs gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual outputs switch-off. In fact the time delay between the fault and the outputs turn off is no more dependent on the RC value of the external network connected to the pin. In the smart shut down circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time the internal logic turns on the open drain output and holds it on until the \overline{SD} voltage goes below the \overline{SD} logic input lower threshold. The Smart shut down system provides the possibility to increase the time constant of the external RC network (that is the disable time after the fault event) up to very large values without increasing the delay time of the protection. Any external signal provided to the \overline{SD} pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the \overline{SD} input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice versa.

8 Typical application diagram

Figure 7. Application diagram



AM02458v1

9 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 8*). In the L6391 a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with diode in series, as shown in *Figure 9*. An internal charge pump (*Figure 9*) provides the DMOS driving voltage.

9.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} \gg \gg C_{EXT}$$

e.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

e.g.: HVG steady state consumption is lower than 200 μA, so if HVG T_{ON} is 5 ms, C_{BOOT} has to supply 1 μC to C_{EXT}. This charge on a 1 μF capacitor means a voltage drop of 1V.

The internal bootstrap driver gives a great advantage: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R_{DSon} (typical value: 120 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{\text{drop}} = I_{\text{charge}} R_{\text{dson}} \rightarrow V_{\text{drop}} = \frac{Q_{\text{gate}}}{T_{\text{charge}}} R_{\text{dson}}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS and T_{charge} is the charging time of the bootstrap capacitor.

For example: using a power MOS with a total gate charge of 30nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 μs . In fact:

Equation 4

$$V_{\text{drop}} = \frac{30\text{nC}}{5\mu\text{s}} \cdot 120\Omega \sim 0.7\text{V}$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 8. Bootstrap driver with high voltage fast recovery diode

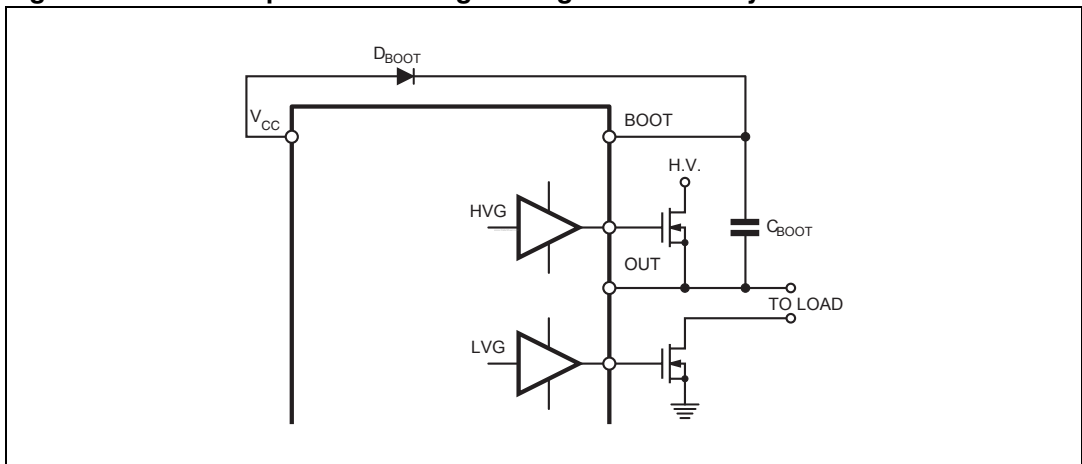
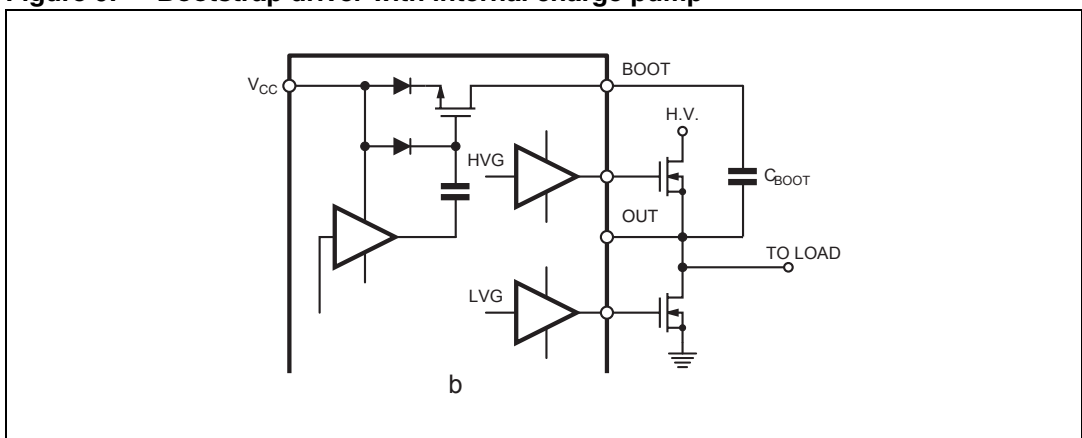


Figure 9. Bootstrap driver with internal charge pump



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Table 10. DIP-14 mechanical data

| Dim. | mm. | | | inch | | |
|------|------|-------|------|-------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| a1 | 0.51 | | | 0.020 | | |
| B | 1.39 | | 1.65 | 0.055 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 15.24 | | | 0.600 | |
| F | | | 7.1 | | | 0.280 |
| l | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | 1.27 | | 2.54 | 0.050 | | 0.100 |

Figure 10. Package dimensions

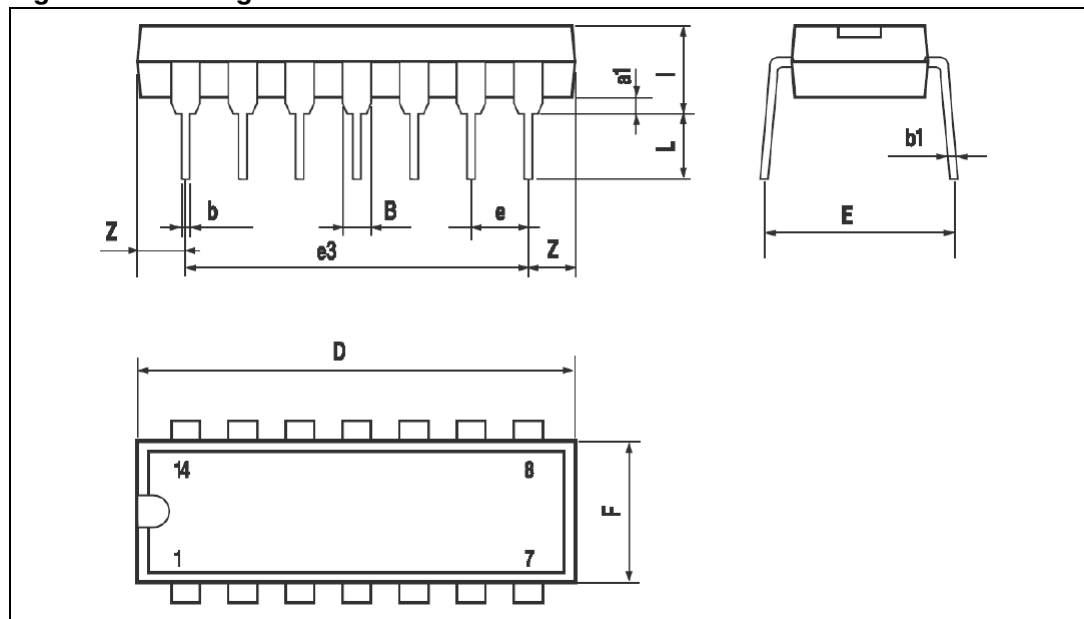
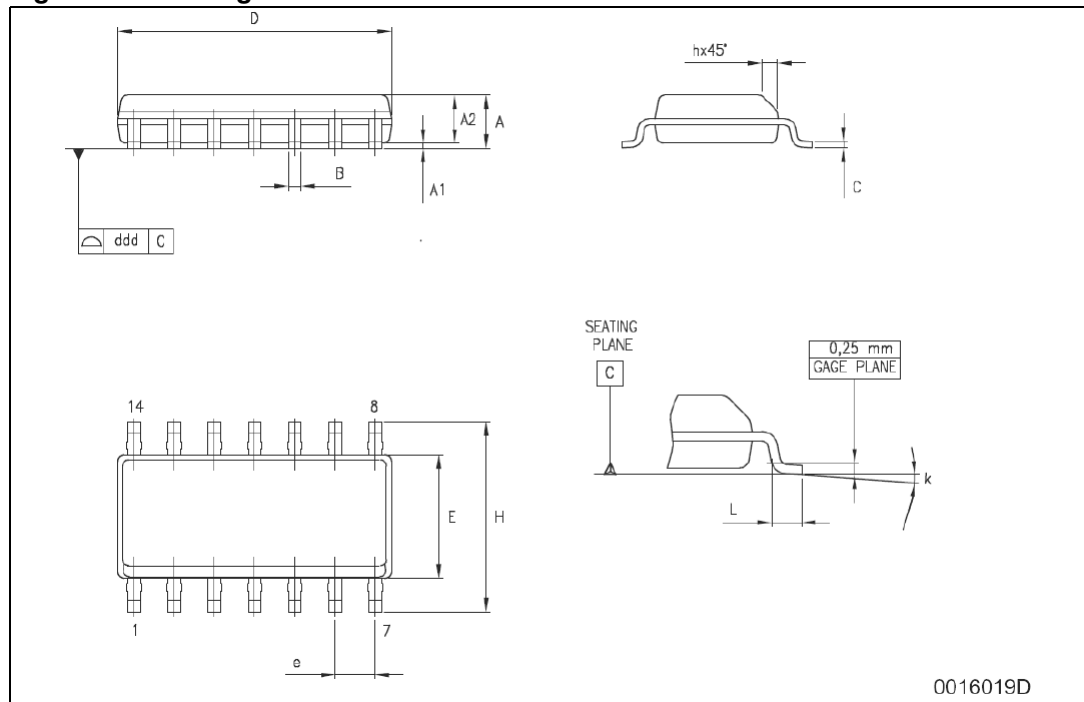


Table 11. SO-14 mechanical data

| Dim. | mm. | | | inch | | |
|------|------------|------|------|-------|-------|-------|
| | Min | Typ | Max | Min | Typ | Max |
| A | | | 1.75 | | | 0.068 |
| a1 | 0.1 | | 0.2 | 0.003 | | 0.007 |
| a2 | | | 1.65 | | | 0.064 |
| b | 0.35 | | 0.46 | 0.013 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.019 | |
| c1 | 45° (typ.) | | | | | |
| D | 8.55 | | 8.75 | 0.336 | | 0.344 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 7.62 | | | 0.300 | |
| F | 3.8 | | 4.0 | 0.149 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.208 |
| L | 0.5 | | 1.27 | 0.019 | | 0.050 |
| M | | | 0.68 | | | 0.026 |
| S | 8° (max.) | | | | | |

Figure 11. Package dimensions



11 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|-------------|----------|---------------|
| 14-Dec-2010 | 1 | First release |

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