INIC-1608
USB to SATA Bridge
Specification

Version 1.0
August 10, 2007
Initio Corporation

Change History:
Create on 07/06/2007.

Table of Contents

1. Introduction:

The INIC-1608 provides an advanced solution to connect SATA devices to USB Host with integrated CPU and embedded SRAM/ROM. To provide high performance and cost effective solution, the INIC-1608 integrates USB-PHY, Mass Storage Class Bulk-Only USB function, SATA link/PHY core and microprocessor into a single ASIC. The INIC-1608 provides the data transfer rate of up to 60 MB/sec connecting to a 1.5G SATA interface.

1.1 Feature Summary

- Integrates USB2.0 PHY IP core.
- Data transfer rate of up to 60 MB/sec.
- Integrated internal Turbo 8051 uP with 12KB embedded ROM and 2KB SRAM.
- External NVRAM supported.
- Support HID.
- Up to 8 GPIO pins.
- Only one external crystal.
- Supports SATA (bridged SATA) Hard Disk drives, CD-RW devices, DVDs, Removable media devices, BD (Blu-Ray Disc) drive
- USB 1.1 and USB 2.0 compliant.
- USB Mass Storage Class Bulk-Only Transport Specification Compliant.
- SATA specification 1.0, SATA II Compliant (Hot Plug is supported).
- Support ATA/ATAPI device DMA and PIO mode.
- 2k bytes of data buffer for data transfer.
- On-Chip 3.3V to 1.8V regulator and 5V to 3.3V regulator.
- 48 pin LQFP

1.2 Firmware/Software Support

- USB Mass Storage Class Bulk-Only Transport support
- Provide software utilities for NVRAM upgraded.

1.3 Devices Support

- Hard disk drives
- CD-RW devices
- DVDs
- Removable media devices
- Blu-Ray Disk driver

2. INIC-1608 Block Diagram:

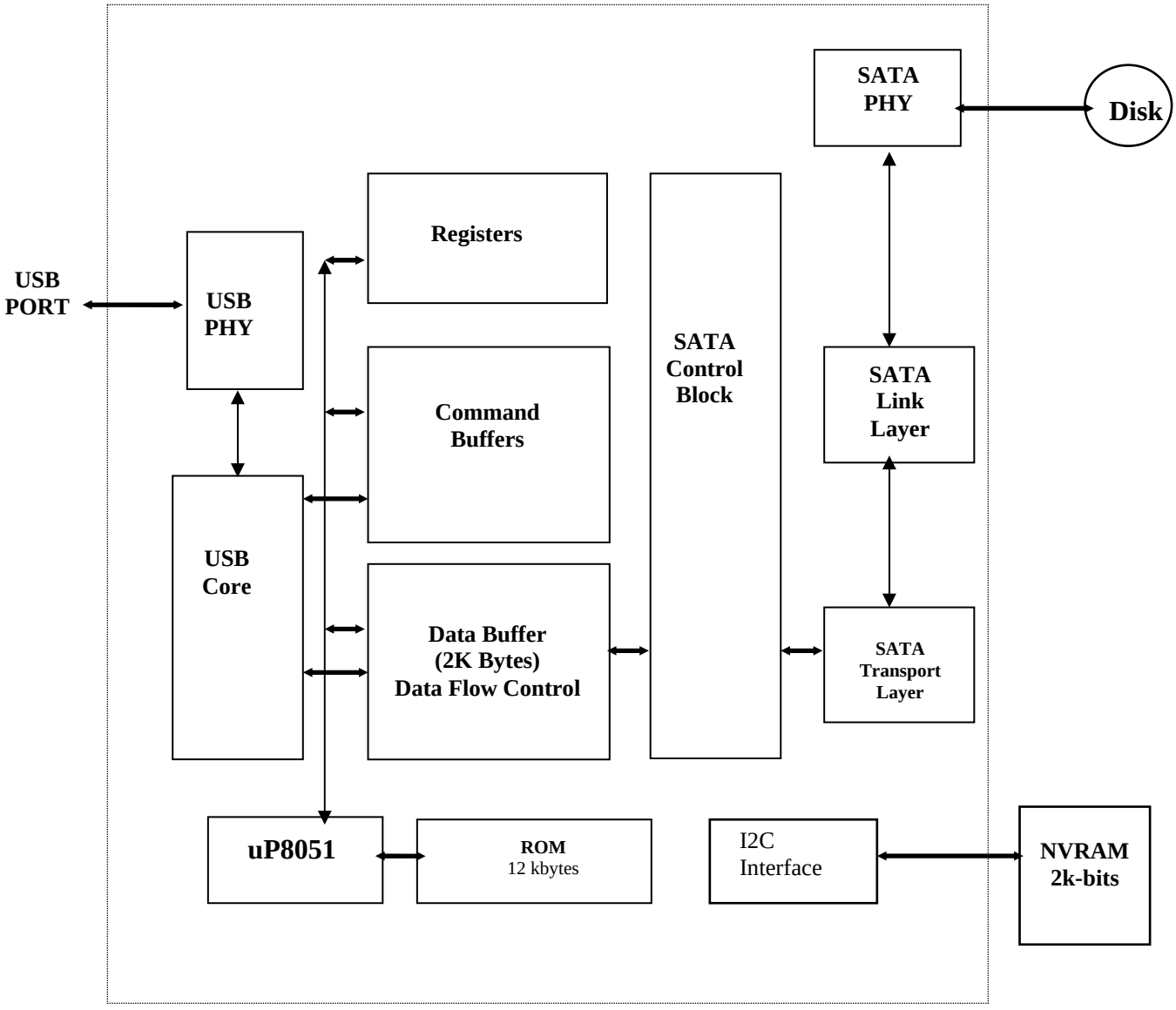
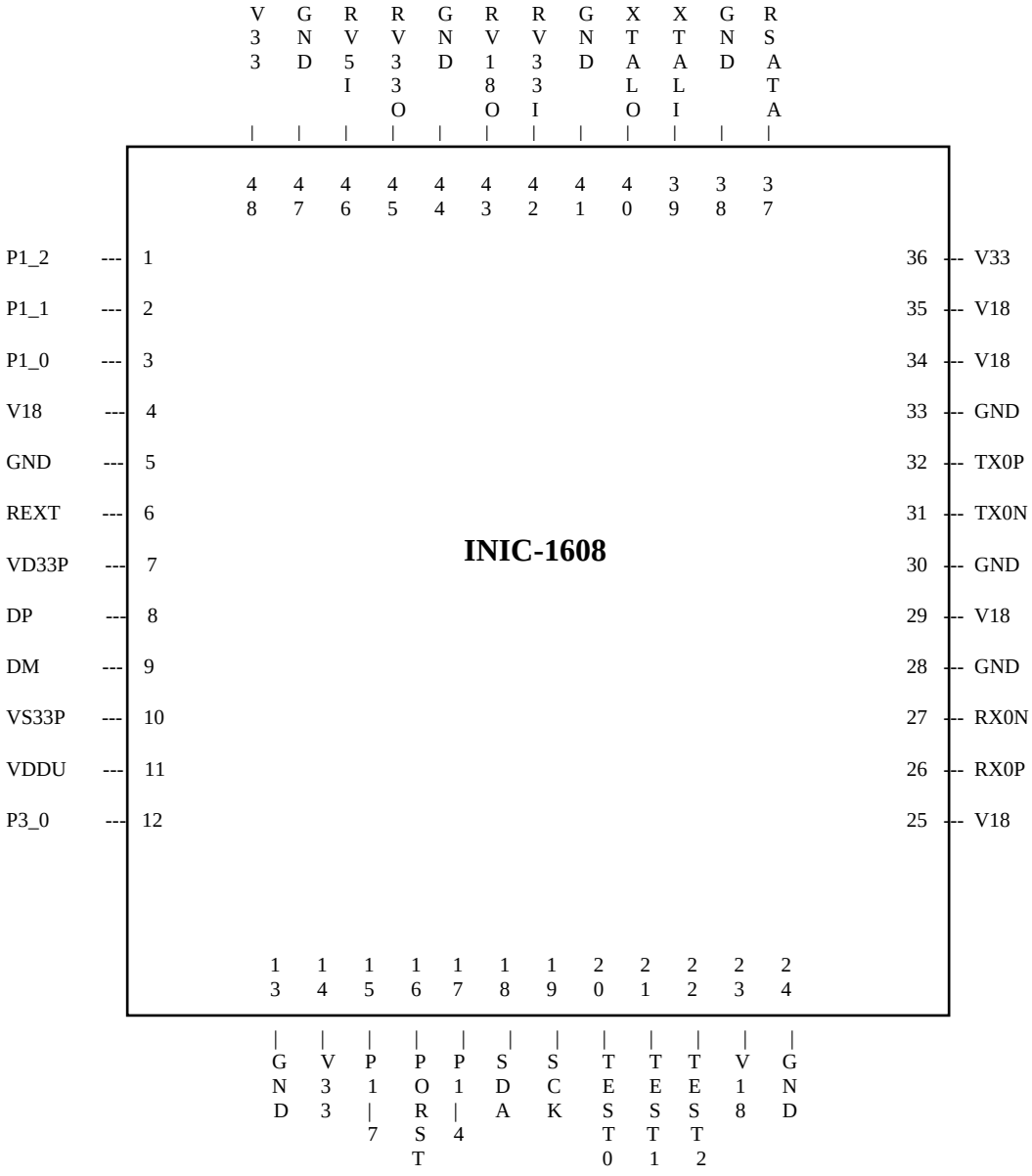


Figure1: USB to SATA Bridge Block Diagram

3. Pin-Out Diagram:



4. Pin Signal Description: (48-pin package)

4.1 USB Interface

Signal Name	Pin Number	I/O	Driver Type	Description
DP	8	I/O	USB high /full speed buffer (D+)	High/Full speed D+ signal
DM	9	I/O	USB high/full speed buffer (D-)	High/Full speed D- signal
REXT_USB	6	A	Power	PLL voltage reference. Current source for 330 ohm(1%) resistor connected to AVSS

4.2 SATA Interface (Analog pins)

Signal Name	Pin Number	I/O	Driver Type	Description
TX0P (SATA Device)	32	O	SATA	Differential Transmit positive signal line
TX0N (SATA Device)	31	O	SATA	Differential Transmit negative signal line
RX0P (SATA Device)	26	I	SATA	Differential Receive positive signal line
RX0N (SATA Device)	27	I	SATA	Differential Receive negative signal line
XTALI	39	I	PX1R	crystal oscillator input (25MHz)
XTALO	40	O		Crystal oscillator output
RSATA	37	I		External Reference Resister (6.19 K ohm)

4.3 System Interface

Signal Name	Pin Number	I/O	Driver Type	Description
PORST	16	I	Schmitt-trigger	Power On Reset. Active low

4.4 Miscellaneous Interface

Signal Name	Pin Number	I/O	Driver Type	Description
TestMode[2:0]	22,21,20	I	Internal pulldown 77Kohm—312Kohm	Test Mode Select 000: Normal 001: rom-bist 010: tstpDO control by CPU 011: tstpDO monitor rom addr 111: USB PHY test 100: SATA PHY test 101: Scan Test 110: Mbist Test

4.5 NVRAM Interface

Signal Name	Pin Number	I/O	Driver Type	Description
SDA/ P1.6	18	I/O	Internal pullup 94Kohm— 261Kohm	1. NRAM data input/output. 2. This pin also configured as P1.6 if NVRAM is not used.
SCK/ P1.5	19	I/O	Internal pullup 94Kohm— 261Kohm	1. NVRAM clock. 2. This pin also configured as P1.5 if NVRAM is not used

4.6 GPIO Interface

Signal Name	Pin Number	I/O	Driver Type	Description
LED/P1.7	15	I/O	Internal pullup 94Kohm— 261Kohm	LED: SATA Activity indicator. Can be used as uP8051 port 1.7
P3.0/VBUS	12	I/O	Schmitt-trigger	uP8051 I/O port 3.0, can be used as VBUS detection
P1.4	17	I/O	Internal pullup 94Kohm— 261Kohm	uP8051 I/O port 1.4, can be used as GPIOs **OTB input if enable OTB**
P1.2	1	I/O	Internal pullup 94Kohm— 261Kohm	uP8051 I/O port 1.2, can be used as output GPIO
P1.1	2	I/O	Internal pullup 94Kohm— 261Kohm	uP8051 I/O port 1.2, can be used as output GPIO
P1.0	3	I/O	Internal pullup 94Kohm— 261Kohm	uP8051 I/O port 1.0, can be used as GPIOs

4.7 Power Regulator pins

Signal Name	Pin Number	I/O	Driver Type	Description
RV33I	42	I		REG 3.3V input
RV18O	43	O		REG 1.8V output
GND	44,41	I		Ground for 2 Regulators
RV5I	46	I		REG 5V input
RV33O	45	O		REG 3.3V output

4.8 Power/GND

Signal Name	Pin Number	I/O	Driver Type	Description
V33	14,48			2 pins (Digital 3.3V) for core
V18	4,23			2 pins (Digital 1.8V) for core
GND	5,13,24,47			4 pins
VD33P	7			For USB (3.3V)
VS33P	10			For USB (GND)
VDDU	11			For USB (1.8V)
V33	36			For SATA(3.3V)
V18	25,29,34,35			For SATA(1.8V)
GND	28,30,33,38			For SATA(GND)

5. Register Address Mapping:

5.1 General Registers

Address	Read Value	Write Value
40A3h	BufferRst	BufferRst
40A6h	TestCtl	TestCtl
40A7	TestCtl1	TestCtl1
40ACh	LED_spd	LED_spd
40ADh	MiscEn	MISCEn
40AFh	MiscCtl	MiscCtl
40B1h	DmaFlush	DmaFlush
40B2h	USB Channel Set	USB Channel Set
40B3h	USB Channel Clear	USB Channel Clear
40B4h	Dir/D2BEn	Dir/D2BEn
40B5h	Run	Run
40B6h	Sata Config	Sata Config
40B7h	Sata Reset	Sata Reset
40B8h	SataStatus	NA
40E0h	I2C_Addr[7:0]	I2C_Addr[7:0]
40E1h	I2C_Data	I2C_Data
40E2h	I2C_Ctrl	I2C_Ctrl
40E3h	I2C_Comm	I2C_Comm
40E4h	I2C_Status	-
4040	OTB_Counter[7:0]	OTB_Counter[7:0]
40E9h	OTB_Ctrl[7:0]	OTB_Ctrl[7:0]
40EAh	OTB_INT_En	OTB_INT_En
40F0h	UsbINT_En	UsbINT_En
40F2h	sataINT_En	sataINT_En
40F4h	GPIO_P_INT_En	GPIO_P_INT_En
40F5h	GPIO_N_INT_En	GPIO_N_INT_En
40F7h	Buffer Clear	Buffer Clear
40F8h	GPIOEn	GPIOEn
40F9h	GPIODataIn	GPIODataOut
40FAh	GPIOoutEn	GPIOoutEn
40FBh	USB Clear	USB Clear

5.2 Buffers

Address	Read Value	Write Value
4100h-413Fh (64 bytes)	Control_in Buffer	Can't be written by CPU
4140h-417Fh (64 bytes)	CBW_in Buffer	CBW_in Buffer
41C0h-41FFh (64 bytes)	Control_out Buffer	Control_out Buffer
4240h-427Fh (64 bytes)	CSW_out Buffer	CSW_out Buffer
4280h-423Fh (64 bytes)	HID_out Buffer	HID_out Buffer

5.3 USB Control Registers

Address	Read Value	Write Value
4500h-450Fh	USB Control	USB Control

5.4 SATA Control Registers

Address	Read Value	Write Value
4800h	Reserved	Reserved
4801h	ATA Error Shadow	ATA Error Shadow
4802h	ATA Status Shadow	ATA Status Shadow
4803h	Control Flag	Control Flag
4804h-480Fh	Reserved	Reserved
4810h	ATA Feature Shadow	ATA Feature Shadow
4811h	ATA Extended Feature Shadow	ATA Extended Feature Shadow
4812h	ATA Device/Head Shadow	ATA Device/Head Shadow
4813h	Reserved	Reserved
4814h	ATA Sector Count Shadow	ATA Sector Count Shadow
4815h	ATA Extended Sector Count Shadow	ATA Extended Sector Count Shadow
4816h	ATA Sector Number Shadow	ATA Sector Number Shadow
4817h	ATA Extended Sector Number Shadow	ATA Extended Sector Number Shadow
4818h	ATA Cylinder Low Shadow	ATA Cylinder Low Shadow
4819h	ATA Extended Cylinder Low Shadow	ATA Extended Cylinder Low Shadow
481Ah	ATA Cylinder High Shadow	ATA Cylinder High Shadow
481Bh	ATA Extended Cylinder High Shadow	ATA Extended Cylinder High Shadow
481Ch	ATA Command Shadow	ATA Command Shadow
481Dh	ATA Control Shadow	ATA Control Shadow
4820h	SATA PHY Control [7:0]	SATA PHY Control [7:0]
4821h	SATA PHY Control [15:8]	SATA PHY Control [15:8]
4822h	SATA PHY Status [7:0]	SATA PHY Status [7:0]
4823h	SATA PHY Status [15:8]	SATA PHY Status [15:8]
4830h-4833h	SATA Status	SATA Status
4834h-4837h	SATA Error	SATA Error
4838h-483Bh	SATA Control	SATA Control
483Ch-483Fh	SATA Active	SATA Active

5.5 Data BUFFER

Address	Read Value	Write Value
5000h-57FFh	Data BUFFER	Data BUFFER

5.6 USB Registers

Address	Read Value	Write Value
6020h	Dev_Status	Dev_Status
6021h	Funct_Adr	Funct_Adr
6022h	Test_mode	Test_mode
6025h	EpTxLength[7:0]	EpTxLength[7:0]
6026h	EpTxLength[15:8]	EpTxLength[15:8]
6030h	EP0_Status	EP0_ Control (Set)

6031h	EP0_Status	EP0_ Control (Clear)
6032h	EP0_Status2	EP0_ Control 2(Set)
6033h	EP0_Status2	EP0_ Control 2(Clear)
6034h	EP0TxLength	EP0TxLength
6038-603F	Hdr0-7	-
6040h	EP1_Status	EP1_ Control (Set)
6041h	EP1_Status	EP1_ Control (Clear)
6050h	EP2_Status	EP2_ Control (Set)
6051h	EP2_Status	EP2_ Control (Clear)
6052h	Usb_rxLength[7:0]	-
6060h	EP3_Status	EP3_ Control (Set)
6061h	EP3_Status	EP3_ Control (Clear)
6070h	TotalCnt0	TotalCnt0
6071h	TotalCnt1	TotalCnt1
6072h	TotalCnt2	TotalCnt2
6073h	TotalCnt3	TotalCnt3
6074h	-	LoadTotalCnt
6080h	GTotalCnt0	GTotalCnt0
6081h	GTotalCnt1	GTotalCnt1
6082h	GTotalCnt2	GTotalCnt2
6083h	GTotalCnt3	GTotalCnt3

5.7 Data Space Mapping

Mapping Address	Type	Access Type	Mapping Block
0000h-07FFh	Data	Read/Write	Internal SRAM (2KB)
4000h-47FFh	Data	Read/Write	Internal Register/Buffers
4800h-48FFh	Data	Read/Write	SATA Registers
5000h-57FFh	Data	Read/Write	Data BUFFER (2KB)
6000h-60FFh	Data	Read/Write	USB Registers

5.8 Code Space: Internal ROM:

Address	Read Value	Write Value
0-3000h	Firmware Code (12K Bytes) (Instruction Fetch)	N/A

6. Programming Guide:

6.1 CPU Write NVRAM.

1. CPU write access address at register I2C_Addr(0x40E0).
2. CPU write data at register I2C_Data(0x40E1).
3. CPU write Control Code at register I2C_Ctrl(0x40E2).
4. CPU write Run and Read_Write direction(0) at register I2C_Comm(0x40E3).
5. CPU poll I2C_Comm bit 7, wait until cleared.
6. CPU may read register I2C_Status(0x40E4) to check write success or not.

6.2 CPU Read NVRAM.

1. CPU write access address at register I2C_Addr(0x40E0).
2. CPU write Control Code at register I2C_Ctrl(0x40E2).
3. CPU write Run and Read_Write direction(1) at register I2C_Comm(0x40E3).
4. CPU poll I2C_Comm bit 7, wait until cleared.
5. CPU read register I2C_Data(0x40E1).
6. CPU may read register I2C_Status(0x40E4) to check read success or not.

6.3 CPU Poll NVRAM.

After write data to NVRAM, NVRAM need certain time before next write operation can be accepted. CPU may poll NVRAM to decide NVRAM ready or not. It is done same as a NVRAM read. If I2C_Status(0x40E4) bit 0 is 1, the NVRAM not ready.

6.4 Host Read/Write 8051 data space from USB

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1608 here. Default hardware report PID is 0x160f.
2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.
3. Host may send DATA_WRITE/DATA_READ packet through control channel to WRITE/READ 8051 data space.

DATA_WRITE setup packet format is,

offset	field	size	value	Description
0	bmReqType	1	0x40	Vendor write
1	bReq	1	0x81	Data space write
2	wValue	2	Addr[7:0]	Address to be writen
3			Addr[15:8]	
4	wIndex	2	Data[7:0]	Data space data
5			0x00	Don't care
6	wLength	2	0x00	
7			0x00	

DATA_READ setup packet format is,

offset	field	size	value	data	Description

0	bmReqType	1	0xc0	Data from Data space	Vendor read
1	bReq	1	0x82		Data read
2	wValue	2	Addr[7:0]		Address to be writen
3			Addr[15:8]		
4	wIndex	2	0x00		Don't care
5			0x00		Don't care
6	wLength	2	0x01		
7			0x00		

READ_CHIP_ID setup packet format is:

Offset	Field	Size	Value	Data	Description
0	bmReqType	1	0xc0	Chip-ID 0x08, 0x16, 0xc9, 0x25	Vendor read
1	bReq	1	0x03		
2	wValue	2	0x00		
3			0x00		
4	wIndex	2	0x00		Don't care
5			0x00		Don't care
6	wLength	2	0x04		
7			0x00		

HOLD_CPU setup packet format is:

Offset	Field	Size	Value	Description
0	bmReqType	1	0x40	Vendor write
1	bReq	1	0x04	HOLD_CPU
2	wValue	2	0x00	Don't care
3			0x00	
4	wIndex	2	0x00	Don't care
5			0x00	Don't care
6	wLength	2	0x00	Don't care
7			0x00	Don't care

6.*5 NVRAM Download from USB cable*

The download utility may read/write NVRAM through access I2C registers similar as CPU does.

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1608 here. Default hardware report PID is 0x160f.
2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.

6.5.1 NVRAM Write.

3. Host send DATA_WRITE packet with wValue I2C_Addr(0x40E0) and wIndex[15:8] the NVRAM address to be accessed
4. Host send DATA_WRITE packet with wValue I2C_Data(0x40E1) and wIndex[15:8] the value to be write to NVRAM
5. Host send DATA_WRITE packet with wValue I2C_Ctrl(0x40E2) and wIndex[15:8] the Control Code to be write to NVRAM
6. Host send DATA_WRITE packet with wValue I2C_Comm(0x40E3) and wIndex[15:8] the Run bit[b7] and read/write direction 0 [b0]

7. Host poll bit 7 of I2C_Comm(0x40E3) until this bit is cleared by sending DATA_READ packet with wValue I2C_Comm(0x40BF)
8. Host send DATA_READ packet with wValue I2C_Status(0x40E4) to check write success or not

6.5.2 NVRAM Read.

9. Host send DATA_WRITE packet with wValue I2C_Addr(0x40E0) and wIndex[15:8] the NVRAM address to be accessed
10. Host send DATA_WRITE packet with wValue I2C_Ctrl(0x40E2) and wIndex[15:8] the Control Code to be write to NVRAM
11. Host send DATA_WRITE packet with wValue I2C_Comm(0x40E3) and wIndex[15:8] the Run bit[b7] and read/write direction 1 [b0]
12. Host poll bit 7 of I2C_Comm(0x40E3) until this bit is cleared by sending DATA_READ packet with wValue I2C_Comm(0x40E3)
13. Host send DATA_READ packet with wValue I2C_Data(0x40E1) to get the data from NVRAM.
14. Host send DATA_READ packet with wValue I2C_Status(0x40E4) to check write success or not

6.5.3 NVRAM Polling.

Just same as NVRAM Read. If I2C_Status(0x40E4) bit 0 is 1, NVRAM not ready for next write.

7. Register Descriptions:

7.1 BUFFER Reset Register (0x40A3)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	7'b0	Reserved.
Buffer0Rst	rw	0	1'b0	DMA BUFFER 0 Reset. This bit is used to reset DMA BUFFER 0. This bit is self-cleared by hardware after set.

7.2 Test Control Register (0x40A6)

Field name	rscu	bit #	reset	Description
Reserved	r	7-5	3'b0	Reserved.
ChipID	r	4	1'b0	Chip-ID. Read only. 1-> 1608 0-> 1606
TestMuxSel	rw	3-0	4'h0	Test mux output select. These 4 bits select specific internal signals to be routed to device's outputs during test mode. (internal testing purpose)

7.2.0 Test Control Register (0x40A7)

Field name	rscu	bit #	reset	Description
SE0_En	rw	7	1'b0	Reserved.
RevID	r	6:3	1'b0	Rev-ID.
Squ_b	rw	2-0	3'b111	SATA PHY Control Reserved

7.2.1 LED_spd register (0x40AC)

Field name	rscu	bit #	reset	Description
Out_Abort_En	rw	7	1'b0	0->enable Out abort
usbAtaDone_En	rw	6	1'b0	1-> enable usbAtaDone clear internal counter
cpuClkSwitch_En	rw	5	1'b0	0-> cpu clock is 75Mhz 1-> cpu clock is 10Mhz(150Mhz/16)
Usb_WakeUpEn	rw	4	1'b0	1: Enable external interrupt wakeup USB when device is now in suspend

				state.
LED_spd [3 : 0]	rw	3-0	4'h0	Define LED blink speed : 0000 : 1/32 sec. per blink 0001 : 2/32 sec. per blink Up to ~ ~ 1111 : 16/32 sec. per blink

7.2.2 MiscEn register (0x40AD)

Field name	rscu	bit #	reset	Description
Force_usbMode	r	7	1'b0	1-> set usbMode
Start_Calib1_En	rw	6	1'b0	1 : Allow SATA OOB to do calibration for SATA host channel
iVbus_Sel_En	r	5	1'b0	1->Enable internal VBUS re-rounting
TL_Wakeup	rw	4	1'b0	Control bit for SATA block
TL_Slumber	rw	3	1'b0	Control bit for SATA block
TL_Partial	rw	2	1'b0	Control bit for SATA block
Sata_busy_sel	rw	1	1'b0	0 : Select sata_busy as sata device activity detection 1 : Select (sata_busy or sata_drq) as sata device activity detection
Reserved	r	0	1'b0	Reserved-for SATA

7.3 MiscCtl register (0x40AF): This 8-registers is in lclk domain (37.5 MHz)

Field name	rscu	bit #	reset	Description
USB_Crystal_En	rw	7	1'b0	1->turn off USB clock
bp_sel	rw	6	1'b1	0: select USB mode 1: select SATA-to-SATA bypass mode.
USB_CLK_Ctl	rw	5	1'b0	Firmware set/clr this bit. If set, PHY clock is free run. If clr, PHY clock will stop when device goes to suspend mode.
Usb_Enumeration	rw	4	1'b1	1: Enable USB Enumeration. 0: Disable USB Enumeration.
HW_Rst_Event	rw	3	1'b1	This bit is set by hardware reset. Software reset has no effect on this bit. Firmware can clear this bit by writing a 0 to it.
HidEn	rw	2	1'b0	1 : Endpoint defined as: 8(IN), 2(OUT), 1(INT) 0 : Endpoint defined as: 1(IN), 2(OUT), 3(INT)
NewMode	rw	1	1'b0	1 : 1608 report residue same as totalCnt minus USB Txed or Rxed 0 : 1608 report residue same as totalCnt minus ATA Txed or Rxed
iVbus	rw	0	1'b0	The value of VBUS is equivalent this bit if iVbus_Sel_En(0x40Ad[5]) is set.

7.4 SoftRst register (0x40B0)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	7'b0	Reserved.
SoftRst	w	0	1'b0	1: Software reset (setting this bit will reset the data buffer related logic)

7.5 DMA Flush register (0x40B1)

Field name	rscu	bit #	reset	Description
sgBufCpuRd	rw	7	1'b0	F/W read sgBuf in Fifo mode, F/W set this bit first.
Reserved	r	6-1	6'b0	Reserved
Flush/Abort	rw	0	1'b0	When DMA BUFFER is overrun, this bit is used by firmware to flush data out for outgoing data or abort the DMA operation for incoming data. This bit is self-cleared by hardware.

7.6 USB Channel Set/Clear register (0x40B2 Set) (0x40B3 Clear)

Field name	rscu	bit #	reset	Description
Reserved	r	7	7'b0	Reserved

CmdTx4Run (for HID_out)	rwu	6	1'b0	The Set register is set by software and cleared by hardware when transfer is completed. When the Clear register is set by software, the corresponding channel is cleared.
CmdTx3Run (for CSW_out)	rwu	5	1'b0	The Set register is set by software and cleared by hardware when transfer is completed. When the Clear register is set by software, the corresponding channel is cleared.
Reserved	r	4	1'b0	Reserved
CmdTx1Run (for Control_out)	rwu	3	1'b0	The Set register is set by software and cleared by hardware when transfer is completed. When the Clear register is set by software, the corresponding channel is cleared.
Reserved	r	2-0	3'b0	Reserved

7.7 Dir/D2BEn register (0x40B4)

Field name	rscu	bit #	reset	Description
Dir	rw	7	1'b0	Indicates the direction of the data transfer: 0: Data write into SATA device. 1: Data output from SATA device. Proper Dir bit must be programmed before writing ATA command
D2BEn	rw	6	1'b0	Data to Buffer Mode Enable. The two SATA channels can be configured to transfer data to and from the buffer memory without a host connection.
Reserved	r	5-0	6'b0	Reserved

7.8 Run register (0x40B5)

Field name	rscu	bit #	reset	Description
PhaseError	rws	7	1'b0	Phase Error status. Set by hardware.
Reserved	r	6-1	6'b0	Reserved
Run	rw	0	1'b0	Write 1: Start the data transfer; the hardware will clear this bit when the transfer is completed. Firmware also can write 0 to clear this bit. D2BEn (Register 0x40B4 bit 6) and Run (Register 0x40B5 bit 0) work together to start different data transfer: D2BEn Run 0 0 : Idle 0 1 : Start transfer between USB and SATA device according to the DIR bit (Register 0x40B4 bit 7). 1 0 : Idle 1 1 : Start transfer between DMA buffer and SATA device according to the DIR bit (Register 0x40B4 bit 7)

7.9 SATA Config register (0x40B6)

Field name	rscu	bit #	Reset	Description
HwFlushEn	rw	7	1'b1	When set to 1: automatic hardware flush is enabled.
PhaseErrEn	rw	6	1'b1	When set to 1: An PhaseErr event will report PhaseErr to register 0x40B5 bit 7.
LED_Idle_HIGH	rw	5	1'b0	0: SATA idle will drive LED pin LOW 1: SATA idle will drive LED pin HIGH

LED_busy_sel	rw	4	1'b0	0 : SATA busy will blink LED 1 : SATA busy will drive LED ON
Reserved	r	3-0	4'b0	Reserved

7.10 SATA Reset register (0x40B7)

Field name	rscu	bit #	reset	Description
ATAPhyRst	rw	7	1'b0	SATA channels Hard reset to Phy layer, Auto-Clear by hardware
Reserved	r	6-5	2'b0	Reserved.
ATAUppRst	rw	4	1'b0	SATA Channel 0 reset to Link/Transport/Application layer
Reserved	r	3-1	3'b0	Reserved.
AtaCh0INT	r	0	1'b0	SATA Channel 0 interrupt signal.

7.11 I2C_Addr Register (0x40E0)

Field name	rscu	bit #	reset	Description
I2C_Addr	rw	7-0	8'h0	CPU writes the to-be executed NVRAM address to this register.

7.12 I2C_Data Register (0x00xE1) (I2C Data port)

Field name	rscu	bit #	reset	Description
I2C_Data	rw	7-0	8'h0	This is the data port for CPU to access NVRAM A: To Write to NVRAM: CPU Writes a 8-bit data to this port, Hardware will send this data to NVRAM B: To Read from NVRAM: CPU reads this port to get data from NVRAM

7.13 I2C_Ctrl Register (0x40E2) (I2C Control Code)

Field name	rscu	bit #	reset	Description
Reserved	w	7	1'b0	reserved
Control_Code	rw	6:3	4'b0	Control Code
Block_Select	rw	2:0	3'b0	I2C device block select bits

7.14 I2C_COMM Register (0x40E3)

Field name	rscu	bit #	reset	Description
I2C_TX_START	rw	7	1'b0	1-> Hardware start to Read/Write NVRAM. Clear by hardware when finished.
reserved	rw	6:1	6'b0	reserved
Rd_nWr	wr	0	1'b0	0-> write to NVRAM 1-> read data from NVRAM

7.15 I2C_Status Register (0x40E4)

Field name	rscu	bit #	reset	Description
reserved	rw	7-3	5'b0	reserved
Data_Ack	r	0	1'b0	0-> NVRAM ACK with Data write phase 1->NVRAM NACK with Data write phase
Addr_Ack	r	0	1'b0	0-> NVRAM ACK with Address write phase 1->NVRAM NACK with Address write phase
Ctrl_Ack	r	0	1'b0	0-> NVRAM ACK with Contrl Code write phase 1->NVRAM NACK with Contrl Code write phase

7.16 OTB_Counter Register (0x40E8)

Field name	rscu	bit #	reset	Description
OTB_Counter	rw	7:0	8'b0	How many push-release done. Clear after FW read.

7.16.1 OTB_Ctrl Register (0x40E9)

Field name	rscu	bit #	reset	Description
I2C_Enable	rw	7	1'b0	0-> I2C enable 1-> I2C disable, SCK(pin 21) as 8051 port 1.5 SDA(pin 20) as 8051 port 1.6
OTB_Enbale	rw	6	1'b0	0-> OTB enable, 8051 port 1.4 as button input 1-> OTB disable, 8051 port 1.4 as GPIO
reserved	rw	5:2	4'b0	reserved
Debouncing time	rw	1:0	2'b0	2'b00-> 36ms 2'b01->72ms 2'b10->108ms 2'b11->144ms

7.16.2 OTB_INT_Enable Register (0x40EA)

Field name	rscu	bit #	reset	Description
OTB_Counter_INTE	rw	7	1'b0	1: Enable OTB_Counter<>0 trigger sysINT.
OTB_pos_INTE	rw	6	1'b0	1: Enable button RELEASE trigger sysINT
OTB_neg_INTE	rw	5	1'b0	1: Enable button PUSH trigger sysINT
reserved	rw	4:0	5'b0	reserved

7.17 usb_INT_Enable Register (0x40F0)

Field name	rscu	bit #	reset	Description
Usb_busRst_INT_En	rw	7	1'b0	1: Enable Usb_busRst to trigger sysINT. To check if this INT has occurred, please read register 6030 bit 6.
Usb_bulkOnlyRst_INT_En	rw	6	1'b0	1: Enable Usb_bulkOnlyRst to trigger sysINT. To check if this INT has occurred, please read register 6030 bit 5.

Usb_Ep0Req_INT_En	rw	5	1'b0	1: Enable Usb_ Ep0Req to trigger sysINT. To check if this INT has occurred, please read register 6032 bit 0.
Usb_CBW_INT_En	rw	4	1'b0	1: Enable Usb_CBW to trigger sysINT. To check if this INT has occurred, please read register 6050 bit 1.
Usb_wakeup_INT_En	rw	3	1'b0	1: Enable Usb_wakeup to trigger sysINT. To check if this INT has occurred, please read register 6020 bit 3. (value 0 means wakeup)
Usb_suspendINT_En	rw	2	1'b0	1: Enable Usb_suspend to trigger sysINT. To check if this INT has occurred, please read register 6020 bit 3. (value 1 means suspend)
VBUS_P__INT_En	rw	1	1'b0	1: Enable positive of VBUS to trigger sysINT. To check if this INT has occurred, please read register 40AF bit 6. (value 1 means VBUS is high)
VBUS_N__INT_En	rw	0	1'b0	1: Enable negative of VBUS to trigger sysINT. To check if this INT has occurred, please read register 40AF bit 6. (value 1 means VBUS is high)

7.18 SATA_INT_Enable Register (0x40F2)

Field name	rscu	bit #	reset	Description
Reserved	r	7-4	4'b0	Reserved
SATA_Busy_INT_En	rw	3	1'b0	1: Enable SATA host detection to trigger sysINT
SATA_Dev_INT_En	rw	2	1'b0	1: Enable SATA_Dev_INT to trigger sysINT. To check if this INT has occurred, please read register 40B7 bit 0.
SATA_PhyRdy_P_INT_En	rw	1	1'b0	1: Enable positive of SATA_PhyRdy to trigger sysINT. To check if this INT has occurred, please read register 4820 bit 0.
SATA_PhyRdy_N_INT_En	rw	0	1'b0	1: Enable negitive of SATA_PhyRdy to trigger sysINT. To check if this INT has occurred, please read register 4820 bit 0.

7.19 SATA_BUSY_INT Register (0x40F3)

Field name	rscu	bit #	reset	Description
Reserved	r	7-4	4'b0	Reserved
SATA_BUSY_INT	rw	3	1'b0	'1' indicates a sysINT caused by SATA host detection has occurred. Firmware can write '1' to clear this status bit. 1. USB to SATA mode If this bit set, SATA cable was plugged. Whenever F/W clear it, this bit will be set periodically unless firmware switches to SATA mode. 2. SATA to SATA mode If this bit set, SATA cable was plugged. After the connection between Host and Device has been built, this bit won't be set anymore after it was cleared by firmware unless the bus reset has occurred or SATA cable has been un-plugged and re-plugged. If Squelch bit (0x4822) set is detected, SATA cable was unplugged.

Reserved	r	2-0	3'b0	Reserved

7.20 GPIO_P_INT_Enable Register (0x40F4)

Field name	rscu	bit #	reset	Description
Reserved	rw	7-4	4'b0	Reserved
GPIO3_P_INT_En	rw	3	1'b0	1: Enable GPIO3 High level to trigger sysINT.
GPIO2_P_INT_En	rw	2	1'b0	1: Enable GPIO2 High level to trigger sysINT.
GPIO1_P_INT_En	rw	1	1'b0	1: Enable GPIO1 High level to trigger sysINT.
GPIO0_P_INT_En	rw	0	1'b0	1: Enable GPIO0 High level to trigger sysINT.

7.21 GPIO_N_INT_Enable Register (0x40F5)

Field name	rscu	bit #	reset	Description
Reserved	r	7-4	4'b0	reserved
GPIO3_N_INT_En	rw	3	1'b0	1: Enable GPIO3 Low level to trigger sysINT.
GPIO2_N_INT_En	rw	2	1'b0	1: Enable GPIO2 Low level to trigger sysINT.
GPIO1_N_INT_En	rw	1	1'b0	1: Enable GPIO1 Low level to trigger sysINT.
GPIO0_N_INT_En	rw	0	1'b0	1: Enable GPIO0 Low level to trigger sysINT.

7.22 Buffer Clear Register (0x40F7)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	7'b0	reserved
Clear Buffer	rw	0	1'b0	1: Clear data Buffer and state machine.

7.23 GPIO_Enable Register (0x40F8)

Field name	rscu	bit #	reset	Description
Reserved	rw	7-1	7'b0	reserved
GPIO0 _En	rw	0	1'b0	1: use P1_7 pin as GPIO0

7.24 GPIO_Data Register (0x40F9)

Field name	rscu	bit #	reset	Description
Reserved	rw	7-1	7'b0	reserved
GPIO0 _Data	rw	0	1'b0	Read: Read the value of P1_7 pin (i.e. GPIO0_DataIn) Write: Write the value to GPIO0_DataOut (i.e. P1_7 pin)

7.25 GPIO_Output_Enable Register (0x40FA)

Field name	rscu	bit #	reset	Description
Reserved	rw	7-1	7'b0	reserved
GPIO0_Output_En	rw	0	1'b0	0: Select GPIO0 to input mode 1: Select GPIO0 to output mode

7.26 USB Clear Register (0x40FB)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	4'b0	reserved
Clear USB	rw	0	1'b0	1: Clear USB traffic problem. (When USB traffic encounter problem)

7.27 Buffer Address Map

Address	Description
4100-413Fh	Control_in Buffer, 64 bytes
4140-417Fh	CBW_in Buffer, 64 bytes
41C0-41FFh	Control_out Buffer, 64 bytes
4240-426Fh	CSW_out Buffer, 48 bytes
4280-42AFh	HID_out Buffer, 48 bytes

7.28 USB Control

Address	Description
4500-450Fh	USB Control

```
450Eh bit 7-0: dataLength[7:0]
450Fh bit 7-0: dataLength[15:8]
```

8. SATA CHANNEL REGISTERS (0x4800-0x483F):

8.1 Command Parameter Blocks (CPB) Structure Definition

31 24	23 16	15 08	07 00	
Control Flag	ATA Status	ATA Error	Reserved	4800h
Reserved				4804h
Reserved				4808h
Reserved				480Ch
Port Sel.	ATA Device/Head	ATA Ex. Feature	ATA Feature	4810h
ATA Ex. Sector Number	ATA Sector Number	ATA Ex. Sector Count	ATA Sector Count	4814h
ATA Ex. Cylinder High	ATA Cylinder High	ATA Ex. Cylinder Low	ATA Cylinder Low	4818h
Reserved	Reserved	ATA Control	ATA Command	481Ch

8.1.1. ATA Error Shadow

Offset: 4801h

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Error register after status update.

Bit		Name	Definition
07-00	0	ATAERR	ATA Error Register content.

8.1.2. ATA Status Shadow
Offset: 4802h

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Status register after status update.

Bit		Name	Definition
07-00	0	ATASTAT	ATA Status Register content.

8.1.3. Control Flags
Offset: 4803h

Bit		Name	Definition
7:3	5'b0	Pkt_Length	Packet command CDB structure size in bytes.
2:1	2'b0	Reserved	Reserved
0	1'b0	PPKT	Packet Command. When set, indicating the current command is an ATAPI packet command. After sending the register FIS to the device, hardware will automatically fetch the CDB from cmdReceive buffer and send to device through PIO.

8.1.4. Reserved
Offset: 4804-4807h

8.1.5. ATA Feature Shadow
Offset: 4810h

Bit		Name	Definition
07-00	0	ATAFEAT	ATA Feature Register content.

8.1.6. ATA Extended Feature Shadow
Offset: 4811h

Bit		Name	Definition
07-00	0	ATAEXFEAT	ATA Extended Feature Register content.

8.1.7. ATA Device/Head Shadow
Offset: 4812h

Bit		Name	Definition
07-00	0	ATADEVHD	ATA Device/Head Register content.

8.1.8. ATA Sector Count Shadow
Offset: 4814h

Bit		Name	Definition
07-00	0	ATASECCNT	ATA Sector Count Register content.

8.1.9. ATA Extended Sector Count Shadow
Offset: 4815h

Bit		Name	Definition
07-00	0	ATAEXSECCNT	ATA Extended Sector Count Register content.

8.1.10. ATA Sector Number Shadow
Offset: 4816h

Bit		Name	Definition
07-00	0	ATASECNUM	ATA Sector Number Register content.

8.1.11. ATA Extended Sector Number Shadow
Offset: 4817h

Bit		Name	Definition
07-00	0	ATAEXSECNUM	ATA Extended Sector Number Register content.

8.1.12. ATA Cylinder Low Shadow
Offset: 4818h

Bit		Name	Definition
07-00	0	ATACYLLO	ATA Cylinder Low Register content.

8.1.13. ATA Extended Cylinder Low Shadow
Offset: 4819h

Bit		Name	Definition
07-00	0	ATAEXCYLLO	ATA Extended Cylinder Low Register content.

8.1.14. ATA Cylinder High Shadow
Offset: 481Ah

Bit		Name	Definition
07-00	0	ATACYLHI	ATA Cylinder High Register content.

8.1.15. ATA Extended Cylinder High Shadow
Offset: 481Bh

Bit		Name	Definition
07-00	0	ATAEXCYLHI	ATA Extended Cylinder High Register content.

8.1.16. ATA Command Shadow
Offset: 481Ch

Bit		Name	Definition
07-00	0	ATACMD	ATA Command Register content.

8.1.17. ATA Control Shadow
Offset: 481Dh

Bit		Name	Definition
07-00	0	ATACTL	ATA Control Register content.

8.2 SATA PHY Low Control Register (4820h)

Field name	rscu	bit #	Reset	Description
Pw_dn_txpll	rw	7	1'b0	Power down for TX_PLL
USB_Clk_Ctrl	Rw	6	1'b0	1: set usb clock free run 0: usb clock may stop when device in suspend mode
Pw_dn_rxpll	Rw	5	1'b0	Power down for RX_PLL
Reserved	Rw	4	1'b0	Reserved
Bypass_calib	Rw	3	1'b1	Disable calibration process during OOB
Farafleb	Rw	2	1'b0	Place PHY in far-end analog loopback mode
Nearafleb	Rw	1	1'b0	Place PHY in near-end analog loopback mode
Fphyrdy	Rw	0	1'b0	Force PHY ready for

8.3 SATA PHY HighControl Register (4821h)

Field name	rscu	bit #	Reset	Description
Reserved	Rw	15-13	3'b100	Reserved
Drv_level_ch1	Rw	12	1'b0	1: select 700mv output drive for channel 1 0: select 500mv output driver for channel 1
Pw_dn_ch0	Rw	11	1'b0	power down for channel 0 , bias circuit and calibration
Drv_level_ch0	Rw	10	1'b0	1: select 700mv output drive for channel 0 0: select 500mv output driver for channel 0
Pw_dn_ch1	Rw	9	1'b0	Power down for channel 1
Tx_pl_err_rst	Rw	8	1'b0	TX phase error reset

8.4 SATA PHY Low Status Register (4822h)

Field name	rscu	bit #	Reset	Description
OOB_status_1	R	7	1'b0	When 4bits OOB_staus_3~0 is 4'b1010, it means PHY is ready, all other states mean not ready
OOB_status_0	R	6	1'b0	
Reserved	R	5:4	2'b0	Reserved
Squelch	R	3	1'b0	SATA ch0 squelch signal out
Reserved	R	2:0	3'b0	Reserved

8.5 SATA PHY High Status Register (4823h)

Field name	rscu	bit #	Reset	Description
PhyStatus[15:10]	rw	15-10	6'h0	PHY Status[15:10]
OOB_status_3	R	9		When 4bits OOB_staus_3~0 is 4'b1010, it means PHY is ready, all other states mean not ready
OOB_status_2	r	8		

8.6 SATA Status Register (4830h-4833h)

Field name	rscu	bit #	Reset	Description

sStatus	r	31-0	32'b0	SATA Status

8.7 SATA Error Register (4834h-4837h)

Field name	rscu	bit #	Reset	Description
sError	r	31-0	32'b0	SATA Error

8.8 SATA Control Register (4838h-483Bh)

Field name	rscu	bit #	Reset	Description
sControl	rw	31-0	32'b0	SATA Control

8.9 Bist Mode Register (483Ch)

Field name	rscu	bit #	Reset	Description
Bist Mode	rw	7-6	2'h0	Not defined
Bist Mode_5	r/w	5	0	Far end loopback pattern will be sent out
Bist Mode_4	r/w	4	0	Far end Retimed loopback will be sent out
Bist Mode_3	r/w	3	0	Lone bit pattern will bet sent out
Bist Mode_2	r/w	2	0	High Freq. pattern will be sent out
Bist Mode_1	r/w	1	0	Mid Freq. pattern will be sent out
Bist Mode_0	r/w	0	0	Low Freq. pattern will be sent out

8.10 Sata_busy_drq_status(483Dh)

Field name	rscu	bit #	Reset	Description
Sata_busy_drq	rw	7-4	4'h0	
Sata_busy_drq_3	r/w	3	0	Dev_busy
Sata_busy_drq_2	r/w	2	0	Dev_drq
Sata_busy_drq_1	r/w	1	0	ATA_dev_busy
Sata_busy_drq_0	r/w	0	0	ATA_dev_drq

8.11 Bist_Act_Fis_0 Register (483Eh)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_0	rw	7-0	8'h0	Bist_act_fis data1[7:0]

8.12 Bist_Act_Fis_1 Register (483Fh)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_1	rw	7-0	8'h0	Bist_act_fis data1[15:8]

8.13 Bist_Act_Fis_2 Register (4840h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_2	rw	7-0	8'h0	Bist_act_fis data1[23:16]

8.14 Bist_Act_Fis_3 Register (4841h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_3	rw	7-0	8'h0	Bist_act_fis data1[31:24]

8.15 Bist_Act_Fis_4 Register (4842h)

Field name	rscu	bit #	Reset	Description

Bist_Act_Fis_4	rw	7-0	8'h0	Bist_act_fis data2[7:0]

8.15 Bist_Act_Fis_5 Register (4843h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_5	rw	7-0	8'h0	Bist_act_fis data2[15:8]

8.16 Bist_Act_Fis_6 Register (4844h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_6	rw	7-0	8'h0	Bist_act_fis data2[23:16]

8.17 Bist_Act_Fis_7 Register (4845h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_7	rw	7-0	8'h0	Bist_act_fis data2[31:24]

8.18 Bist_Act_Fis_8 Register (4846h)

Field name	rscu	bit #	Reset	Description
Bist_Act_Fis_8	rw	7-0	8'h0	Bist_act_fis pattern definition Write this register will trigger HW to send bist _act_fis (58) Out.

9. Data BUFFER:

Address	Read Value	Write Value
5000h-57FFh	Data BUFFER	Data BUFFER

10. USB Registers:

10.1 Device Status (Dev_Status[7:0], 0x6020)

Field name	rscu	bit #	reset	Description
VBUS	r	7	1'b0	Read: USB's VBUS status
Test_mode	rsu	6	1'b0	Set when SET_FEATURE (TEST_MODE).
Attach	ru	5	1'b1	Hardware reset default state. Clear if detect VBUS valid. Then set Power bit
Powered	ru	4	1'b0	Set if VBUS=1 & previous state is Attach. Or, power interruption.
Suspend	ru	3	1'b0	After bus IDLE for sometime, hardware set this bit. When RESUME detected, hardware reset this bit and return to previous state
Default	ru	2	1'b0	After bus reset, hardware set this bit.
Addressed	rscu	1	1'b0	Set_Address or Set_Configuration(0)
Configured	rscu	0	1'b0	Set_configuration

10.2 Function Address (Funct_Adr[7:0], 0x6021)

Field name	rscu	bit #	reset	Description
RSVD	ru	7	1'b0	Reserved
Adr	ru	6:0	7'b0	Set_Address

10.3 Test Mode (Test_mode[7:0], 0x6022)

Field name	rscu	bit #	reset	Description
RSVD	ru	7:4	4'b0	Reserved
Test_mode	rwu	3:0	4'b0	Test Mode Selectors(Table 9-7, USB2.0 spec) 4'h1: Test_J 4'h2: Test_K 4'h4: Test_SE0_NAK 4'h8: Test_Packet others: RSVD

10.4 End Point TX Data Length Low Bytes (Ep_TxLength[7:0], 0x6025)

Field name	rscu	bit #	reset	Description
Ep_TxLength	rwu	7:0	8'b0	For EP1 (Bulk_IN): For ATA-Command-no-DMA-involved, this field indicates how many bytes sent back to host. Maximum 512-bytes

10.5 End Point TX Data Length High Bytes (Ep_TxLength[15:8], 0x6026)

Field name	rscu	bit #	reset	Description
RSVD	r	7:2	6'b0	Reserved
Ep_TxLength	rwu	1:0	2'b0	High bytes

10.6 End Point 0 Status/Control (EP0_Status [7:0], 0x6030: Set, 0x6031: Clear)

Field name	rscu	bit #	reset	Description
Suspend_gnt	rsc	7	1'b0	Suspend-request granted
USB_busRst	rcu	6	1'b0	Set by hardware after an USB bus reset detected. Clear by firmware.
Bulk_only_Rst	rcu	5	1'b0	Set by hardware, read and cleared by firmware after firmware responds bulk-only-reset command done.
EP0_line_st	ru	4:3	2'b0	Line States
EP0_speed	ru	2	1'b0	1—HS, 0--FS
Remote_wakeup	rscu	1	1'b0	Set/Clr by firmware. Remote wakeup request.
Halt	rscu	0	1'b0	1-EP0 halt. Function STALL. Device reset is require to clear this bit

10.7 End Point 0 Status/Control2 (EP0_Status2 [7:0], 0x6032: Set, 0x6033: Clear, Bulk-IN)

Field name	rscu	bit #	reset	Description
FW_RDY	rsc	7	1'b0	0: Default value as no firmware installed. Hardware response all control packets for firmware download in most cases. 1: Firmware controls some setup packet response.
RSVD	r	6:4	3'b0	Reserved
EP0_StatRun	rsu	3	1'b0	Set by firmware if device ready to go to control status stage.
EP0_OUT	rcu	2	1'b0	Set by hardware if a control command-data is received. Clear by firmware after processing.
EP0_Run	rsu	1	1'b0	Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer

				length in the Ep_TxLength(0x25, 0x26)
EP0_Setup	rcu	0	1'b0	Set by hardware if a control command is received. Clear by firmware after processing.

10.8 End Point TX Data Length Low Bytes (Ep0TxLength [7:0], 0x6034)

Field name	rscu	bit #	reset	Description
RSVD	r	7	1'b0	Reserved
Ep0TxLength	rwu	6:0	7'b0	For EP0 (Control): This field is filled by firmware. When firmware taking control setup packet response, firmware write this field to inform hardware the data length to be send back to host. Maximum 64-bytes.

10.9 Setup Packet (Hdr0—Hdr7 [7:0], 0x6038—0x603F)

Field name	rscu	bit #	reset	Description
Hdr	ru	7:0	8'bx	8 bytes setup packet.

10.10 End Point 1 Status/Control (EP1_Status [7:0], 0x6040: Set, 0x6041: Clear, Bulk-IN)

Field name	rscu	bit #	reset	Description
GTotalCntEq0	r	7	0	1— Ata Global Total counter equal 0 0--- Ata Global Total counter not equal 0
TotalCntEq0	r	6	0	1— Ata Total counter equal 0 0--- Ata Total counter not equal 0
Short_IN	r	5	1'b0	1-> the last sent packet is a short packet. For bulk-in packet only
CBW_Err	r	4	1'b0	1-> indicate a wrong CBW received
CSW_Run	rscu	3	1'b0	Set by firmware when firmware ready to send CSW. Clear by hardware after CSW is sent successfully.
RSVD	r	2	1'b0	Reserved
EP1_Run	rscu	1	1'b0	Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer length in the Ep_TxLength(0x25, 0x26)
Halt	rscu	0	1'b0	1-EP1 halt.

10.11 End Point 2 Status/Control (EP2_Status [7:0], 0x6050: Set, 0x6051 Clear, Bulk-OUT)

Field name	rscu	bit #	reset	Description
FS_En	rw	7	1'b0	Force device to Full Speed only mode
RX_2K	rsc	6	1'b0	1-> bridge Rxed 2K bytes. Auto-clear after Rxed CBW
Short_OUT	r	5	1'b0	1-> the last received packet is a short packet. For bulk-out packet only
RX_DONE	rsc	4	1'b0	1->bridge received all data from host. Ready for CSW transmit. Auto-clear after Rxed CBW
Rx_TokenIN	rw	3	1'b0	1-> IN-Token received. Auto-clear after Rxed CBW
EP2_Rx	rcu	2	1'b0	Set by hardware after the bulk out packet received. The number of total data length received will be shown in Usb_rxLength register. This bit is used by firmware to monitor the data transfer between USB and internal data buffer. This bit is cleared by firmware or automatically cleared by hardware after the

				next CBW received or sg0Run bit set by firmware.
EP2_CBW	rcu	1	1'b0	Set by hardware if a valid CBW received. Clear after processing by firmware.
Halt	rscu	0	1'b0	1-EP2 halt.

10.12 Usb_rxLength (usb_rxLength[7:0], 0x6052, Bulk-OUT)

Field name	rscu	bit #	reset	Description
rxLength	ru	7:0	8'b0	The low byte of data length received. This register is used to show how many date received from USB to internal data buffer.

10.13 End Point 3 Status/Control (EP3_Status [7:0], 0x6060: Set, 0x6061: Clear, INTR-IN)

Field name	rscu	bit #	reset	Description
RSVD	r	7:3	5'b0	Reserved
EP3_run	rsu	2	1'b0	1—packet ready. Cleared by hardware after Tx completed
RSVD	r	1	1'b0	Reserved
Halt	rscu	0	1'b0	1-EP3 halt.

10.14 End Point TX Data Length Low Bytes (Ep3TxLength [7:0], 0x6062)

Field name	rscu	bit #	reset	Description
RSVD	r	7	1'b0	Reserved
Ep3TxLength	rwu	7:0	7'b0	For EP3 (INT_IN): This field is filled by firmware. Firmware writes this field to inform hardware the data length to be sent back to host. Maximum 64-bytes.

10.15 Total Count0 (TotalCnt[7:0], 0x6070 TotalCnt0)

Field name	rscu	bit #	reset	Description
TotalCnt0	rwu	7-0	8'b0	TotalCnt[7:0]

10.16 Total Count1 (TotalCnt[15:8], 0x6071 TotalCnt1)

Field name	rscu	bit #	reset	Description
TotalCnt1	rwu	7-0	8'b0	TotalCnt[15:8]

10.17 Total Count2 (TotalCnt[23:16], 0x6072 TotalCnt2)

Field name	rscu	bit #	reset	Description
TotalCnt2	rwu	7-0	8'b0	TotalCnt[23:16]

10.18 Total Count3 (TotalCnt[31:24], 0x6073 TotalCnt3)

Field name	rscu	bit #	reset	Description
TotalCnt3	rwu	7-0	8'b0	TotalCnt[31:24]

10.19 Load Total Count (Load TotalCnt, 0x6074)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	7'b0	Reserved
LoadTotalCnt	w	0	1'b0	Write an 1 to this bit will re-load the value from register 0x73-0x70's TotalCnt[31:0] to internal counter.

10.20 Global Total Count0 (GTotalCnt[7:0], 0x6080 GTotalCnt0)

Field name	rscu	bit #	reset	Description
GTotalCnt0	rwu	7-0	8'b0	GTotalCnt[7:0]

10.21 Global Total Count1 (GTotalCnt[15:8], 0x6081 GTotalCnt1)

Field name	rscu	bit #	reset	Description
GTotalCnt1	rwu	7-0	8'b0	GTotalCnt[15:8]

10.22 Global Total Count2 (GTotalCnt[23:16], 0x6082 GTotalCnt2)

Field name	rscu	bit #	reset	Description
GTotalCnt2	rwu	7-0	8'b0	GTotalCnt[23:16]

10.23 Global Total Count3 (GTotalCnt[31:24], 0x6083 GTotalCnt3)

Field name	rscu	bit #	reset	Description
GTotalCnt3	rwu	7-0	8'b0	GTotalCnt[31:24]

11. Electrical Information:

11.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
Vcc	Power Supply	-0.3	3.6	V
Vin	Input Voltage	-0.3	Vcc+0.3	V
Vout	Output Voltage	-0.3	Vcc+0.3	V
Tstg	Storage Temperature	-55	150	°C

11.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input Voltage	0	-	Vcc	V
Tj	Commercial Junction Operating Temperature	0	25	115	°C

11.3 General DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
Iil	Input Leakage Current	-1		1	μA
Ioz	Tristate Leakage Current	-1		1	μA
Cin	Input Capacitance		2.8		pF

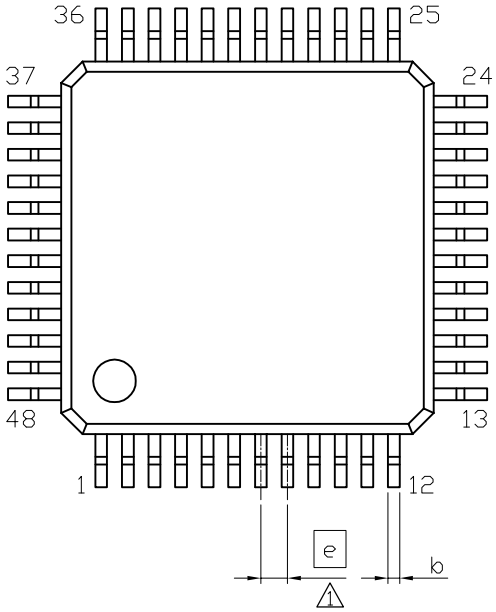
Cout	Output Capacitance	2.7		4.9	pF
Cbid	Bi-directional Buffer Capacitance	2.7		4.9	pF

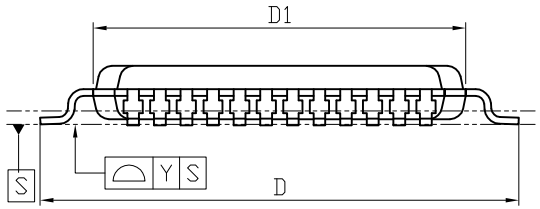
11.4 DC Electrical Characteristics for 3.3V Operation

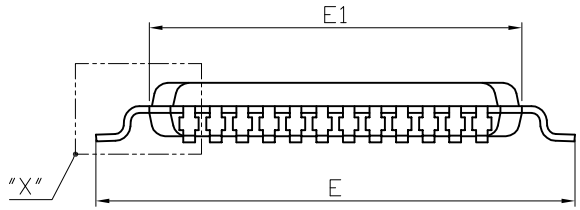
(Under Vcc=3.0-3.6V, Tj=0-115C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input Low Voltage	CMOS	-0.3		0.8	V
Vih	Input High Voltage	CMOS	2.0		5.5	V
Vol	Output Low Voltage	Ioh-2-24mA			0.4	V
Voh	Output High Voltage	Ioh=2-24mA	2.4			V
Ri	Input Pullup/pulldown Resistance	Vil=0/Vih=Vcc		75		kΩ
Icc	Operating Supply Current	Vcc=3.3V			150	mA

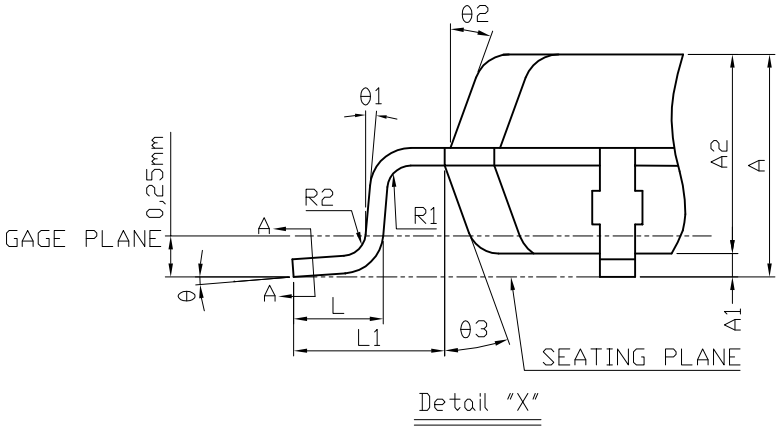
12. Packaging Specification



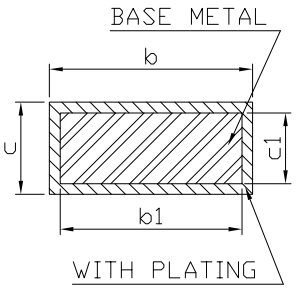




SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
⚠1 e	0.35	0.50	0.65	14	20	26
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0,075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°



Detail "X"



SECTION A-A

NOTE:
1.REFER TO JEDEC MS-026/BBC
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.
⚠1 5.Remark: Modify [e] .

				PKG. CODE	DRAWING NUMBER	REV.
						4
SIZE	A3	BY	DATE	TITLE	LQFP48 (7x7mm) PACKAGE OUTLINE Footprint 2.0mm	
DRAWN			2005.09.06			
DESIGNED						
CHECKED				SCALE	10 : 1	PROJ.
APPROVED				SHEET	1 OF 1	