# INIC-1605
# USB to SATA Bridge
# Specification

**Version 1.01**
**August 14, 2006**
**Initio Corporation**

Change History:

8-14-06 – Minor feature edits
8-4-06 - Release

## Table of Contents

# 1. Introduction:

The INIC-1605 provides an advanced solution to connect SATA devices to USB with integrated CPU and embedded SRAM. To provide high performance and cost effective solution, the INIC-1605 integrates USB-PHY Mass Storage Class Bulk-Only USB function, SATA link/PHY core and microprocessor into a single ASIC. The INIC-1605 provides the data transfer rate of up to 60 MB/sec connecting to a SATA interface.

## 1.1 Feature Summary

- Integrates USB2.0 PHY IP core.
- Data transfer rate of up to 60 MB/sec on USB side.
- Integrated internal Turbo 8051 uP with 16KB embedded SRAM.
- Program Flash In-Line (Firmware download mechanism, USB direct for MFG Test, write .bta file.
- Local Bus Interface to Serial Peripheral Interface (SPI) Flash Only.
- Support HID.
- Up to 9 GPIO pins.
- The option of using only one external crystal.
- Provide software utilities for downloading the upgraded firmware code under USB.
- Supports SATA (bridged SATA) Hard Disk drives, CD-RW devices, DVDs, Removable media devices
- USB 1.1 and USB 2.0 compliant.
- USB Mass Storage Class Bulk-Only Transport Specification Compliant.
- SATA specification 1.0, SATA II and eSATA Compliant (Hot Plug is supported).
- Supports SATA NCQ.
- Supports 3Gbps SATA HDD connection to internal 1.5Gbps SATA II Phy.
- Support ATA/ATAPI device DMA and PIO mode.
- 4k bytes of data buffer for data transfer.
- One SATA channel support.
- On-Chip 3.3V to 1.8V regulator.
- 64 pin LQFP

## 1.2 Firmware/Software Support

- USB Mass Storage Class Bulk-Only Transport support
- Provide software utilities for downloading the upgraded firmware code

## 1.3 Devices Support

- Hard disk drives
- CD-RW devices
- DVDs
- Removable media devices

## 2. INIC-1605 Block Diagram:

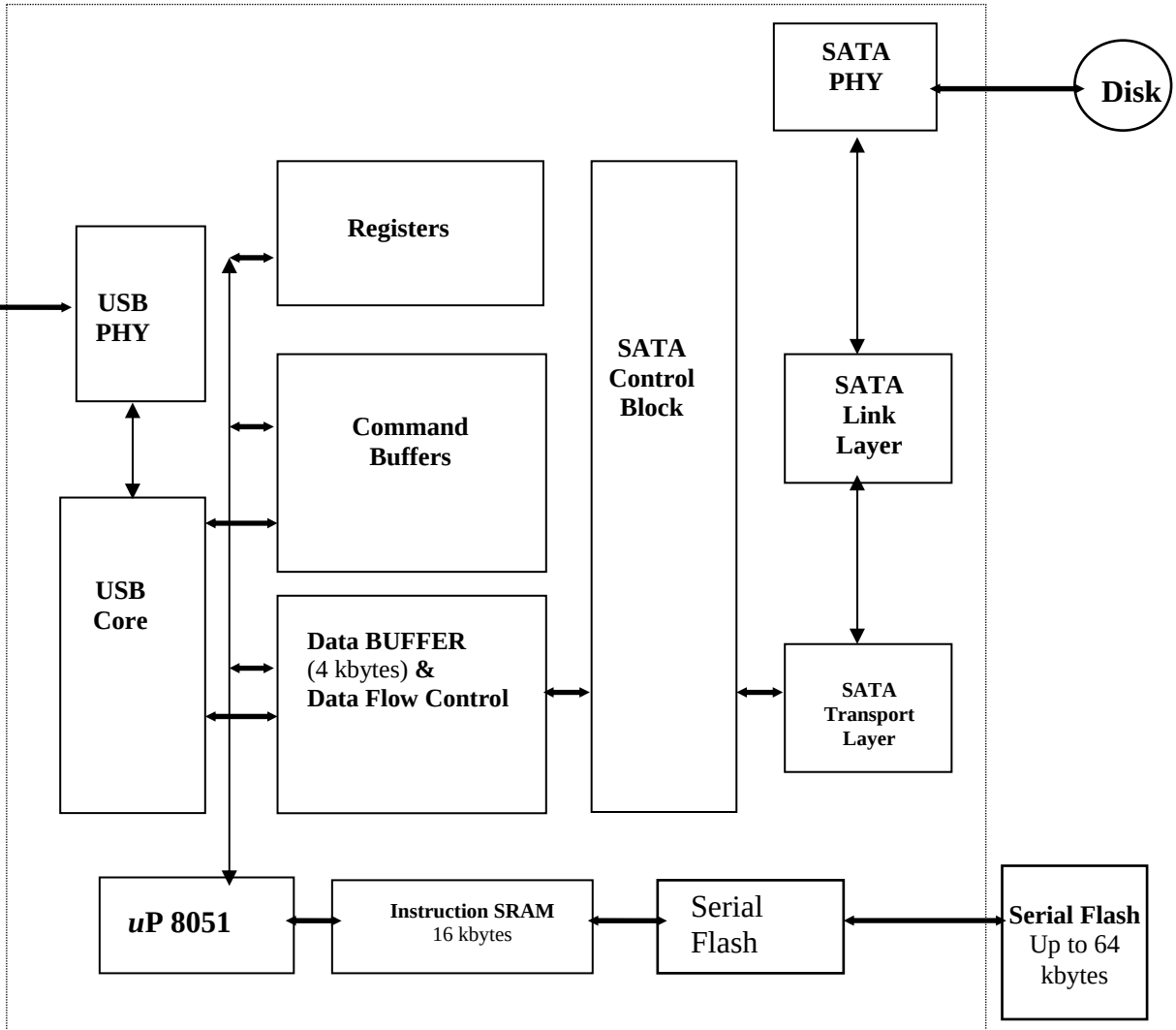
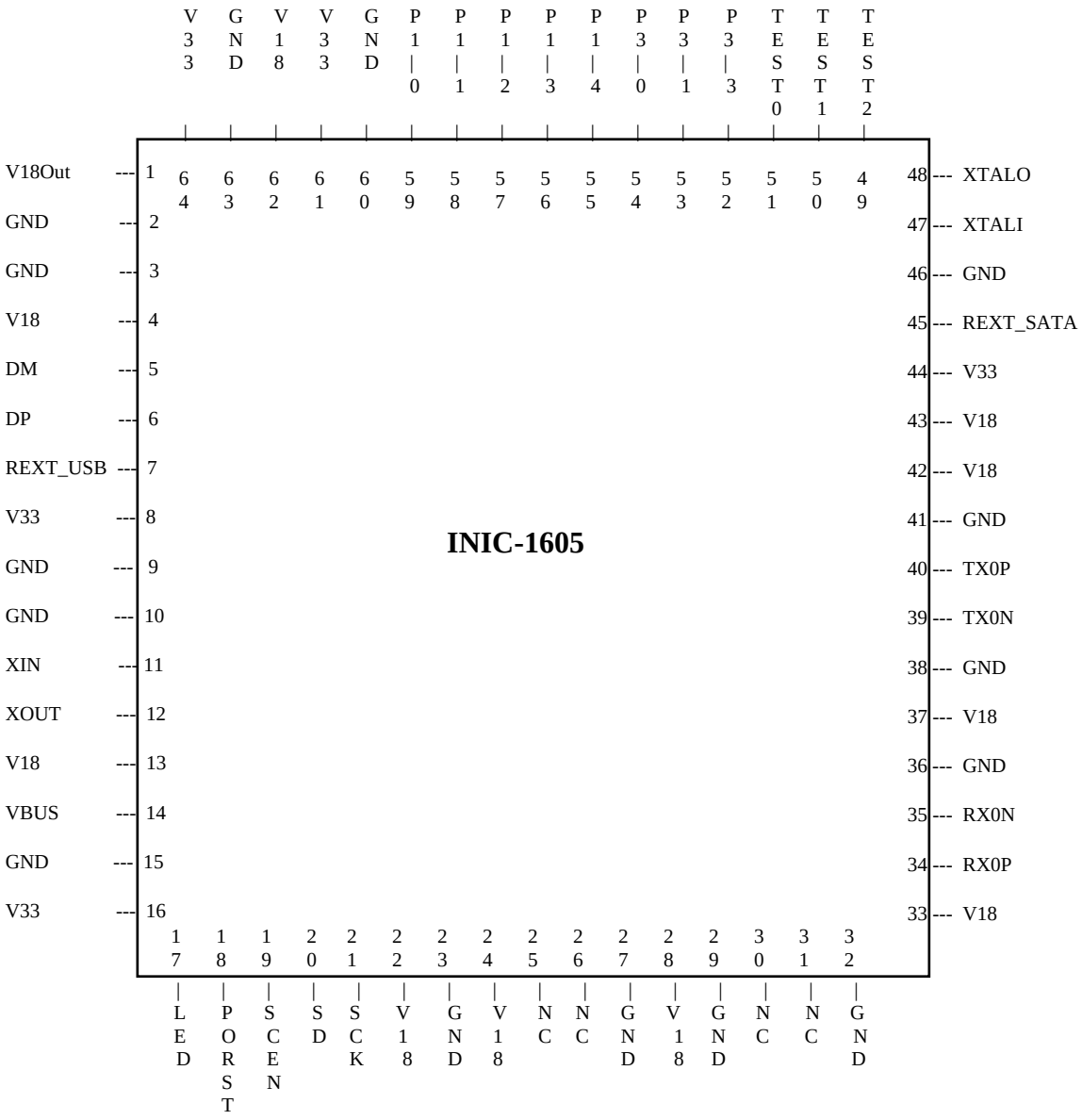



**Figure1: USB to SATA Bridge Block Diagram**

## 3. Pin-Out Diagram:



# 4. Pin Signal Description: (64-pin package)

## 4.1 USB Interface (Analog pins except VBUS)

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| DP | 6 | I/O | USB high /full speed buffer (D+) | High/Full speed D+ signal |
| DM | 5 | I/O | USB high/full speed buffer (D-) | High/Full speed D- signal |
| REXT_USB | 7 | A | Power | PLL voltage reference. Current source for 330 ohm(1%) resistor connected to AVSS |
| VBUS | 14 | I | No internal pullup/down | Active HIGH. Indicates that VBUS is present. |
| XIN | 11 | I | A | Crystal oscillator input (12MHz) |
| XOUT | 12 | O | A | Crystal oscillator output (12MHz) |

## 4.2 SATA Interface (Analog pins)

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| TX0P (SATA Device) | 40 | O | SATA | Channel0 Differential Transmit positive signal line |
| TX0N (SATA Device) | 39 | O | SATA | Channel0 Differential Transmit negative signal line |
| RX0P (SATA Device) | 34 | I | SATA | Channel0 Differential Receive positive signal line |
| RX0N (SATA Device) | 35 | I | SATA | Channel0 Differential Receive negative signal line |
| XTALO | 48 | O | | Crystal oscillator output |
| REXT_SATA | 45 | I | | External Reference Resister (6.19 K ohm) |

## 4.3 System Interface

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| PORST# | 18 | I | Internal pullup 80Kohm | Power On Reset. |

## 4.4 Miscellaneous Interface

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| TestMode[2:0] | 49,50,51 | I | Internal pulldown 80Kohm | Test Mode Select<br>000: Normal<br>001: Reserved<br>010: testMux (internal testing)<br>011: USB PHY test(internal testing)<br>100: SATA PHY test(internal testing)<br>101: Scan Test(ATPG tests)<br>110: Mbist Test (internal testing)<br>111: POR_from_pin_Test(internal testing) |

## 4.5 Serial Flash Interface

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| SCEN/<br>P1.7In/<br>GPIO3 | 19 | I/O | Internal pull down 80Kohm | 1. Serial Flash Chip Enable.<br>2. This pin also connects to uP8051.P1.7In port.<br>3. This pin can also be configured as GPIO3.<br>4. Strap for USBPLL_freq_sel.<br>(0* : Use crystal input 12MHz XIN for USB PLL.) (*default)<br>(1 : Use internal clock source for USB PLL.) |
| SD/<br>P1.6In/<br>GPIO2 | 20 | I/O | Internal pull down 80Kohm | 1. Serial Flash data input/output.<br>2. This pin also connects to uP8051.P1.6In port.<br>3. This pin can also be configured as GPIO2. |
| SCK/<br>P1.5In/<br>GPIO1 | 21 | I/O | Internal pullup 80Kohm | 1. Serial Flash clock.<br>2. This pin also connects to uP8051.P1.5In port.<br>3. This pin can also be configured as GPIO1 |

## 4.6 MVRAM/GPIO Interface

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| LED | 17 | I/O | Internal pullup 80Kohm | LED: SATA Activity indicator. |
| P3.3/<br>INT1# | 52 | I/O | No internal pullup/down | uP8051 I/O port 3.3, can be used as GPIO |
| P3.1/<br>UART_TxD | 53 | I/O | Internal pullup 80Kohm | uP8051 I/O port 3.1, can be used as GPIOs |
| P3.0/<br>UART_RxD | 54 | I/O | Internal pullup 80Kohm | uP8051 I/O port 3.0, can be used as GPIOs |
| P1.4 | 55 | I/O | Internal pullup 80Kohm | uP8051 I/O port 1.4, can be used as GPIOs |
| P1.3 | 56 | I/O | Internal pullup 80Kohm | uP8051 I/O port 1.3, can be used as GPIOs |
| P1.2/<br>refclkSel_0 | 57 | I/O | Internal pullup 80Kohm | uP8051 I/O port 1.2, can be used as output GPIO<br>1. The pullup/pulldown of pin58, pin57 will select the frequency of refclk:<br>pin58 pin57 refclk<br>pullup pulldown 100MHz<br>pullup pullup 25MHz*<br>pulldown pulldown 150MHz<br>pulldown pullup 75MHz<br><br>*: default selection is 25MHz |
| P1.1/<br>refclkSel_1 | 58 | I/O | Internal pull up 80Kohm | Note 1: P1.1 is used as strap pin only. |
| P1.0 | 59 | I/O | Internal pullup 80Kohm | uP8051 I/O port 1.0, can be used as GPIOs |

### 4.7 Power Regulator pins

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| REG_VCC3 | 64 | I | | Total 1 pin |
| REG_GND | 2 | I | | Total 1 pin |
| REG_V18Out | 1 | O | | Total 1 pin |

### 4.8 Power/GND

| Signal Name | Pin Number | I/O | Driver Type | Description |
|---|---|---|---|---|
| VCC3 | 16,61 | | | 2 pins (Digital 3.3V) |
| VCC18 | 22,62 | | | 2 pins (Digital 1.8V) |
| GND | 15,23,60,63 | | | 4 pins |
| USB_VCC3A | 8 | | | 1 pin:Analog 3.3V (VD33P) |
| USB_GNDA | 9 | | | 1 pin:Analog GND (VS33P) |
| USB_VCC18A | 13 | | | 1 pin:Analog 1.8V (VDDA) for USB PLL |
| USB_GND18A | 10 | | | 1 pin:Analog GND (VSSA) for USB PLL |
| USB_VCC18 | 4 | | | 1 pin:Digital 1.8V (VDDU) |
| USB_GND18 | 3 | | | 1 pin:Digital GND (VSSU) |
| SATA_VDDA | 24,28,33,37 | | | 4 pins (Analog 1.8V) |
| SATA_VDDP | 42,43 | | | 2 pins (SATA PLL 1.8V) |
| SATA_VDDO | 44 | | | 1 pin (Xtal PWR 3.3V) |
| SATA_GNDA | 27,29,32,36, 38,41,46 | | | 7 pins (Analog GND) |

## 5. Register Address Mapping:

### 5.1 General Registers

| Address | Read Value | Write Value |
|---|---|---|
| 40A3h | BufferRst | BufferRst |
| 40A6h | TestCtl | TestCtl |
| 40ACh | LED_spd | LED_spd |
| 40ADh | MiscEn | MISCEn |
| 40AFh | MiscCtl | MiscCtl |
| 40B1h | DmaFlush | DmaFlush |
| 40B2h | USB Channel Set | USB Channel Set |
| 40B3h | USB Channel Clear | USB Channel Clear |
| 40B4h | Dir/D2BEn | Dir/D2BEn |
| 40B5h | Run | Run |
| 40B6h | Sata Config | Sata Config |
| 40B7h | Sata Reset | Sata Reset |
| 40B8h | SataStatus | NA |
| 40BDh | SPI_Status | SPI-Ctrl |
| 40BEh | SPI_RdData | SPI-WrData |
| 40BFh | SPI_Command | SPI-Command |
| 40DDh | SPI_ADR[7:0] | SPI_ADR[7:0] |
| 40DEh | SPI_ADR[15:8] | SPI_ADR[15:8] |
| 40DFh | SPI_ADR[31:16] | SPI_ADR[31:16] |

| | | |
|---|---|---|
| 40F0h | UsbINT_En | UsbINT_En |
| 40F2h | sataINT_En | sataINT_En |
| 40F4h | GPIO_P_INT_En | GPIO_P_INT_En |
| 40F5h | GPIO_N_INT_En | GPIO_N_INT_En |
| 40F7h | Buffer Clear | Buffer Clear |
| 40F8h | GPIOEn | GPIOEn |
| 40F9h | GPIODataIn | GPIODataOut |
| 40FAh | GPIOoutEn | GPIOoutEn |
| 40FBh | USB Clear | USB Clear |

## 5.2 Buffers

| Address | Read Value | Write Value |
|---|---|---|
| 4100h-413Fh (64 bytes) | Control_in Buffer | Can't be written by CPU |
| 4140h-417Fh (64 bytes) | CBW_in Buffer | CBW_in Buffer |
| 41C0h-41FFh (64 bytes) | Control_out Buffer | Control_out Buffer |
| 4240h-427Fh (64 bytes) | CSW_out Buffer | CSW_out Buffer |
| 4280h-423Fh (64 bytes) | HID_out Buffer | HID_out Buffer |

## 5.3 USB Control Registers

| Address | Read Value | Write Value |
|---|---|---|
| 4500h-450Fh | USB Control | USB Control |

## 5.4 SATA Control Registers

| Address | Read Value | Write Value |
|---|---|---|
| 4800h | Reserved | Reserved |
| 4801h | ATA Error Shadow | ATA Error Shadow |
| 4802h | ATA Status Shadow | ATA Status Shadow |
| 4803h | Control Flag | Control Flag |
| 4804h-480Fh | Reserved | Reserved |
| 4810h | ATA Feature Shadow | ATA Feature Shadow |
| 4811h | ATA Extended Feature Shadow | ATA Extended Feature Shadow |
| 4812h | ATA Device/Head Shadow | ATA Device/Head Shadow |
| 4813h | Reserved | Reserved |
| 4814h | ATA Sector Count Shadow | ATA Sector Count Shadow |
| 4815h | ATA Extended Sector Count Shadow | ATA Extended Sector Count Shadow |
| 4816h | ATA Sector Number Shadow | ATA Sector Number Shadow |
| 4817h | ATA Extended Sector Number Shadow | ATA Extended Sector Number Shadow |
| 4818h | ATA Cylinder Low Shadow | ATA Cylinder Low Shadow |
| 4819h | ATA Extended Cylinder Low Shadow | ATA Extended Cylinder Low Shadow |
| 481Ah | ATA Cylinder High Shadow | ATA Cylinder High Shadow |
| 481Bh | ATA Extended Cylinder High Shadow | ATA Extended Cylinder High Shadow |
| 481Ch | ATA Command Shadow | ATA Command Shadow |
| 481Dh | ATA Control Shadow | ATA Control Shadow |
| 4820h | SATA PHY Control [7:0] | SATA PHY Control [7:0] |
| 4821h | SATA PHY Control [15:8] | SATA PHY Control [15:8] |
| 4822h | SATA PHY Status [7:0] | SATA PHY Status [7:0] |

| | | |
|---|---|---|
| 4823h | SATA PHY Status [15:8] | SATA PHY Status [15:8] |
| 4830h-4833h | SATA Status | SATA Status |
| 4834h-4837h | SATA Error | SATA Error |
| 4838h-483Bh | SATA Control | SATA Control |
| 483Ch-483Fh | SATA Active | SATA Active |

## 5.5 Data BUFFER

| Address | Read Value | Write Value |
|---|---|---|
| 5000h-5FFFh | Data BUFFER | Data BUFFER |

## 5.6 USB Registers

| Address | Read Value | Write Value |
|---|---|---|
| 6020h | Dev_Status | Dev_Status |
| 6021h | Funct_Adr | Funct_Adr |
| 6022h | Test_mode | Test_mode |
| 6025h | EpTxLength[7:0] | EpTxLength[7:0] |
| 6026h | EpTxLength[15:8] | EpTxLength[15:8] |
| 6030h | EP0_Status | EP0_ Control (Set) |
| 6031h | EP0_Status | EP0_ Control (Clear) |
| 6032h | EP0_Status2 | EP0_ Control 2(Set) |
| 6033h | EP0_Status2 | EP0_ Control 2(Clear) |
| 6034h | EP0TxLength | EP0TxLength |
| 6038-603F | Hdr0-7 | - |
| 6040h | EP1_Status | EP1_ Control (Set) |
| 6041h | EP1_Status | EP1_ Control (Clear) |
| 6050h | EP2_Status | EP2_ Control (Set) |
| 6051h | EP2_Status | EP2_ Control (Clear) |
| 6052h | Usb_rxLength[7:0] | - |
| 6060h | EP3_Status | EP3_ Control (Set) |
| 6061h | EP3_Status | EP3_ Control (Clear) |
| 6070h | TotalCnt0 | TotalCnt0 |
| 6071h | TotalCnt1 | TotalCnt1 |
| 6072h | TotalCnt2 | TotalCnt2 |
| 6073h | TotalCnt3 | TotalCnt3 |
| 6074h | - | LoadTotalCnt |
| 6080h | GTotalCnt0 | GTotalCnt0 |
| 6081h | GTotalCnt1 | GTotalCnt1 |
| 6082h | GTotalCnt2 | GTotalCnt2 |
| 6083h | GTotalCnt3 | GTotalCnt3 |

## 5.7 Data Space Mapping

| Mapping Address | Type | Access Type | Mapping Block |
|---|---|---|---|
| 0000h-3FFFh | Data | Read/Write | Internal SRAM (16KB) |
| 4000h-47FFh | Data | Read/Write | Internal Register/Buffers |
| 4800h-48FFh | Data | Read/Write | SATA Registers |
| 5000h-5FFFh | Data | Read/Write | Data BUFFER (4KB) |
| 6000h-60FFh | Data | Read/Write | USB Registers |

## 5.8 Code Space: Internal SRAM:

| Address | Read Value | Write Value |
|---|---|---|
| 0-3FFFh | Firmware Code (16K Bytes) (Instruction Fetch) | N/A |

# 6. Programming Guide:

## 6.1 USB direct access 8051's code/data space (Byte mode only)

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1605 here.
2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.
3. Host may send READ_HOLD_CPU packet through control channel to read back HOLD_CPU bit.
4. Host may send FLASH_WRITE/FLASH_READ/DATA_WRITE/DATA_READ packet through control channel to WRITE/READ flash or data space.

## 6.2 Hardware Program/Download procedure (Byte mode only)

INIC-1605 provides the mechanism for USB host to access the flash chip directly.

Host may program and read **serial flash** memory through default endpoint. Flash write setup packet format is,

| offset | field | size | value | Description |
|---|---|---|---|---|
| 0 | bmReqType | 1 | 0x40 | Vendor write |
| 1 | bReq | 1 | | Flash write<br>[7]: 0—Flash memory<br>[6]: 1—addr valid<br>[5]: 1—data valid<br>[4:0]: 5'h01—Flash Write |
| 2 | wValue | 2 | Addr[7:0] | Address to be written |
| 3 | | | Addr[15:0] | |
| 4 | wIndex | 2 | Data[7:0] | |
| 5 | | | opCode | Flash data |
| 6 | wLength | 2 | 0x00 | |
| 7 | | | 0x00 | |

Flash Read setup packet format is,

| offset | field | size | value | data | Description |
|---|---|---|---|---|---|
| 0 | bmReqType | 1 | 0xc0 | Data from Flash | Vendor read |
| 1 | bReq | 1 | | | Flash read<br>[7]: 0—Flash memory<br>[6]: 1—addr valid<br>[5]: 1—data valid<br>[4:0]: 5'h02—Flash Read |
| 2 | wValue | 2 | Addr[7:0] | | Address to be written |
| 3 | | | Addr[15:0] | | |
| 4 | wIndex | 2 | 0x00 | | |
| 5 | | | opCode | | Don't care |

| | | | | | |
|---|---|---|---|---|---|
| 6 | wLength | 2 | 0x01 | | |
| 7 | | | 0x00 | | |

READ_CHIP_ID setup packet format is,

| offset | field | size | value | data | Description |
|---|---|---|---|---|---|
| 0 | bmReqType | 1 | 0xc0 | Chip-ID 0x10, 0x16, 0xc9, 0x25 | Vendor read |
| 1 | bReq | 1 | 0x03 | | |
| 2 | wValue | 2 | 0x00 | | |
| 3 | | | 0x00 | | |
| 4 | wIndex | 2 | 0x00 | | Don't care |
| 5 | | | 0x00 | | Don't care |
| 6 | wLength | 2 | 0x04 | | |
| 7 | | | 0x00 | | |

HOLD_CPU setup packet format is,

| offset | field | size | value | Description |
|---|---|---|---|---|
| 0 | bmReqType | 1 | 0x40 | Vendor write |
| 1 | bReq | 1 | 0x04 | HOLD_CPU |
| 2 | wValue | 2 | 0x00 | Don't care |
| 3 | | | 0x00 | |
| 4 | wIndex | 2 | 0x00 | Don't care |
| 5 | | | 0x00 | Don't care |
| 6 | wLength | 2 | 0x00 | Don't care |
| 7 | | | 0x00 | Don't care |

## 6.3 SPI Serial Flash Programming Guide:

A1. Serial Peripheral Interface (SPI) Serial Flash Operation:

A1.1 Hardware bootload:

1. After power on, hardware will automatically load 4 K bytes codes from SPI Serial Flash (location 0000h – 0fffh) in internal memory(duplicates into two 4 K bytes area: location 0000-0fffh and 3000-3fffh).
2. After the hardware 4 K bytes bootload, firmware may execute this 4 K byte codes from memory location 0000h, a copy additional 12 K bytes code from Serial Flash into internal memory. Please see the example in A1.2 for this copy sequences:

A1.2 Example for firmware to read codes from Serial Flash location 24'h00A000 and copy it into internal memory location 16'h0B00:

1. CPU writes Register_40BF with 0x03 (Command Read) /* to prepare the command code */
2. CPU writes Register_40DF with 0x00 (SPI_ADR[23:16]) /* to prepare the SPI_ADDR */
3. CPU writes Register_40DE with 0xA0 (SPI_ADR[15:8])
4. CPU writes Register_40DD with 0x00 (SPI_ADR[7:0])
5. CPU writes Register_40BD with 0xE0 (SPI_Ctrl) /* to send out this Read command to Serial Flash */
6. CPU reads Register_40BE to trigger the read action.
7. CPU reads Register_40BD, check if bit 0 becomes 1'b1. If yes, go to step 8, otherwise repeat step 7
8. CPU reads Register_40BE to get the content, and write it to internal memory location 16'0B00.

A1.3 Example for firmware to do Sector_Erase to Serial Flash location 24'h008xxx :( Sector 8)

1. CPU writes Register_40BF with 0x06 (Command WREN) /* to prepare the command code */
2. CPU writes Register_40BD with 0x80 (SPI_Ctrl) /* to send out this WREN command to Serial Flash */
3. CPU writes Register_40BF with 0x20 /* Command Sector_Erase */
4. CPU writes Register_40DF with 0x00 (SPI_ADR[23:16])
5. CPU writes Register_40DE with 0x80 (SPI_ADR[15:8]) /* Sector 8 */
6. CPU writes Register_40DD with 0x00 (SPI_ADR[7:0])
7. CPU writes Register_40BE with dummy data (SPI_Data)
8. CPU writes Register_40BD with 0xC0 (SPI_Ctrl) /* to send out this Sector_Erase command to Serial Flash */
9. CPU writes Register_40BF with 0x05 (Command RDSR)
10. CPU writes Register_40BD with 0xA0 (SPI_Ctrl) /* to send out this RDSR command to Serial Flash */
11. CPU reads Register_40BD, check if bit 0 becomes 1'b1. If yes, go to step 12, otherwise repeat step 11
12. CPU reads Register_40BE to get the status, check if bit 0 becomes 1'b0. If yes, go to step 13, otherwise go to step 9
13. CPU writes Register_40BD with 0x00 (SPI_Ctrl) /* turn off this control */

A1.4 Example for firmware to write data to Serial Flash location 24'h008123:

1. CPU writes Register_40BF with 0x06 (Command WREN) /* to prepare the command code */
2. CPU writes Register_40BD with 0x80 (SPI_Ctrl) /* to send out this WREN command to Serial Flash */
3. CPU writes Register_40BF with 0x02 (Command ByteWr)
4. CPU writes Register_40DF with 0x00 (SPI_ADR[23:16])
5. CPU writes Register_40DE with 0x81 (SPI_ADR[15:8])
6. CPU writes Register_40DD with 0x23 (SPI_ADR[7:0])
7. CPU writes Register_40BE with Data (SPI_Data)
8. CPU writes Register_40BD with 0xE0 (SPI_Ctrl) /* to send out this ByteWr command to Serial Flash */
9. CPU reads Register_40BD, check if bit 1 becomes 1'b1. If yes, go to step 10, otherwise repeat step 9
10. CPU writes Register_40BD with 0x00 (SPI_Ctrl) /* turn off this control */

# 7. Register Descriptions:

## 7.1 BUFFER Reset Register (0x40A3)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-5 | 3'b0 | Reserved. |
| Buffer1Rst | rw | 4 | 1'b0 | DMA BUFFER 1 Reset. This bit is used to reset DMA BUFFER 1. This bit is self-cleared by hardware after set. |
| Reserved | r | 3-1 | 3'b0 | Reserved. |
| Buffer0Rst | rw | 0 | 1'b0 | DMA BUFFER 0 Reset. This bit is used to reset DMA BUFFER 0. This bit is self-cleared by hardware after set. |

## 7.2 Test Control Register (0x40A6)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-6 | 2'b0 | Reserved. |
| RevID | r | 5-4 | 2'h0 | Revision ID. These 2 bits are read only. |
| TestMuxSel | rw | 3-0 | 4'h0 | Test mux output select. These 4 bits select specific internal signals to be routed to device's outputs during test mode. (internal testing purpose) |

### 7.2.1 LED_spd register (0x40AC)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-5 | 3'b0 | Reserved |
| Usb_WakeUpEn | rw | 4 | 1'b0 | 1: Enable external interrupt wakeup USB when device is now in suspend state. |

| | | | | |
|---|---|---|---|---|
| LED_spd [3 : 0] | rw | 3-0 | 4'h0 | Define LED blink speed : 0000 : 1/32 sec. per blink<br>0001 : 2/32 sec. per blink<br>Up to ~ ~ 1111 : 16/32 sec. per blink |

### 7.2.2 MiscEn register (0x40AD)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-6 | 2'b00 | Reserved |
| Reserved | r | 5 | 1'b0 | Reserved |
| TL_Wakeup | rw | 4 | 1'b0 | Control bit for SATA block |
| TL_Slumber | rw | 3 | 1'b0 | Control bit for SATA block |
| TL_Partial | rw | 2 | 1'b0 | Control bit for SATA block |
| Sata_busy_sel | rw | 1 | 1'b0 | 0 : Select sata_busy as sata device activity detection<br>1 : Select (sata_busy or sata_drq) as sata device activity detection |
| Reserved | r | 0 | 1'b0 | Reserved |

## 7.3 MiscCtl register (0x40AF): This 8-registers is in lclk domain (37.5 MHz)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Sim_mode | rw | 7 | 1'b0 | Internal testing. Do Not set to 1. |
| Reserved | r | 6 | | Reserved |
| PHYCLK_Ctl | rw | 5 | 1'b0 | Firmware set/clr this bit. If set, PHY clock is free run. If clr, PHY clock will stop when device goes to suspend mode. |
| Usb_Enumeration | rw | 4 | 1'b1 | 1: Enable USB Enumeration. 0: Disable USB Enumeration. |
| HW_Rst_Event | rw | 3 | 1'b1 | This bit is set by hardware reset. Software reset has no effect on this bit. Firmware can clear this bit by writing a 0 to it. |
| HidEn | rw | 2 | 1'b0 | 1 : Endpoint defined as: 8(IN), 2(OUT), 1(INT)<br>0 : Endpoint defined as: 1(IN), 2(OUT), 3(INT) |
| NewMode | rw | 1 | 1'b0 | 1 : 1605 report residue same as totalCnt minus USB Txed or Rxed<br>0 : 1605 report residue same as totalCnt minus ATA Txed or Rxed |
| Reserved | r | 0 | 1'b0 | Reserved |

## 7.4 SoftRst register (0x40B0)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-1 | 7'b0 | Reserved. |
| SoftRst | w | 0 | 1'b0 | 1: Software reset (setting this bit will reset the data buffer related logic) |

## 7.5 DMA Flush register (0x40B1)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-1 | 7'b0 | Reserved |
| Flush/Abort | rw | 0 | 1'b0 | When DMA BUFFER is overrun, this bit is used by firmware to flush data out for outgoing data or abort the DMA operation for incoming data. This bit is self-cleared by hardware. |

## 7.6 USB Channel Set/Clear register (0x40B2 Set) (0x40B3 Clear)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7 | 7'b0 | Reserved |
| CmdTx4Run | rwu | 6 | 1'b0 | The Set register is set by software and cleared by hardware when transfer |

| | | | | |
|---|---|---|---|---|
| (for HID_out) | | | | is completed.<br>When the Clear register is set by software, the corresponding channel is cleared. |
| CmdTx3Run<br>(for CSW_out) | rwu | 5 | 1'b0 | The Set register is set by software and cleared by hardware when transfer is completed.<br>When the Clear register is set by software, the corresponding channel is cleared. |
| Reserved | r | 4 | 1'b0 | Reserved |
| CmdTx1Run<br>(for Control_out) | rwu | 3 | 1'b0 | The Set register is set by software and cleared by hardware when transfer is completed.<br>When the Clear register is set by software, the corresponding channel is cleared. |
| Reserved | r | 2-0 | 3'b0 | Reserved |

## 7.7 Dir/D2BEn register (0x40B4)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Dir | rw | 7 | 1'b0 | Indicates the direction of the data transfer:<br>0: Data write into SATA device.<br>1: Data output from SATA device.<br>**Proper Dir bit must be programmed before writing ATA command** |
| D2BEn | rw | 6 | 1'b0 | Data to Buffer Mode Enable. The two SATA channels can be configured to transfer data to and from the buffer memory without a host connection. |
| Reserved | r | 5-0 | 6'b0 | Reserved |

## 7.8 Run register (0x40B5)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| PhaseError | rws | 7 | 1'b0 | Phase Error status. Set by hardware. |
| Reserved | r | 6-1 | 6'b0 | Reserved |
| Run | rw | 0 | 1'b0 | Write 1: Start the data transfer; the hardware will clear this bit when the transfer is completed.<br>Firmware also can write 0 to clear this bit.<br>D2BEn (Register 0x40B4 bit 6) and Run (Register 0x40B5 bit 0) work together to start different data transfer:<br>D2BEn Run<br>0 0 : Idle<br>0 1 : Start transfer between USB and SATA device according to the DIR bit (Register 0x40B4 bit 7).<br>1 0 : Idle<br>1 1 : Start transfer between DMA buffer and SATA device according to the DIR bit (Register 0x40B4 bit 7) |

## 7.9 SATA Config register (0x40B6)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| HwFlushEn | rw | 7 | 1'b1 | When set to 1: automatic hardware flush is enabled. |
| PhaseErrEn | rw | 6 | 1'b1 | When set to 1: An PhaseErr event will report PhaseErr to |

| | | | | |
|---|---|---|---|---|
| | | | | register 0x40B5 bit 7. |
| LED_Idle_HIGH | rw | 5 | 1'b0 | 0: SATA idle will drive LED pin LOW<br>1: SATA idle will drive LED pin HIGH |
| LED_busy_sel | rw | 4 | 1'b0 | 0 : SATA busy will blink LED<br>1 : SATA busy will drive LED ON |
| Reserved | r | 3-0 | 4'b0 | Reserved |

## 7.10 SATA Reset register (0x40B7)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| ATAPhyRst | rw | 7 | 1'b0 | SATA channels Hard reset to Phy layer, Auto-Clear by hardware |
| Reserved | r | 6-5 | 2'b0 | Reserved. |
| ATAUppRst | rw | 4 | 1'b0 | SATA Channel 0 reset to Link/Transport/Application layer |
| Reserved | r | 3-1 | 3'b0 | Reserved. |
| AtaCh0INT | r | 0 | 1'b0 | SATA Channel 0 interrupt signal. |

## 7.11 SPI Ctrl/Status Register (0x40BD) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| StartCMD | w | 7 | 1'b0 | 1: CPU write 1 to start the serial flash's command phase |
| SPI_AdrValid | w | 6 | 1'b0 | 1: Validate the Address field in the SPI command |
| SPI_DataValid | w | 5 | 1'b0 | 1: Validate the Data field in the SPI command |
| StartWRSR | w | 4 | 1'b0 | 1: CPU write 1 to start the serial flash's Write_Status_Register action |
| reserved | r | 3-2 | 2'b0 | |
| SPI_WrDone | r | 1 | 1'b0 | Read only: CPU has send out the serial write command to serial flash.<br>CPU may start sending out the read_status_command (RDSR) to serial flash to check the BUSY bit. When BUSY bit is 0, it means serial flash has finished the write operation. |
| SPI_RdDataRdy | r | 0 | 1'b0 | Read only: CPU has send out the serial read command to serial flash. |

## 7.12 SPI_Data Register (0x40BE) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| SPI_Data | rw | 7-0 | 8'h0 | This is the data port for CPU to access aerial flash<br><br>A: To Write to serial flash:<br>CPU Writes to this port: CPU writes a 8-bit data to serial flash.<br><br>B: To Read from serial flash:<br>CPU reads this port:<br>CPU does 1st Read: CPU activates the read action to fetch data from serial flash.<br>CPU poll SPI_RdDataRdy (register BD bit 0) until it is 1<br>CPU does 2nd Read: to actually get the data. |

### 7.13 SPI_CMD Register (0x40BF) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| SPI_CMD | rw | 7-0 | 8'h0 | CPU writes the to-be executed SPI_command code in this register.<br>For example: SPI_read has a command code: 03h |

### 7.14 SPI_ADR[7:0] Register (0x40DD) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| SPI_ADR[7:0] | rw | 7-0 | 8'h0 | CPU writes the to-be executed SPI_ADR[7:0] code in this register. |

### 7.15 SPI_ADR[15:8] Register (0x40DE) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| SPI_ADR[15:8] | rw | 7-0 | 8'h0 | CPU writes the to-be executed SPI_ADR[15:8] code in this register. |

### 7.16 SPI_ADR[23:16] Register (0x40DF) (for SPI-Serial Flash only)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| SPI_ADR[23:16] | rw | 7-0 | 8'h0 | CPU writes the to-be executed SPI_ADR[23:16] code in this register. |

### 7.17 usb_INT_Enable Register (0x40F0)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Usb_busRst_INT_En | rw | 7 | 1'b0 | 1: Enable Usb_busRst to trigger sysINT.<br>To check if this INT has occurred, please read register 6030 bit 6. |
| Usb_bulkOnlyRst_INT_En | rw | 6 | 1'b0 | 1: Enable Usb_bulkOnlyRst to trigger sysINT.<br>To check if this INT has occurred, please read register 6030 bit 5. |
| Usb_Ep0Req_INT_En | rw | 5 | 1'b0 | 1: Enable Usb_ Ep0Req to trigger sysINT.<br>To check if this INT has occurred, please read register 6032 bit 0. |
| Usb_CBW_INT_En | rw | 4 | 1'b0 | 1: Enable Usb_CBW to trigger sysINT.<br>To check if this INT has occurred, please read register 6050 bit 1. |
| Usb_wakeup_INT_En | rw | 3 | 1'b0 | 1: Enable Usb_wakeup to trigger sysINT.<br>To check if this INT has occurred, please read register 6020 bit 3. (value 0 means wakeup) |
| Usb_suspendINT_En | rw | 2 | 1'b0 | 1: Enable Usb_suspend to trigger sysINT.<br>To check if this INT has occurred, please read register 6020 bit 3. (value 1 means suspend) |
| VBUS_P__INT_En | rw | 1 | 1'b0 | 1: Enable positive of VBUS to trigger sysINT.<br>To check if this INT has occurred, please read register 40AF |

| | | | | |
|---|---|---|---|---|
| | | | | bit 6. (value 1 means VBUS is high) |
| VBUS_N__INT_En | rw | 0 | 1'b0 | 1: Enable negative of VBUS to trigger sysINT.<br>To check if this INT has occurred, please read register 40AF bit 6. (value 1 means VBUS is high) |

### 7.18 SATA_INT_Enable Register (0x40F2)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-3 | 5'b0 | Reserved |
| SATA_Dev_INT_En | rw | 2 | 1'b0 | 1: Enable SATA_Dev_INT to trigger sysINT.<br>To check if this INT has occurred, please read register 40B7 bit 0. |
| SATA_PhyRdy_P_INT_En | rw | 1 | 1'b0 | 1: Enable positive of SATA_PhyRdy to trigger sysINT.<br>To check if this INT has occurred, please read register 4820 bit 0. |
| SATA_PhyRdy_N_INT_En | rw | 0 | 1'b0 | 1: Enable negitive of SATA_PhyRdy to trigger sysINT.<br>To check if this INT has occurred, please read register 4820 bit 0. |

### 7.19 SATA_BUSY_INT Register (0x40F3)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-4 | 4'b0 | Reserved |
| Reserved | r | 3-0 | 4'b0 | Reserved |

### 7.20 GPIO_P_INT_Enable Register (0x40F4)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | rw | 7-4 | 4'b0 | Reserved |
| GPIO3_P_INT_En | rw | 3 | 1'b0 | 1: Enable GPIO3 High level to trigger sysINT. |
| GPIO2_P_INT_En | rw | 2 | 1'b0 | 1: Enable GPIO2 High level to trigger sysINT. |
| GPIO1_P_INT_En | rw | 1 | 1'b0 | 1: Enable GPIO1 High level to trigger sysINT. |
| GPIO0_P_INT_En | rw | 0 | 1'b0 | 1: Enable GPIO0 High level to trigger sysINT. |

### 7.21 GPIO_N_INT_Enable Register (0x40F5)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-4 | 4'b0 | reserved |
| GPIO3_N_INT_En | rw | 3 | 1'b0 | 1: Enable GPIO3 Low level to trigger sysINT. |
| GPIO2_N_INT_En | rw | 2 | 1'b0 | 1: Enable GPIO2 Low level to trigger sysINT. |
| GPIO1_N_INT_En | rw | 1 | 1'b0 | 1: Enable GPIO1 Low level to trigger sysINT. |
| GPIO0_N_INT_En | rw | 0 | 1'b0 | 1: Enable GPIO0 Low level to trigger sysINT. |

### 7.22 Buffer Clear Register (0x40F7)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| Reserved | r | 7-1 | 4'b0 | reserved |
| Clear Buffer | rw | 0 | 1'b0 | 1: Clear data Buffer and state machine. |

### 7.23 GPIO_Enable Register (0x40F8)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | rw | 7-4 | 4'b0 | reserved |
| GPIO3_En | rw | 3 | 1'b0 | 1: use SCEN pin as GPIO3 |
| GPIO2 _En | rw | 2 | 1'b0 | 1: use SD pin as GPIO2 |
| GPIO1 _En | rw | 1 | 1'b0 | 1: use SCK pin as GPIO1 |
| GPIO0 _En | rw | 0 | 1'b0 | 1: use LED pin as GPIO0 |

### 7.24 GPIO_Data Register (0x40F9)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | rw | 7-4 | 4'b0 | reserved |
| GPIO3_Data | rw | 3 | 1'b0 | Read: Read the value of SCEN pin (i.e. GPIO3_DataIn)<br>Write: Write the value to GPIO3_DataOut (i.e. SCEN pin) |
| GPIO2 _Data | rw | 2 | 1'b0 | Read: Read the value of SD pin (i.e. GPIO2_DataIn)<br>Write: Write the value to GPIO2_DataOut (i.e. SD pin) |
| GPIO1 _Data | rw | 1 | 1'b0 | Read: Read the value of SCK pin (i.e. GPIO1_DataIn)<br>Write: Write the value to GPIO1_DataOut (i.e. SCK pin) |
| GPIO0 _Data | rw | 0 | 1'b0 | Read: Read the value of LED pin (i.e. GPIO0_DataIn)<br>Write: Write the value to GPIO0_DataOut (i.e. LED pin) |

### 7.25 GPIO_Output_Enable Register (0x40FA)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | rw | 7-4 | 4'b0 | reserved |
| GPIO3_Output_En | rw | 3 | 1'b0 | 0: Select GPIO3 to input mode<br>1: Select GPIO3 to output mode |
| GPIO2_Output_En | rw | 2 | 1'b0 | 0: Select GPIO2 to input mode<br>1: Select GPIO2 to output mode |
| GPIO1_Output_En | rw | 1 | 1'b0 | 0: Select GPIO1 to input mode<br>1: Select GPIO1 to output mode |
| GPIO0_Output_En | rw | 0 | 1'b0 | 0: Select GPIO0 to input mode<br>1: Select GPIO0 to output mode |

### 7.26 USB Clear Register (0x40FB)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-1 | 4'b0 | reserved |
| Clear USB | rw | 0 | 1'b0 | 1: Clear USB traffic problem. (When USB traffic encounter problem) |

## 7.27 Buffer Address Map

| Address | Description |
|---|---|
| 4100-413Fh | Control_in Buffer, 64 bytes |
| 4140-417Fh | CBW_in Buffer, 64 bytes |
| 41C0-41FFh | Control_out Buffer, 64 bytes |
| 4240-426Fh | CSW_out Buffer, 48 bytes |
| 4280-42AFh | HID_out Buffer, 48 bytes |

## 7.28 USB Control

| Address | Description |
|---|---|
| 4500-450Fh | USB Control |

```
450Eh bit 7-0: dataLength[7:0]
450Fh bit 7-0: dataLength[15:8]
```

# 8. SATA CHANNEL REGISTERS (0x4800-0x483F):

## 8.1 Command Parameter Blocks (CPB) Structure Definition

| 31 24 | 23 16 | 15 08 | 07 00 | |
|---|---|---|---|---|
| Control Flag | ATA Status | ATA Error | Reserved | 4800h |
| Reserved | | | | 4804h |
| Reserved | | | | 4808h |
| Reserved | | | | 480Ch |
| Reserved | ATA Device/Head | ATA Ex. Feature | ATA Feature | 4810h |
| ATA Ex. Sector Number | ATA Sector Number | ATA Ex. Sector Count | ATA Sector Count | 4814h |
| ATA Ex. Cylinder High | ATA Cylinder High | ATA Ex. Cylinder Low | ATA Cylinder Low | 4818h |
| Reserved | Reserved | ATA Control | ATA Command | 481Ch |

### 8.1.1. ATA Error Shadow
### Offset: 4801h

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Error register after status update.

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAERR | ATA Error Register content. |

### 8.1.2. ATA Status Shadow
### Offset: 4802h

When the Host programs the CPB, this byte of data is ignored. At the end of a command, the IDMA engine will update the content of this register to reflect the content of the ATA Status register after status update.

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATASTAT | ATA Status Register content. |

### 8.1.3. Control Flags
**Offset: 4803h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-04 | 5'h0 | RSVD | Reserved. |
| 03 | 0 | PPKT | Packet Command. When set, indicating the current command is an ATAPI packet command. After sending the register FIS to the device, hardware will automatically fetch the CDB from cmdReceive buffer and send to device through PIO. |
| 01-00 | 2'h0 | CDBS | Packet command CDB structure size in bytes.<br>00: 8 bytes<br>01: 12 bytes<br>10: 16 bytes<br>11: Reserved |

### 8.1.4. Reserved
**Offset: 4804-4807h**

### 8.1.5. ATA Feature Shadow
**Offset: 4810h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAFEAT | ATA Feature Register content. |

### 8.1.6. ATA Extended Feature Shadow
**Offset: 4811h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAEXFEAT | ATA Extended Feature Register content. |

### 8.1.7. ATA Device/Head Shadow
**Offset: 4812h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATADEVHD | ATA Device/Head Register content. |

### 8.1.8. ATA Sector Count Shadow
**Offset: 4814h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATASECCNT | ATA Sector Count Register content. |

### 8.1.9. ATA Extended Sector Count Shadow
**Offset: 4815h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAEXSECCNT | ATA Extended Sector Count Register content. |

### 8.1.10. ATA Sector Number Shadow
**Offset: 4816h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATASECNUM | ATA Sector Number Register content. |

### 8.1.11. ATA Extended Sector Number Shadow
**Offset: 4817h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAEXSECNUM | ATA Extended Sector Number Register content. |

### 8.1.12. ATA Cylinder Low Shadow
**Offset: 4818h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATACYLLO | ATA Cylinder Low Register content. |

### 8.1.13. ATA Extended Cylinder Low Shadow
**Offset: 4819h**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAEXCYLLO | ATA Extended Cylinder Low Register content. |

### 8.1.14. ATA Cylinder High Shadow
**Offset: 481Ah**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATACYLHI | ATA Cylinder High Register content. |

### 8.1.15. ATA Extended Cylinder High Shadow
**Offset: 481Bh**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATAEXCYLHI | ATA Extended Cylinder High Register content. |

### 8.1.16. ATA Command Shadow
**Offset: 481Ch**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATACMD | ATA Command Register content. |

### 8.1.17. ATA Control Shadow
**Offset: 481Dh**

| Bit | | Name | Definition |
|---|---|---|---|
| 07-00 | 0 | ATACTL | ATA Control Register content. |

## 8.2 SATA PHY Low Control Register (4820h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| Pw_dn_txpll | rw | 7 | 0 | Power down for TX-PLL |
| Drv_level_1 | Rw | 6 | 0 | 1: select 700mv output driver for channel 1<br>0: select 500mv output driver for channel 1 |
| Pw_dn_rxpll | Rw | 5 | 0 | Power down for RX-PLL |
| Slct5_15 | Rw | 4 | 0 | Over sampling method select<br>1: select 15 bit processing window<br>0: select 5 bit processing window |
| Bypass_calib | Rw | 3 | 1 | Disable calibration process during OOB |
| Farafleb | Rw | 2 | 0 | Place PHY in far-end analog loopback mode |
| Nearafleb | Rw | 1 | 0 | Place PHY in near-end analog loopback mode |
| Fphyrdy | Rw | 0 | 0 | Force PHY ready |

## 8.3 SATA PHY HighControl Register (4821h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| Reserved | Rw | 15-12 | 4'b0000 | |
| Pw_dn_ch0 | Rw | 11 | 0 | Power down for phy channel 0, bias circuit and calibration circuits |
| Drv_level_0 | Rw | 10 | 0 | 1: select 700mv output driver for channel 0<br>0: select 500mv output driver for channel 0 |
| Pw_dn_ch1 | Rw | 9 | 0 | Power down for channel 1 (high speed IO only) |
| Tx_pl_err_rst | Rw | 8 | 0 | TX phase error reset |

## 8.4 SATA PHY Low Status Register (4822h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| OOB_status_1 | R | 7 | 0 | |
| OOB_status_0 | R | 6 | 0 | |
| Tx_pl_err_lvl0 | R | 5 | 0 | |
| Rx_or_err_lvl0 | R | 4 | 0 | |
| Squelch | R | 3 | 0 | |
| Squelch_err | R | 2 | 0 | |
| Slumber_out | R | 1 | 0 | |
| Partial_out | R | 0 | 0 | |

## 8.5 SATA PHY High Status Register (4823h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| PhyStatus[15:10] | rw | 15-10 | 6'h0 | PHY Status[15:10] |
| OOB_status_3 | R | 9 | | |
| OOB_status_2 | r | 8 | | When 4bits OOB_staus_3~0 is 4'b1010, it means PHY is ready, all other states mean not ready |

## 8.6 SATA Status Register (4830h-4833h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| sStatus | r | 31-0 | 32'b 0 | SATA Status |

## 8.7 SATA Error Register (4834h-4837h)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| sError | r | 31-0 | 32'b 0 | SATA Error |

## 8.8 SATA Control Register (4838h-483Bh)

| Field name | rscu | bit # | Reset | Description |
|---|---|---|---|---|
| sControl | rw | 31-0 | 32'b 0 | SATA Control |

## 9. Data BUFFER:

| Address | Read Value | Write Value |
|---|---|---|
| 5000h-5FFFh | Data BUFFER | Data BUFFER |

## 10. USB Registers:

### 10.1 Device Status (Dev_Status[7:0], 0x6020)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| VBUS | r | 7 | 1'b0 | Read: USB's VBUS status |
| Test_mode | rsu | 6 | 1'b0 | Set when SET_FEATURE (TEST_MODE). |
| Attach | ru | 5 | 1'b1 | Hardware reset default state. Clear if detect VBUS valid. Then set Power bit |
| Powered | ru | 4 | 1'b0 | Set if VBUS=1 & previous state is Attach. Or, power interruption. |
| Suspend | ru | 3 | 1'b0 | After bus IDLE for sometime, hardware set this bit. When RESUME detected, hardware reset this bit and return to previous state |
| Default | ru | 2 | 1'b0 | After bus reset, hardware set this bit. |
| Addressed | rscu | 1 | 1'b0 | Set_Address or Set_Configuration(0) |
| Configured | rscu | 0 | 1'b0 | Set_configuration |

### 10.2 Function Address (Funct_Adr[7:0], 0x6021)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | ru | 7 | 1'b0 | Reserved |
| Adr | ru | 6:0 | 7'b0 | Set_Address |

### 10.3 Test Mode (Test_mode[7:0], 0x6022)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | ru | 7:4 | 4'b0 | Reserved |

| | | | | |
|---|---|---|---|---|
| Test_mode | rwu | 3:0 | 4'b0 | Test Mode Selectors(Table 9-7, USB2.0 spec)<br>4'h1: Test_J<br>4'h2: Test_K<br>4'h4: Test_SE0_NAK<br>4'h8: Test_Packet<br>others: RSVD |

## 10.4 End Point TX Data Length Low Bytes (Ep_TxLength[7:0], 0x6025)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Ep_TxLength | rwu | 7:0 | 8'b0 | For EP1 (Bulk_IN): For ATA-Command-no-DMA-involved, this field indicates how many bytes sent back to host. Maximum 512-bytes |

## 10.5 End Point TX Data Length High Bytes (Ep_TxLength[15:8], 0x6026)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | r | 7:2 | 6'b0 | Reserved |
| Ep_TxLength | rwu | 1:0 | 2'b0 | High bytes |

## 10.6 End Point 0 Status/Control (EP0_Status [7:0], 0x6030: Set, 0x6031: Clear)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Suspend_gnt | rsc | 7 | 1'b0 | Suspend-request granted |
| USB_busRst | rcu | 6 | 1'b0 | Set by hardware after an USB bus reset detected. Clear by firmware. |
| Bulk_only_Rst | rcu | 5 | 1'b0 | Set by hardware, read and cleared by firmware after firmware responds bulk-only-reset command done. |
| EP0_line_st | ru | 4:3 | 2'b0 | Line States |
| EP0_speed | ru | 2 | 1'b0 | 1—HS, 0--FS |
| Remote_wakeup | rscu | 1 | 1'b0 | Set/Clr by firmware. Remote wakeup request. |
| Halt | rscu | 0 | 1'b0 | 1-EP0 halt. Function STALL. Device reset is require to clear this bit |

## 10.7 End Point 0 Status/Control2 (EP0_Status2 [7:0], 0x6032: Set, 0x6033: Clear, Bulk-IN)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| FW_RDY | rsc | 7 | 1'b0 | 0: Default value as no firmware installed. Hardware response all control packets for firmware download in most cases.<br>1: Firmware controls some setup packet response. |
| RSVD | r | 6:4 | 3'b0 | Reserved |
| EP0_StatRun | rsu | 3 | 1'b0 | Set by firmware if device ready to go to control status stage. |
| EP0_OUT | rcu | 2 | 1'b0 | Set by hardware if a control command-data is received. Clear by firmware after processing. |
| EP0_Run | rsu | 1 | 1'b0 | Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer length in the Ep_TxLength( 0x25, 0x26) |
| EP0_Setup | rcu | 0 | 1'b0 | Set by hardware if a control command is received. Clear by firmware after processing. |

## 10.8 End Point TX Data Length Low Bytes (Ep0TxLength [7:0], 0x6034)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | r | 7 | 1'b0 | Reserved |
| Ep0TxLength | rwu | 6:0 | 7'b0 | For EP0 (Control): This field is filled by firmware. When firmware taking control setup packet response, firmware write this field to inform hardware the data length to be send back to host. Maximum 64-bytes. |

## 10.9 Setup Packet (Hdr0—Hdr7 [7:0], 0x6038—0x603F)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Hdr | ru | 7:0 | 8'bx | 8 bytes setup packet. |

## 10.10 End Point 1 Status/Control (EP1_Status [7:0], 0x6040: Set, 0x6041: Clear, Bulk-IN)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| GTotalCntEq0 | r | 7 | 0 | 1— Ata Global Total counter equal 0<br>0--- Ata Global Total counter not equal 0 |
| TotalCntEq0 | r | 6 | 0 | 1— Ata Total counter equal 0<br>0--- Ata Total counter not equal 0 |
| RSVD | r | 5:4 | 2'b0 | Reserved |
| CSW_Run | rscu | 3 | 1'b0 | Set by firmware when firmware ready to send CSW. Clear by hardware after CSW is sent successfully. |
| RSVD | r | 2 | 1'b0 | Reserved |
| EP1_Run | rscu | 1 | 1'b0 | Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer length in the Ep_TxLength( 0x25, 0x26) |
| Halt | rscu | 0 | 1'b0 | 1-EP1 halt. |

## 10.11 End Point 2 Status/Control (EP2_Status [7:0], 0x6050: Set, 0x6051 Clear, Bulk-OUT)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| FS_En | rw | 7 | 1'b0 | Force device to Full Speed only mode |
| RSVD | r | 6:3 | 4'b0 | Reserved |
| EP2_Rx | rcu | 2 | 1'b0 | Set by hardware after the bulk out packet received. The number of total data length received will be shown in Usb_rxLength register. This bit is used by firmware to monitor the data transfer between USB and internal data buffer. This bit is cleared by firmware or automatically cleared by hardware after the next CBW received or sg0Run bit set by firmware. |
| EP2_CBW | rcu | 1 | 1'b0 | Set by hardware if a valid CBW received. Clear after processing by firmware. |
| Halt | rscu | 0 | 1'b0 | 1-EP2 halt. |

## 10.12 Usb_rxLength (usb_rxLength[7:0], 0x6052, Bulk-OUT)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| rxLength | ru | 7:0 | 8'b0 | The low byte of data length received. This register is used to show how many date received from USB to internal data buffer. |

### 10.13 End Point 3 Status/Control (EP3_Status [7:0], 0x6060: Set, 0x6061: Clear, INTR-IN)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | r | 7:3 | 5'b0 | Reserved |
| EP3_run | rsu | 2 | 1'b0 | 1—packet ready. Cleared by hardware after Tx completed |
| RSVD | r | 1 | 1'b0 | Reserved |
| Halt | rscu | 0 | 1'b0 | 1-EP3 halt. |

### 10.14 End Point TX Data Length Low Bytes (Ep3TxLength [7:0], 0x6062)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| RSVD | r | 7 | 1'b0 | Reserved |
| Ep3TxLength | rwu | 7:0 | 7'b0 | For EP3 (INT_IN): This field is filled by firmware. Firmware writes this field to inform hardware the data length to be sent back to host. Maximum 64-bytes. |

### 10.15 Total Count0 (TotalCnt[7:0], 0x6070 TotalCnt0)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| TotalCnt0 | rwu | 7-0 | 8'b0 | TotalCnt[7:0] |

### 10.16 Total Count1 (TotalCnt[15:8], 0x6071 TotalCnt1)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| TotalCnt1 | rwu | 7-0 | 8'b0 | TotalCnt[15:8] |

### 10.17 Total Count2 (TotalCnt[23:16], 0x6072 TotalCnt2)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| TotalCnt2 | rwu | 7-0 | 8'b0 | TotalCnt[23:16] |

### 10.18 Total Count3 (TotalCnt[31:24], 0x6073 TotalCnt3)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| TotalCnt3 | rwu | 7-0 | 8'b0 | TotalCnt[31:24] |

### 10.19 Load Total Count (Load TotalCnt, 0x6074)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| Reserved | r | 7-1 | 7'b0 | Reserved |
| LoadTotalCnt | w | 0 | 1'b0 | Write an 1 to this bit will re-load the value from register 0x73-0x70's TotalCnt[31:0] to internal counter. |

### 10.20 Global Total Count0 (GTotalCnt[7:0], 0x6080 GTotalCnt0)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| GTotalCnt0 | rwu | 7-0 | 8'b0 | GTotalCnt[7:0] |

### 10.21 Global Total Count1 (GTotalCnt[15:8], 0x6081 GTotalCnt1)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| GTotalCnt1 | rwu | 7-0 | 8'b0 | GTotalCnt[15:8] |

### 10.22 Global Total Count2 (GTotalCnt[23:16], 0x6082 GTotalCnt2)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| GTotalCnt2 | rwu | 7-0 | 8'b0 | GTotalCnt[23:16] |

### 10.23 Global Total Count3 (GTotalCnt[31:24], 0x6083 GTotalCnt3)

| Field name | rscu | bit # | reset | Description |
|---|---|---|---|---|
| GTotalCnt3 | rwu | 7-0 | 8'b0 | GTotalCnt[31:24] |

## 11. Electrical Information:

### 11.1 Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| Vcc | Power Supply | -0.3 | 3.6 | V |
| Vin | Input Voltage | -0.3 | Vcc+0.3 | V |
| Vout | Output Voltage | -0.3 | Vcc+0.3 | V |
| Tstg | Storage Temperature | -55 | 150 | °C |

### 11.2 Recommended Operating Conditions

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Vcc | Power Supply | 3.0 | 3.3 | 3.6 | V |
| Vin | Input Voltage | 0 | - | Vcc | V |
| Tj | Commercial Junction Operating Temperature | 0 | 25 | 115 | °C |
| | Industrial Junction Operation Temperature | -40 | 25 | 125 | °C |

### 11.3 General DC Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Iil | Input Leakage Current | -1 | | 1 | μA |
| Ioz | Tristate Leakage Current | -1 | | 1 | μA |
| Cin | Input Capacitance | | 2.8 | | pF |
| Cout | Output Capacitance | 2.7 | | 4.9 | pF |
| Cbid | Bi-directional Buffer Capacitance | 2.7 | | 4.9 | pF |

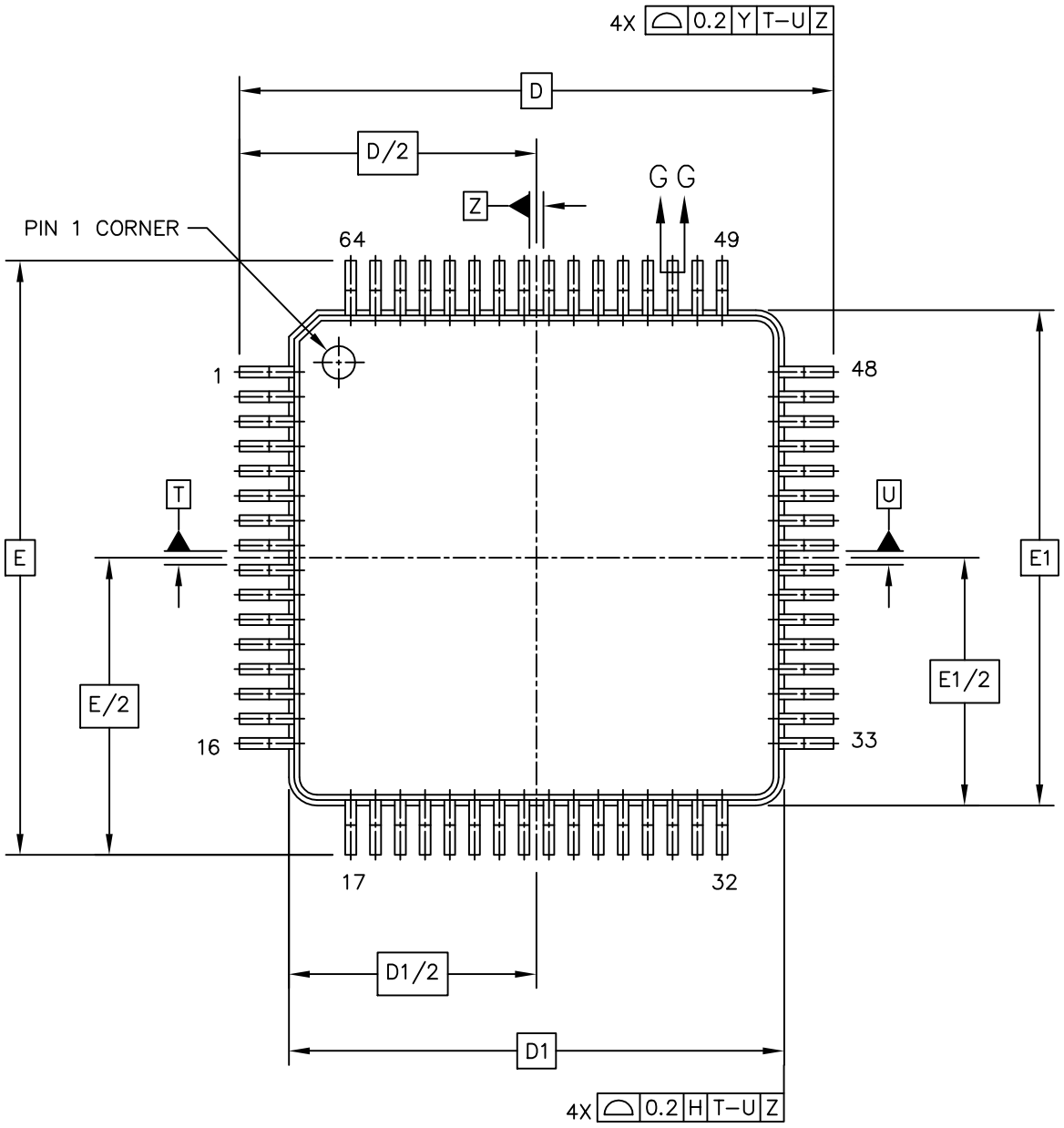
## 11.4 DC Electrical Characteristics for 3.3V Operation

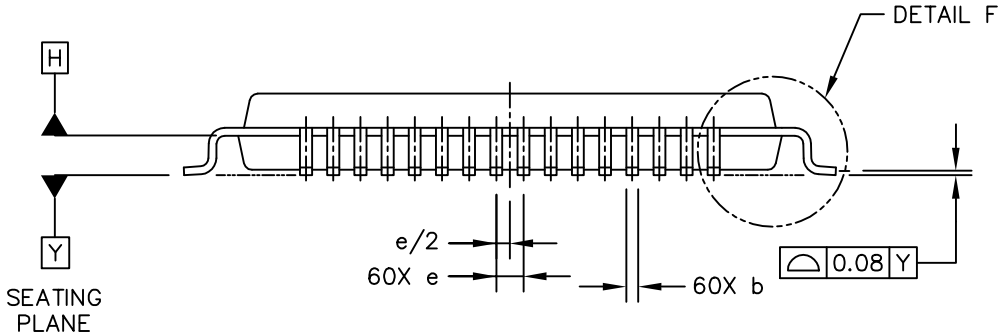
(Under Vcc=3.0-3.6V, Tj=0-115C)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Vil | Input Low Voltage | CMOS | -0.3 | | 0.8 | V |
| Vih | Input High Voltage | CMOS | 2.0 | | 5.5 | V |
| Vol | Output Low Voltage | Ioh-2-24mA | | | 0.4 | V |
| Voh | Output High Voltage | Ioh=2-24mA | 2.4 | | | V |
| Ri | Input Pullup/pulldown Resistance | Vil=0/Vih=Vcc | | 75 | | kΩ |
| Icc | Operating Supply Current | Vcc=3.3V | | | 150 | mA |

## 12. Packaging Specification

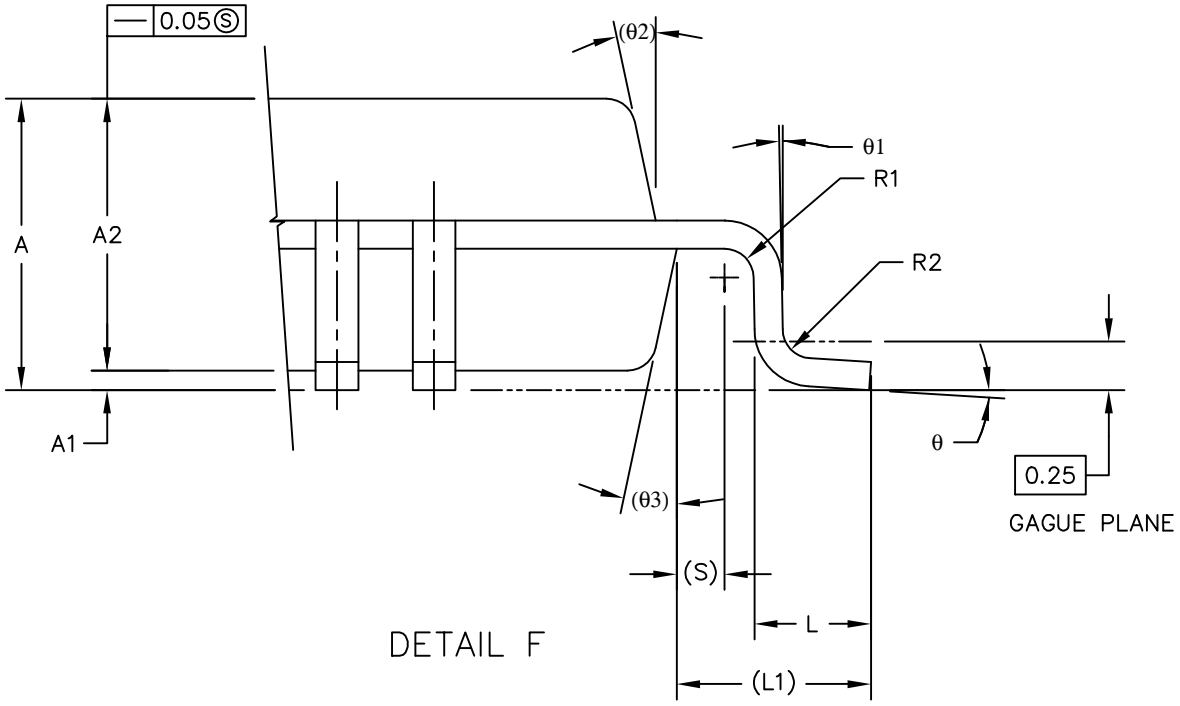
| | PACKAGE OUTLINE | | |
|---|---|---|---|
| | | I | |
| | | | |



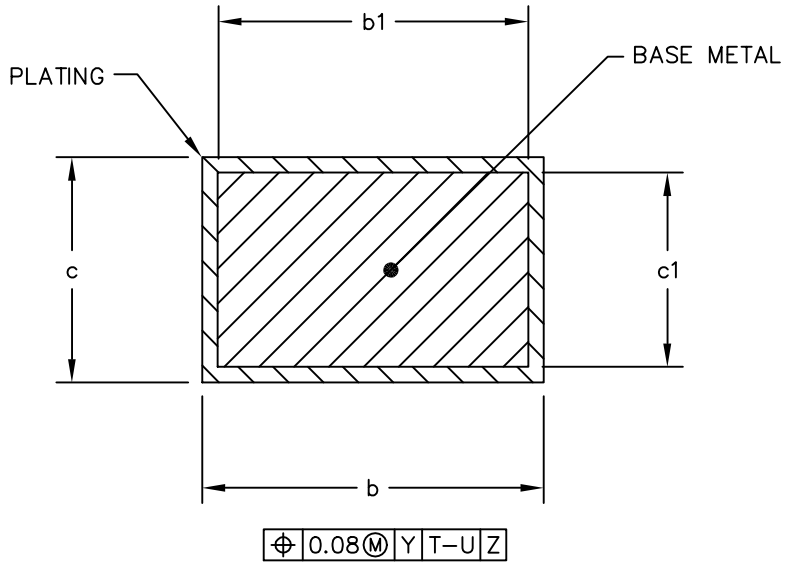




| TITLE: LQFP 64 LD 10X10X1.4 PKG 0.5 PITCH POD | | |
|---|---|---|
| | SHEET | 1 OF 3 |

| | PACKAGE OUTLINE | | |
|---|---|---|---|
| | | I | |
| | | | |




DETAIL F




SECTION G–G

| TITLE: LQFP 64 LD 10X10X1.4 PKG 0.5 PITCH POD | | |
|---|---|---|
| | SHEET | 2 OF 3 |

| | PACKAGE OUTLINE | | |
|---|---|---|---|
| | | I | |
| | | | |

NOTES:

1. DIMENSOIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE DATUM H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

| DIM | MIN | MAX | DIM | MIN | MAX | DIM | MIN | MAX |
|---|---|---|---|---|---|---|---|---|
| A | --- | 1.6 | L1 | 1 REF | | | | |
| A1 | 0.05 | 0.15 | R1 | 0.1 | 0.2 | | | |
| A2 | 1.35 | 1.45 | R2 | 0.1 | 0.2 | | | |
| b | 0.17 | 0.27 | S | 0.2 REF | | | | |
| b1 | 0.17 | 0.23 | θ | 0° | 7° | | | |
| c | 0.09 | 0.2 | θ1 | 0° | --- | | | |
| c1 | 0.09 | 0.16 | θ2 | 12° REF | | | | |
| D | 12 BSC | | θ3 | 12° REF | | | | |
| D1 | 10 BSC | | | | | | | |
| e | 0.5 BSC | | | | | | | |
| E | 12 BSC | | | | | | | |
| E1 | 10 BSC | | | | | | | |
| L | 0.45 | 0.75 | | | | | | |

| TITLE: LQFP 64LD 10X10X1.4 PKG 0.5 PITCH POD | | |
|---|---|---|
| | SHEET | 3 OF 3 |