INIC-1510
USB to PATA Bridge
Specification

Version 1.0
March 30, 2006
Initio Corporation

Change History:

3/30/06 - Release

Table of Contents

1. Introduction:

The INIC-1510 provides an advanced solution to connect ATAPI or EIDE devices to USB interface with integrated CPU and embedded SRAM. To provide high performance and cost effective solution, the INIC-1510 integrates USB-PHY, Mass Storage Class Bulk-Only USB function, ATA control block and microprocessor into a single ASIC. The INIC-1510 provides the data transfer rate of up to 60 MB/sec; its ATA interface supports ultra DMA modes up to 100 MB/sec.

1.1 Feature Summary

- USB Mass Storage Class Bulk-Only specification-compliant (version 1.0)
- Two Bulk endpoints(IN and OUT) and one Interrupt endpoint(IN)
- T13 1410D ATA/ATAPI-6 Compliant(3.3 V with 5V tolerance)
- Support DMA mode 0-2, and UDMA mode 2, 3, 4 and 5 (up to 100MB/s)
- Integrated internal CPU with embedded SRAM
- Implement the firmware download mechanism
- Low power CMOS with 3.3Volts
- 64-pin LQFP package

1.2 Firmware/Software Support

- USB Mass Storage Class Bulk-Only Transport support
- Provide software utilities for downloading the upgraded firmware code

1.3 Devices Support

- Hard disk drives
- CD-RW devices
- DVDs
- Removable media devices.

2. USB to ATA Block Diagram:

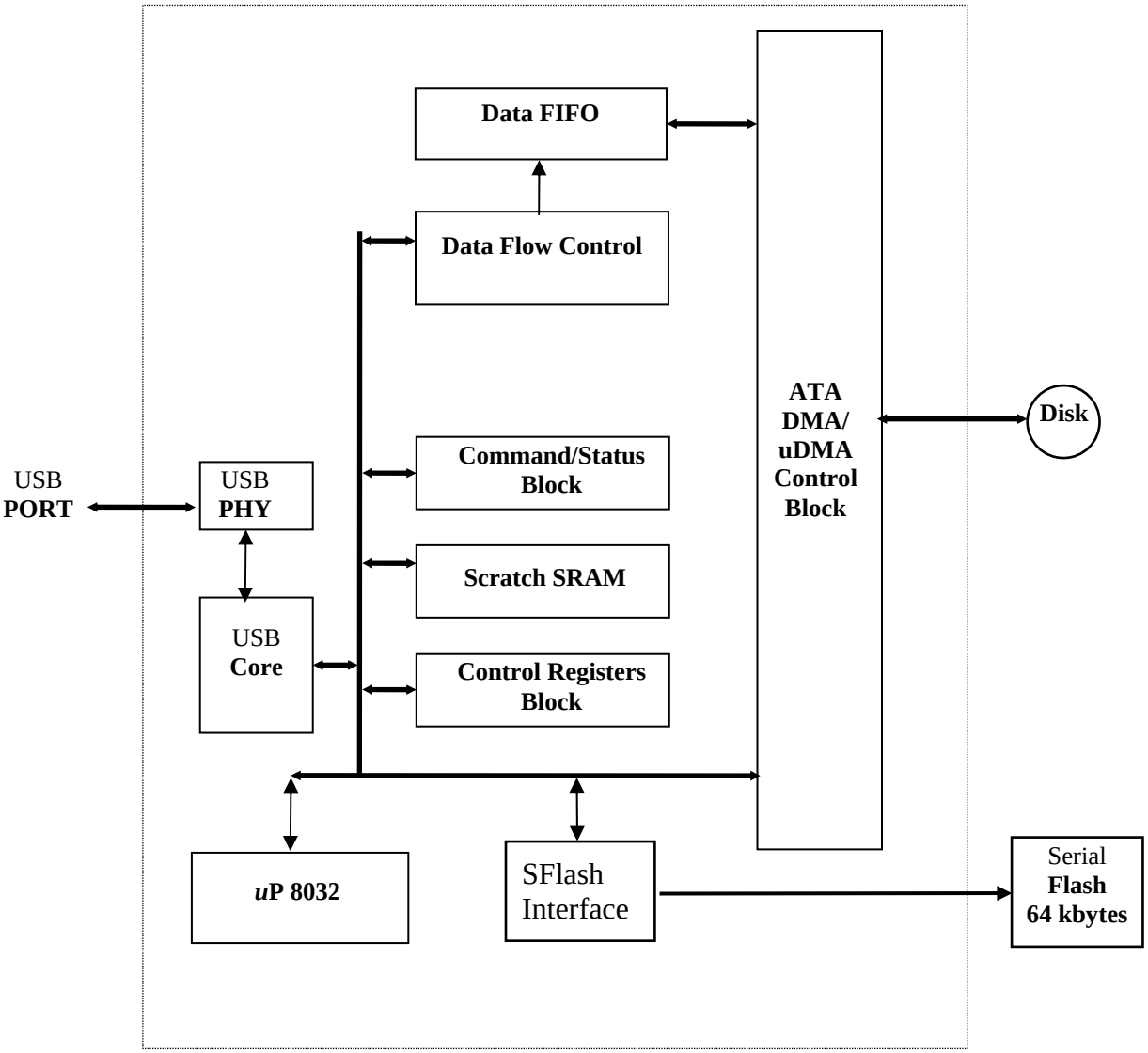


Figure 1: INIC-1510 Block Diagram

3. Pin Signal Description: (64-pin package)

3.1 USB Interface

Signal Name	Pin Number	I/O	Driver Type	Description
DP	21	I/O	USB high /full speed buffer (D+)	High/Full speed D+ signal
DM	20	I/O	USB high/full speed buffer (D-)	High/Full speed D- signal
RREF	19	A	Power	PLL voltage reference. Current source for 330R(1%) resistor connected to AVSS
VBUS	10	I	PIW	Active HIGH. Indicates that VBUS is present.
XIN	15	I	A	Crystal oscillator input (12MHz)
XOUT	16	O	A	Crystal oscillator output (12MHz)

3.2 Serial Flash Interface

Signal Name	Pin Number	I/O	Driver Type	Description
SCEN /GPIOF7	9	I/O	PBU16W	Serial Flash Chip Enable
SD /GPIOF6	8	I/O	PBU16W	Serial Flash data input/output
SCK /GPIOF5	7	I/O	PBU16W	Serial Flash clock

3.3 ATA Interface (driving current 4mA-10mA controlled by Register A8[1:0])

Signal Name	Pin Number	I/O	Driver Type	Description
DD[15:0]/ GPIOD[7:0], GPIOC[7:0]	37, 40, 42, 44, 46, 48, 52, 54, 53, 51, 47, 45, 43, 41, 38, 36	I/O	PBSCUDSL	ATA Data Bus
DA[2:0] /GPIOE[2:0]	29, 28, 27	I/O	PBSCUDSL	Device Address
RESET0# /GPIOB6	60	I/O	PBSCUDSL	Reset 0(Out)
DCS0[1:0]# /GPIOE[4:3]	58, 55	I/O	PBSCUDSL	ATA Device Chip Select 0(Out)
DMARQ0	34	I/O	PBSCUDSL	DMA Request 0(In)
DMACK0# /GPIOB1	30	I/O	PBSCUDSL	DMA Acknowledge 0(Out)

DIOW0# /GPIOB3	33	I/O	PBSCUDSL	I/O Write 0(Out)
DIOR0# /GPIOB2	32	I/O	PBSCUDSL	I/O Read 0(Out)
IORDY0 /GPIOE5	31	I/O	PBSCUDSL	I/O ready 0(In)
ATAINTR0	59	I/O	PBSCUDSL	ATA Interrupt

3.4 System Interface

Signal Name	Pin Number	I/O	Driver Type	Description
PORST#	2	I	PISW	Power On Reset. When this signal is active, all of pins on ATA interface should be tri-stated.
TestMode[1:0]	26, 25	I	PID	Test Mode Select 00-> Normal Operation Mode 01-> usb-bist 10-> MBist 11-> Scan

3.5 GPIO Interface

Signal Name	Pin Number	I/O	Driver Type	Description
P1.[2:0] P1.4	61, 62, 1, 3	I/O	PB16W	uP8032 I/O port 1, can be used as extra GPIOs
P3.[1:0] P3.3	4, 5, 6	I/O	PB16W	uP8032 I/O port 3. can be used as extra GPIOs

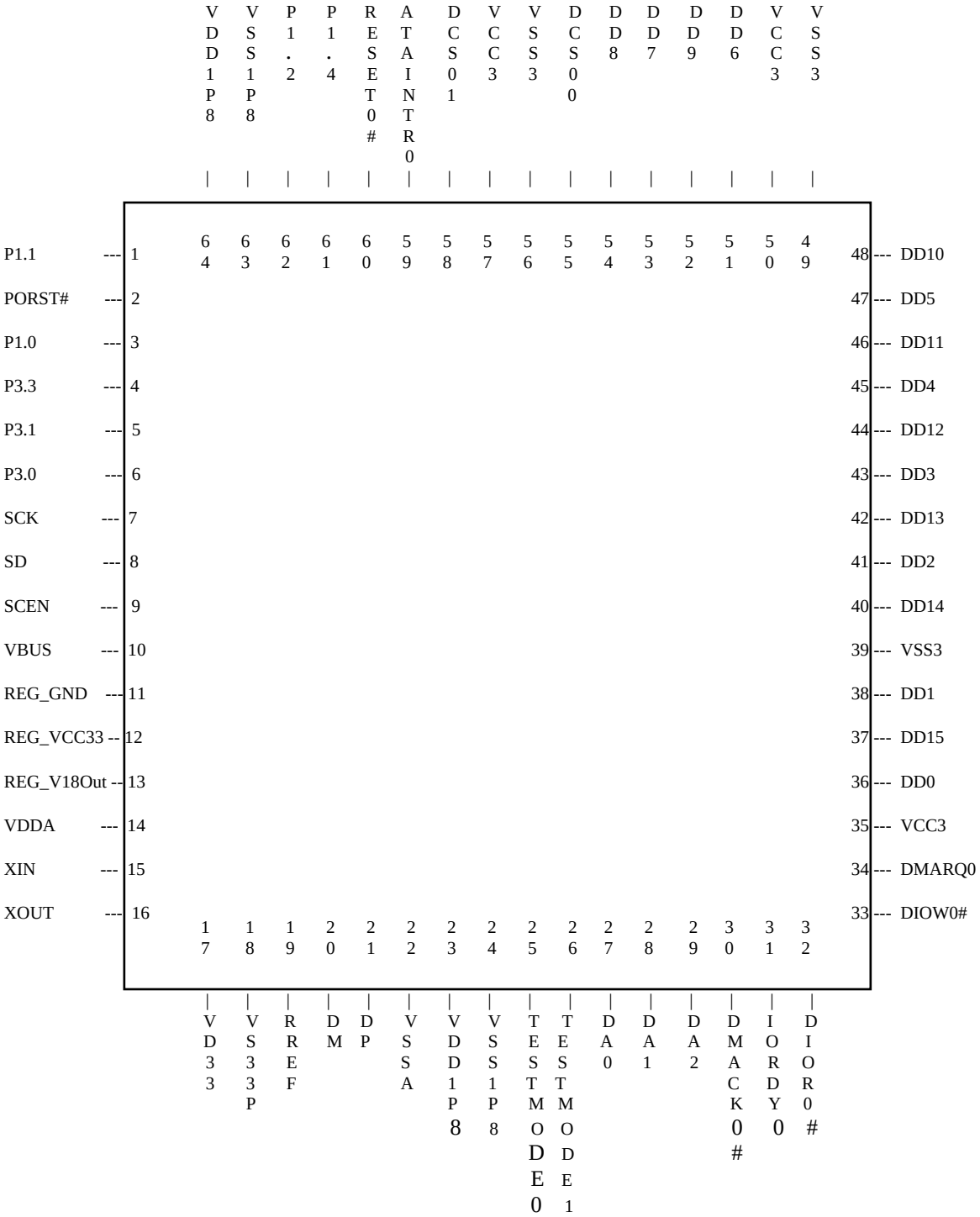
3.6 Power Regulator pins

Signal Name	Pin Number	I/O	Driver Type	Description
REG_VCC33	12	I		Total 1 pin
REG_GND	11	I		Total 1 pin
REG_V18Out	13	O		Total 1 pin

3.7 Power/GND

Signal Name	Pin Number	I/O	Driver Type	Description
VCC3	35, 50, 57			IO 3.3V
VSS3	39, 49, 56			IO GND
VDD1P8	23, 64			Core 1.8V
VSS1P8	24, 63			Core GND
VD33	17			3.3V, for VDD33P and VD33
VS33P	18			USB IO Cell GND
VDDA	14			1.8V for PLL
VSSA	22			VSSA for PLL

3.8 64-Pin Diagram



4. Firmware Program/Download procedure

1. Host send READ_CHIP_ID packet through control channel to read chip-ID, which is 0x29C5_1510 here.
2. Host send HOLD_CPU packet through control channel to set HOLD_CPU bit.
3. Host may send FLASH_WRITE/FLASH_READ/DATA_WRITE/DATA_READ packet through control channel to WRITE/READ flash or data space.

Host may program and read serial flash memory through default endpoint. Flash write setup packet format is:

Offset	Field	Size	Value	Description
0	bmReqType	1	0x40	Vendor write
1	bReq	1		Flash write [7]: 0—Flash memory [6]: 1—addr valid [5]: 1—data valid [4:0]: 5'h01—Flash Write
2	wValue	2	Addr[7:0]	Address to be written
3			Addr[15:0]	
4	wIndex	2	opCode	
5			Data[7:0]	Flash data
6	wLength	2	0x00	
7			0x00	

Flash Read setup packet format is:

Offset	Field	Size	Value	Data	Description
0	bmReqType	1	0xc0	Data from Flash	Vendor read
1	bReq	1			Flash read [7]: 0—Flash memory [6]: 1—addr valid [5]: 1—data valid [4:0]: 5'h02—Flash Read
2	wValue	2	Addr[7:0]		Address to be written
3			Addr[15:0]		
4	wIndex	2	opCode		
5			0x00		Don't care
6	wLength	2	0x01		
7			0x00		

READ_CHIP_ID setup packet format is:

Offset	Field	Size	Value	Data	Description
0	bmReqType	1	0xc0	Chip-ID	Vendor read

1	bReq	1	0x03	0x10, 0x15, 0xc9, 0x25	
2	wValue	2	0x00		
3			0x00		
4	wIndex	2	0x00		Don't care
5			0x00		Don't care
6	wLength	2	0x04		
7			0x00		

HOLD_CPU setup packet format is:

Offset	Field	Size	Value	Description
0	bmReqType	1	0x40	Vendor write
1	bReq	1	0x04	HOLD_CPU
2	wValue	2	0x00	Don't care
3			0x00	
4	wIndex	2	0x00	Don't care
5			0x00	Don't care
6	wLength	2	0x00	Don't care
7			0x00	Don't care

5. Register Address Mapping:

5.1 USB Block (address area: 60xx)

Address	Read Value	Write Value
20h	Dev_Status	Dev_Status
21h	Funct_Adr	Funct_Adr
22h	Test_mode	Test_mode
25h	EpTxLength[7:0]	EpTxLength[7:0]
26h	EpTxLength[15:8]	EpTxLength[15:8]
30h	EP0_Status	EP0_ Control (Set)
31h	EP0_Status	EP0_ Control (Clear)
32h	EP0_Status2	EP0_ Control 2(Set)
33h	EP0_Status2	EP0_ Control 2(Clear)
34h	EP0TxLength	EP0TxLength
38-3F	Hdr0-7	-
40h	EP1_Status	EP1_ Control (Set)
41h	EP1_Status	EP1_ Control (Clear)
50h	EP2_Status	EP2_ Control (Set)
51h	EP2_Status	EP2_ Control (Clear)
52h	Usb_rxLength[7:0]	-
53h	Usb_rxlength[15:8]	-
60h	EP3_Status	EP3_ Control (Set)
61h	EP3_Status	EP3_ Control (Clear)
70h	TotalCnt0	TotalCnt0
71h	TotalCnt1	TotalCnt1
72h	TotalCnt2	TotalCnt2
73h	TotalCnt3	TotalCnt3
74h	-	LoadTotalCnt
80h	GTotalCnt0	GTotalCnt0

81h	GTotalCnt1	GTotalCnt1
82h	GTotalCnt2	GTotalCnt2
83h	GTotalCnt3	GTotalCnt3

5.2 ATA Block: (address area: 40xx)

Address	Read Value	Write Value
90h	Data[7:0]	Data[7:0]
91h	Error	Features
92h	SectorCount	SectorCount
93h	SectorNumber	SectorNumber
94h	CyclinderLow	CylinderLow
95h	CylinderHigh	CylinderHigh
96h	Device/Head	Device/Head
97h	Status	Command
98h	Reserved	Reserved
99h	Reserved	reserved
9Ah	Reserved	reserved
9Bh	Reserved	reserved
9Ch	Reserved	reserved
9Dh	Reserved	reserved
9Eh	AlternateStatus	DeviceControl
9Fh	Reserved	reserved
A0h	FIFO0D[7:0]	FIFO0D[7:0]
A2h	sgPCtl	sgPCtl
A3h	FifoSt	FifoSt
A4h	gpioData	gpioData
A5h	gpioCtl	gpioCtl
A6h	TestCtl0	TestCtl0
A8h	DrvCtl	DrvCtl
ACh	upCtl	upCtl
AFh	MiscCtl	MiscCtl (internal testing)
B0h	LinkCtl	LinkCtl
B1h	DmaCtl	DmaCtl
B4h	sgDCtl	sgDCtl_Set
B5h	sgDCtl	sgDCtl_Clr
B6h	AtaCtl	AtaCtl
B7h	AtaStatus	AtaStatus
BDh	SPI_Status	SPI-Ctrl
BEh	SPI_RdData	SPI-WrData
BFh	SPI_Command	SPI-Command
C0h,C2h-CEh	RData[7:0]	WData[7:0]
C1h,C3h-CFh	RData[15:8]	WData[15:8]
D6h	ATA_Status_Hi	ATA_Status_Hi
D7h	ATA_Status_Lo	ATA_Status_Lo
D8h	UsbINT_En	UsbINT_En
D9h	UsbINT_Status	UsbINT_Clr
DCh	GPIOA_INT_En	GPIOA_INT_En
DDh	SPI_ADR[7:0]	SPI_ADR[7:0]
DEh	SPI_ADR[15:8]	SPI_ADR[15:8]
DFh	SPI_ADR[31:16]	SPI_ADR[31:16]

F2h	GPIOB_Din[7:0]	GPIOB_Dout[7:0]
F3h	GPIOB_Ctrl[7:0]	GPIOB_Ctrl[7:0]
F4h	GPIOC_Din[7:0]	GPIOC_Dout[7:0]
F5h	GPIOC_Ctrl[7:0]	GPIOC_Ctrl[7:0]
F6h	GPIOD_Din[7:0]	GPIOD_Dout[7:0]
F7h	GPIOD_Ctrl[7:0]	GPIOD_Ctrl[7:0]
F8h	GPIOE_Din[7:0]	GPIOE_Dout[7:0]
F9h	GPIOE_Ctrl[7:0]	GPIOE_Ctrl[7:0]
FAh	GPIOF_Din[7:0]	GPIOF_Dout[7:0]
FBh	GPIOF_Ctrl[7:0]	GPIOF_Ctrl[7:0]

Note: 1. Every Read operation from any of 9Xh registers needs to be followed by another Read operation on C0h.
2. Register C1h is used for accessing the high byte of 16-bit PIO data.

5.3 CMD/DATA Block: (address area: 40xx)

Address	Read Value	Write Value
100h-13Fh (64 bytes)	CmdRx0Buffer	Can not be written by CPU
140h-17Fh (64 bytes)	CmdRx1Buffer	Can not be written by CPU
1C0h-1EFh (64 bytes)	CmdTx1Buffer	CmdTx1Buffer
240h-26Fh (64 bytes)	CmdTx3Buffer	CmdTx3Buffer
280h-2AFh (64 bytes)	CmdTx4Buffer	CmdTx4Buffer

5.4 DMA Block: (address area: 40xx)

Address	Read Value	Write Value
500h-53Fh	sgList[3:0]	sgList[3:0]

5.5 Data Space Mapping

Mapping Address	Type	Access Type	Mapping Block
0000h-3FFFh	Data	Read/Write	Internal SRAM (16KB)
4000h-47FFh	Data	Read/Write	Internal Register/Buffers
5000h-5FFFh	Data	Read/Write	SgBuffer (4KB)
6000h-60FFh	Data	Read/Write	USB registers
8000h-FFFFh	Data	Read/Write	External SRAM (32KB)

6. Register Descriptions:

The following are USB registers, based on 0x6000

6.1.1 Device Status (Dev_Status[7:0], 0x20)

Field name	rscu	bit #	reset	Description
RSVD	r	7	1'b0	Reserved
Test_mode	rsu	6	1'b0	Set when SET_FEATURE (TEST_MODE). Exit by cycle VBUS.
Attach	ru	5	1'b1	Hardware reset default state. Clear if detect VBUS valid. Then set Power bit
Powered	ru	4	1'b0	Set if VBUS=1 & previous state is Attach. Or, power interruption.
Suspend	ru	3	1'b0	After bus IDLE for sometime, hardware set this bit. When RESUME detected, hardware reset this bit and return to previous state
Default	ru	2	1'b0	After bus reset, hardware set this bit.
Addressed	rscu	1	1'b0	Set_Address or Set_Configuration(0)
Configured	rscu	0	1'b0	Set_configuration

6.1.2 Function Address (Funct_Adr[7:0], 0x21)

Field name	rscu	bit #	reset	Description
RSVD	ru	7	1'b0	Reserved
Adr	ru	6:0	7'b0	Set_Address

6.1.3 Test Mode (Test_mode[7:0], 0x22)

Field name	rscu	bit #	reset	Description
RSVD	ru	7:4	4'b0	Reserved
Test_mode	rwu	3:0	4'b0	Test Mode Selectors(Table 9-7, USB2.0 spec) 4'h1: Test_J 4'h2: Test_K 4'h4: Test_SE0_NAK 4'h8: Test_Packet others: RSVD

6.1.4 End Point TX Data Length Low Bytes (Ep_TxLength[7:0], 0x25)

Field name	rscu	bit #	reset	Description
Ep_TxLength	rwu	7:0	8'b0	For EP1 (Bulk_IN): For ATA-Command-no-DMA-involved, this field indicates how many bytes sent back to host. Maximum 512-bytes

6.1.5 End Point TX Data Length High Bytes (Ep_TxLength[15:8], 0x26)

Field name	rscu	bit #	reset	Description
RSVD	r	7:2	6'b0	Reserved
Ep_TxLength	rwu	1:0	2'b0	High bytes

6.1.6 End Point 0 Status/Control (EP0_Status[7:0], 0x30: Set, 0x31: Clear)

Field name	rscu	bit #	reset	Description
Suspend_gnt	rsc	7	1'b0	Suspend-request granted
Usb_busRst	rcu	6	1'b0	Set by hardware after an usb bus reset detected. Clear by firmware.
Bulk_only_Rst	rcu	5	1'b0	Set by hardware, read and cleared by firmware after firmware responds bulk-only-reset command done.
RSVD	ru	4:3	2'b0	Reserved
EP0_speed	ru	2	1'b0	1—HS, 0--FS
Remote_wakeup	rscu	1	1'b0	Set/Clr by firmware. Remote wakeup request.
Halt	rscu	0	1'b0	1-EP0 halt. Function STALL. Device reset is require to clear this bit

6.1.7 End Point 0 Status/Control2 (EP1_Status2[7:0], 0x32: Set, 0x33: Clear, Bulk-IN)

Field name	rscu	bit #	reset	Description
FW_RDY	rsc	7	1'b0	0: Default value as no firmware installed. Hardware response all control packet for firmware download in most case. 1: Firmware controls some setup packet response.
RSVD	r	6:4	3'b0	Reserved
EP0_StatRun	rsu	3	1'b0	Set by firmware if device ready to go to control status stage.
EP0_OUT	rcu	2	1'b0	Set by hardware if a control command-data is received. Clear by firmware after processing.
EP0_Run	rsu	1	1'b0	Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer length in the Ep_TxLength(0x25, 0x26)
EP0_Setup	rcu	0	1'b0	Set by hardware if a control command is received. Clear by firmware after processing.

6.1.8 End Point TX Data Length Low Bytes (Ep0TxLength[7:0], 0x34)

Field name	rscu	bit #	reset	Description
RSVD	r	7	1'b0	Reserved
Ep0TxLength	rwu	6:0	7'b0	For EP0 (Control): This field is filled by firmware. When firmware taking control setup packet response, firmware write this field to inform hardware the data length to be send back to host. Maximum 64-bytes.

6.1.9 Setup Packet (Hdr0—Hdr7[7:0], 0x38—0x3F)

Field name	rscu	bit #	reset	Description
Hdr	ru	7:0	8'bx	8 bytes setup packet.

6.1.10 End Point 1 Status/Control (EP1_Status[7:0], 0x40: Set, 0x41: Clear, Bulk-IN)

Field name	rscu	bit #	reset	Description
GTotalCntEq 0	r	7	0	1-> Ata Global TotalCnt equ 0 0-> else
TotalCntEq0	r	7	0	1-> Ata TotalCnt equ 0 0-> else
RSVD	r	5:4	4'b0	Reserved
CSW_Run	rscu	3	1'b0	Set by firmware when firmware ready to send CSW. Clear by hardware after CSW is sent successfully.
RSVD	r	2	1'b0	Reserved
EP1_Run	rscu	1	1'b0	Set by firmware. When firmware set this bit, the data will be transferred from data buffer to USB. How many bytes transferred is based on the data transfer length in the Ep_TxLength(0x25, 0x26)
Halt	rscu	0	1'b0	1-EP1 halt.

6.1.11 End Point 2 Status/Control (EP2_Status[7:0], 0x50: Set, 0x51 Clear, Bulk-OUT)

Field name	rscu	bit #	reset	Description
FS_En	rw	7	1'b0	1-> force device to Full Speed mode only
RSVD	r	6:3	5'b0	Reserved
EP2_Rx	rcu	2	1'b0	Set by hardware after the bulk out packet received. The number of total data length received will be shown in Usb_rxLength register. This bit is used by firmware to monitor the data transfer between USB and internal data buffer. This bit is cleared by firmware or automatically cleared by hardware after the next CBW received or sg0Run bit set by firmware.
EP2_CBW	rcu	1	1'b0	Set by hardware if a valid CBW received. Clear after processing by firmware.
Halt	rscu	0	1'b0	1-EP2 halt.

6.1.12 Usb_rxLength(usb_rxLength[7:0], 0x52, Bulk-OUT)

Field name	rscu	bit #	reset	Description
rxLength	rwu	7:0	8'b0	The low byte of data length received. This register is used to show how many date received from USB to internal data buffer.

6.1.13 Usb_rxLength(usb_rxLength[11:8], 0x53, Bulk-OUT)

Field name	rscu	bit #	reset	Description
rxLength	rwu	7:0	8'b0	The high byte of data length received. This register is used by firmware to show how many data received from USB to internal data buffer.

6.1.14 End Point 3 Status/Control (EP3_Status[7:0], 0x60: Set, 0x61: Clear, INTR-IN)

Field name	rscu	bit #	reset	Description

RSVD	r	7:3	5'b0	Reserved
EP3_run	rsu	2	1'b0	1—packet ready. Cleared by hardware after Tx completed
RSVD	r	1	1'b0	Reserved
Halt	rscu	0	1'b0	1-EP3 halt.

6.1.15 End Point TX Data Length Low Bytes (Ep3TxLength[7:0], 0x62)

Field name	rscu	bit #	reset	Description
RSVD	r	7	1'b0	Reserved
Ep3TxLength	rwu	7:0	7'b0	For EP3 (INT_IN): This field is filled by firmware. Firmware writes this field to inform hardware the data length to be sent back to host. Maximum 64-bytes.

6.1.16 Total Count0 (TotalCnt[7:0], 0x70 TotalCnt0)

Field name	rscu	bit #	reset	Description
TotalCnt0	rwu	7-0	8'b0	TotalCnt[7:0]

6.1.17 Total Count1 (TotalCnt[15:8], 0x71 TotalCnt1)

Field name	rscu	bit #	reset	Description
TotalCnt1	rwu	7-0	8'b0	TotalCnt[15:8]

6.1.18 Total Count2 (TotalCnt[23:16], 0x72 TotalCnt2)

Field name	rscu	bit #	reset	Description
TotalCnt2	rwu	7-0	8'b0	TotalCnt[23:16]

6.1.19 Total Count3 (TotalCnt[31:24], 0x73 TotalCnt3)

Field name	rscu	bit #	reset	Description
TotalCnt3	rwu	7-0	8'b0	TotalCnt[31:24]

6.1.20 Load Total Count (Load TotalCnt, 0x74)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	7'b0	Reserved
LoadTotalCnt	w	0	1'b0	Write an 1 to this bit will re-load the value from register 0x73-0x70's TotalCnt[31:0] to internal counter.

6.1.21 Global Total Count0 (GTotalCnt[7:0], 0x80 GTotalCnt0)

Field name	rscu	bit #	reset	Description
GTotalCnt0	rwu	7-0	8'b0	GTotalCnt[7:0]

6.1.22 Global Total Count1 (GTotalCnt[15:8], 0x81 GTotalCnt1)

Field name	rscu	bit #	reset	Description
GTotalCnt1	rwu	7-0	8'b0	GTotalCnt[15:8]

6.1.23 Global Total Count2 (GTotalCnt[23:16], 0x82 GTotalCnt2)

Field name	rscu	bit #	reset	Description
GTotalCnt2	rwu	7-0	8'b0	GTotalCnt[23:16]

6.1.24 Global Total Count3 (GTotalCnt[31:24], 0x83 GTotalCnt3)

Field name	rscu	bit #	reset	Description
GTotalCnt3	rwu	7-0	8'b0	GTotalCnt[31:24]

The following are general registers, and are in address area: 40XX

6.2.1 FIFO 0 Data Register (FIFO0D[7:0], 0x0A0)

Field name	rscu	bit #	reset	Description
Fifo0Data	rw	7:0	8'h0	DMA FIFO 0 Data register. Software can access DMA FIFO 0 through this register.

6.2.2 sgPioCmd Control Register (sgPCtl, 0x0A2)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	6'b0	Reserved.
Pio0Run	rw	0	1'b0	After set. Before set this bit, the firmware needs to disable AtaDMAEn bit on DMA Control register, write the package header into the segment of sgCMD buffer, set RUN bit on sgCMD Control register, and fill data into FIFO data register.

6.2.3 FIFO Status Register (FifoST, 0x0A3)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	6'b0	Reserved.
Fifo0Rst	rw	0	1'b0	DMA FIFO 0 Reset. This bit is used to reset DMA FIFO 0. This bit is self-cleared by hardware after set.

6.2.4 GPIO Data Register (gpioDATA, 0x0A4)

Field name	rscu	bit #	reset	Description
VBUS	r	7	1'b0	Read: USB's VBUS status
AtaRST0#	w	6	1'b1	ATA channel 0 reset signal. When clear, it will reset the ATA device.
GPIOD[5:0]	rw	5-0	6'h0	Write: GPIOOut[5:0], Read: GPIOIn[5:0]

6.2.5 GPIO Control Register (gpioCtl, 0x0A5)

Field name	rscu	bit #	reset	Description
GPIOEn	rw	7	1'b0	GPIO mode enable.
Reserved	r	6	1'b0	Reserved.
GPIOCtl[5:0]	rw	5-0	6'h0	General Purpose I/O Control 5-0. When set, the GPIO data is output.

6.2.6 Test Control 0 Register (TestCtl0, 0x0A6)

Field name	rscu	bit #	reset	Description
RstAtareq_	rw	7	1'b0	Ata request reset. When set, it will reset the current Ata request.
Reserved	rw	6	1'b0	Reserved.
RevID	r	5-4	2'h0	Revision ID. These 2 bits are read only.
Reserved	rw	6	1'b0	Reserved.

6.2.7 ATA I/O Cell Driving Control Register (DrvCtl, 0x0A8)

Field name	rscu	bit #	reset	Description
CFEn	rw	7	1'b0	Compact Flash Mode Enable. When set, the ATA engine will run in pseudo DMA mode enabling fast compact flash access.
CFReq	rw	6	1'b0	Compact Flash Request. When set, it indicates to the ATA engine that compact flash has requested data transfer.
Reserved	r	5-3	4'h0	Reserved.
AtaTSEn	rw	2	1'b0	ATA Bus Tristate Enable. Clear this bit to 0 will put the INI1430 ATA bus in tristate mode.
DrvSel	rw	1-0	2'h3	ATA Output Driving: 00: 4 mA 01: 6 mA 10: 8 mA 11: 10 mA

6.2.8 uP Control Register (upCtl, 0x0AC)

Field name	rscu	bit #	reset	Description
Reserved	r	7-2	6'b0	Reserved.
usbWakeupEn	rw	1	1'b0	1-> enable external interrupt wake up host
Reserved	r	0	1'b0	Reserved.

6.2.9 MiscCtl register (0x0AF)

Field name	rscu	bit #	reset	Description
Reserved	rw	7	1'b0	Reserved.
NewMode	rw	6	1'b0	0: inic1530 mode 1: enhance mode

Set_usbClkEn	rw	5	1'b0	1: usb clock free run
Enum	rw	4	1'b1	0: disconnect device from usb host
HidEn	rw	3	1'b0	0: endp will be IN(1)OUT(2)INTR(3) 1: endp will be IN(8)OUT(2)INTR(1)
Reserved	rw	2:0	3'b0	Reserved.

6.2.10 sgCmd Definition

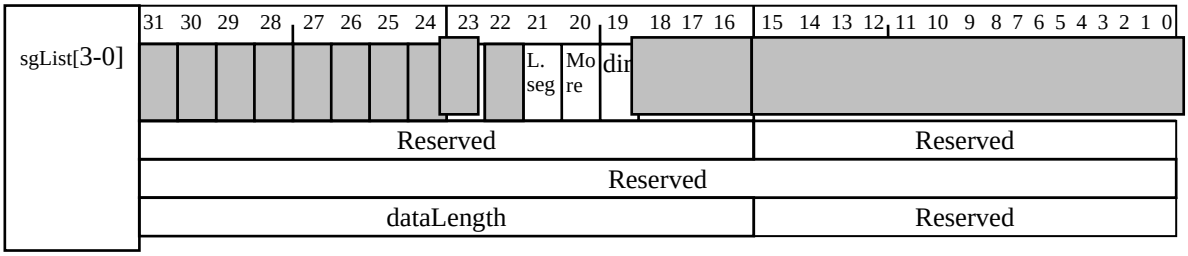


Figure 2: sgCmd format

Field name	width	quadlet	Bit #	Description
L. seg	1	1	21	If the command is the last one of S/G segments, this bit should be set by firmware.
More	1	1	20	If the number of commands in SgCmd buffer is more than one, this bit should be set by firmware.
Dir	1	1	19	When 0, the DMA data are transferred from P1394 bus to ATA device. When 1, the DMA data are transferred from ATA device to P1394 bus.

6.2.11 Link Control Register (linkCtl, 0x0B0)

Field name	rscu	bit #	reset	Description
Reserved	r	7-1	6'b0	Reserved.
softReset	rwu	0	1'b0	When set to 1, all Host Controller state is reset, all FIFO's are flushed, and Host Controller registers is reset. The read value of this bit is 1 while a soft reset or hard reset is in progress. The read value of this bit is 1 when neither soft reset nor hard reset is in progress. Software can use the value of his bit to determine when a reset has completed and the Host Controller is safe to operate.

6.2.12 DMA Control register (DmaCtl, 0x0B1)

Field name	rscu	bit #	reset	Description
Reserved	r	7-4	1'h0	Reserved.

DIOW#	rw	3	1'b1	When DMA FIFO is underrun, this bit is used by firmware to toggle DIOW# signal.
DIOR#	rw	2	1'b1	When DMA FIFO is underrun, this bit is used by firmware to toggle DIOR# signal.
DMACK#	rw	1	1'b1	When DMA FIFO is underrun, this bit is used by firmware to toggle DMACK# signal.
Flush/Abort	rw	0	1'b0	When DMA FIFO is overrun, this bit is used by firmware to flush data out for outgoing data or abort the DMA operation for incoming data. This bit is self-cleared by hardware.

6.2.13 Channel Clear Register (cmdCtl_Clr, 0x0B3)

Field name	rscu	bit #	reset	Description
Reserved	r	7	7'b0	Reserved
CmdTx4Run (for HID_out)	rwu	6	1'b0	When the Clear register is set by software, the corresponding channel is cleared.
CmdTx3Run (for CSW_out)	rwu	5	1'b0	When the Clear register is set by software, the corresponding channel is cleared.
Reserved	r	4	1'b0	Reserved
CmdTx1Run (for Control_out)	rwu	3	1'b0	When the Clear register is set by software, the corresponding channel is cleared.
Reserved	r	2	1'b0	Reserved
CmdTx1Run (for CBW)	rwu	1	1'b0	When the Clear register is set by software, the corresponding channel is cleared.
CmdTx1Run (for Setup-Packet)	rwu	0	1'b0	When the Clear register is set by software, the corresponding channel is cleared.

6.2.14 sgDma Control Register (sgCtl_Set, 0x0B4) (sgCtl_Clr, 0x0B5)

Field name	rscu	bit #	reset	Description
Reserved	r	7:1	7'b0	Reserved.
Sg0Run	rwu	0	1'b0	When Set register is set by software, the corresponding channel is ready to be transmitted. The hardware clears these bits when the transfer is completed. Software can set bit[3:0] on Clear register to clear the corresponding bit. When Clear register is written by software, the DMA channels will be reset to idle. (USB bulk transfer will only use sg0Run)

6.2.15 ATA Control register (AtaCtl, 0x0B6)

Field name	rscu	bit #	reset	Description
AtaDMAEn	rw	7	1'b1	When 1, ataDMA is enabled.
pioReq/pioGnt	rw	6	1'b0	Write 1 for PIO request. PIO grant status when read.
dmaMode	rw	5	1'b0	0-2: DMA mode 0 - 2
	rw	4	1'b0	4-7: UDMA mode 2, 3, 4 and 5 (up to uDMA100)
	rw	3	1'b0	
pioMode	rw	2	1'b0	0-4: PIO mode 0-4
	rw	1	1'b0	
	rwu	0	1'b0	

6.2.16 ATA Control/Status register (ataStatus, 0x0B7)

Field name	rscu	bit #	reset	Description
Reserved	rw	7	1'b	Reserved

			0	
AtaCh01En	rw	6	1'b0	Ata Channel 0 &1 Enable. When set, DMA write to channel 0 & 1 will be executed simultaneously.
PioXEn	rw	5	1'b0	PIO transfer engine enable. When set, the PIO engine will transfer data to/from the ATA bus using PIO transfer mechanism.
Reserved	r	4	1'b0	Reserved.
Reserved	ru	3	1'bx	Reserved
AtaIORDY0	ru	2	1'bx	Ata channel 0 IORDY line.
Reserved	ru	1	1'bx	Reserved
AtaINTRQ0	ru	0	1'bx	Ata channel 0 INTRQ line.

6.2.17 SPI_Ctrl/Status Register (0x0BD) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
StartCMD	w	7	1'b0	1: CPU write 1 to start the serial flash's command phase
reserved	r	6-5	2'b0	
StartWRSR	rw	4	1'b0	1: CPU write 1 to start the serial flash's Write_Status_Register action
reserved	r	3-2	2'b0	
SPI_WrDone	r	1	1'b0	Read only: CPU has send out the serial write command to serial flash. CPU may start sending out the read_status_command (RDSR) to serial flash to check the BUSY bit. When BUSY bit is 0, it means serial flash has finished the write operation.
SPI_RdDataRdy	r	0	1'b0	Read only: CPU has send out the serial read command to serial flash.

6.2.18 SPI_Data Register (0x0BE) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
SPI_Data	rw	7-0	8'h0	This is the data port for CPU to access aerial flash A: To Write to serial flash: CPU Writes to this port: CPU writes a 8-bit data to serial flash. B: To Read from serial flash: CPU reads this port: CPU does 1st Read: CPU activates the read action to fetch data from serial flash. CPU poll SPI_RdDataRdy (register BD bit 0) until it is 1 CPU does 2nd Read: to actually get the data.

6.2.19 SPI_CMD Register (0x0BF) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
SPI_CMD	rw	7-0	8'h0	CPU writes the to-be excuted SPI_command code in this register. For example: SPI_read has a command code: 03h

6.2.20 ATA_Status_Low Register (0x0D6)

Field name	rscu	bit #	reset	Description
ATA_Status[7:0]	rw	7-0	8'h0	CPU writes the ATA status to this register

6.2.21 ATA_Status_High Register (0x0D7)

Field name	rscu	bit #	reset	Description
ATA_Status[15:8]	rw	7-0	8'h0	CPU writes the ATA status to this register

6.2.22 usb_INT_Enable Register (0x0D8)

Field name	rscu	bit #	reset	Description
Usb_busRst_INT_En	rw	7	1'b0	1: Enable Usb_busRst to trigger sysINT.
Usb_bulkOnlyRst_INT_En	rw	6	1'b0	1: Enable Usb_bulkOnlyRst to trigger sysINT.
Usb_Ep0Req_INT_En	rw	5	1'b0	1: Enable Usb_ Ep0Req to trigger sysINT.
Usb_CBW_INT_En	rw	4	1'b0	1: Enable Usb_CBW to trigger sysINT.
Usb_wakeup_INT_En	rw	3	1'b0	1: Enable Usb_wakeup to trigger sysINT.
Usb_suspendINT_En	rw	2	1'b0	1: Enable Usb_suspend to trigger sysINT.
VBUS_P__INT_En	rw	1	1'b0	1: Enable positive of VBUS to trigger sysINT.
VBUS_N__INT_En	rw	0	1'b0	1: Enable negative of VBUS to trigger sysINT.

6.2.23 usb_INT_Status/Clear Register (0x0D9)

Field name	rscu	bit #	reset	Description
Usb_busRst	rw	7	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
Usb_bulkOnlyRst	rw	6	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit.
Usb_Ep0Req	rw	5	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
Usb_CBW	rw	4	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
Usb_wakeup	rw	3	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
Usb_suspend	rw	2	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
VBUS_P__INT	rw	1	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit
VBUS_N__INT	rw	0	1'b0	Read: 1: indicates this interrupt event occurred Write 1: will clear this status bit

6.2.24 GPIOA_INT_Enable Register (0x0DC)

Field name	rscu	bit #	reset	Description
GPIOA7_N_INTEn	rw	5	1'b0	1: Enable negative level of GPIOA7In to trigger sysINT.
GPIOA6_N_INTEn	rw	5	1'b0	1: Enable negative level of GPIOA6In to trigger sysINT.
GPIOA5_N_INTEn	rw	5	1'b0	1: Enable negative level of GPIOA5In to trigger sysINT.
GPIOA4_N_INTEn	rw	4	1'b0	1: Enable negative level of GPIOA4In to trigger sysINT.
GPIOA3_N_INTEn	rw	3	1'b0	1: Enable negative level of GPIOA3In to trigger sysINT.
GPIOA2_N_INTEn	rw	2	1'b0	1: Enable negative level of GPIOA2In to trigger sysINT.
GPIOA1_N_INTEn	rw	1	1'b0	1: Enable negative level of GPIOA1In to trigger sysINT.
GPIOA7_P_INT_En	rw	0	1'b0	1: Enable positive level of GPIOA7In to trigger sysINT.

6.2.25 SPI_ADR[7:0] Register (0x0DD) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
SPI_ADR[7:0]	rw	7-0	8'h0	CPU writes the to-be executed SPI_ADR[7:0] code in this register.

6.2.26 SPI_ADR[15:8] Register (0x0DE) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
SPI_ADR[15:8]	rw	7-0	8'h0	CPU writes the to-be executed SPI_ADR[15:8] code in this register.

6.2.27 SPI_ADR[23:16] Register (0x0DF) (for SPI-Serial Flash only)

Field name	rscu	bit #	reset	Description
SPI_ADR[23:16]	rw	7-0	8'h0	CPU writes the to-be executed SPI_ADR[23:16] code in this register.

6.2.28 GPIOA_H Enable Register (0x0EC)

Field name	rscu	bit #	reset	Description
Reserved	r	7	1'b0	reserved
GPIOB_En	rw	6	1'b0	1: Enable GPIOB group
GPIOC_En	rw	5	1'b0	1: Enable GPIOC group
GPIOD_En	rw	4	1'b0	1: Enable GPIOD group
GPIOE_En	rw	3	1'b0	1: Enable GPIOE group

GPIOF_En	rw	2	1'b0	1: Enable GPIOF group
Reserved	r	1	1'b0	reserved
Reserved	r	0	1'b0	reserved

6.2.29 GPIOB Data Register (0x0F2)

Field name	rscu	bit #	Reset	Description
GPIOA_Data[7:0]	rw	7-0	8'b0	Write: GPIOB_Dout[7:0] Read: GPIOB_Din[7:0]

6.2.30 GPIOB Ctrl Register (0x0F3)

Field name	rscu	bit #	Reset	Description
GPIOB_Ctrl[7:0]	rw	7-0	8'b0	1: Enable output buffer for the corresponding GPIO bit

6.2.31 GPIOC Data Register (0x0F4)

Field name	rscu	bit #	reset	Description
GPIOC_Data[7:0]	rw	7-0	8'b0	Write: GPIOC_Dout[7:0] Read: GPIOC_Din[7:0]

6.2.32 GPIOC Ctrl Register (0x0F5)

Field name	rscu	bit #	reset	Description
GPIOC_Ctrl[7:0]	rw	7-0	8'b0	1: Enable output buffer for the corresponding GPIO bit

6.2.33 GPIOD Data Register (0x0F6)

Field name	rscu	bit #	reset	Description
GPIOD_Data[7:0]	rw	7-0	8'b0	Write: GPIOD_Dout[7:0] Read: GPIOD_Din[7:0]

6.2.34 GPIOD Ctrl Register (0x0F7)

Field name	rscu	bit #	reset	Description
GPIOD_Ctrl[7:0]	rw	7-0	8'b0	1: Enable output buffer for the corresponding GPIO bit

6.2.35 GPIOE Data Register (0x0F8)

Field name	rscu	bit #	reset	Description
GPIOE_Data[7:0]	rw	7-0	8'b0	Write: GPIOE_Dout[7:0] Read: GPIOE_Din[7:0]

6.2.36 GPIOE Ctrl Register (0x0F9)

Field name	rscu	bit #	reset	Description
GPIOE_Ctrl[7:0]	rw	7-0	8'b0	1: Enable output buffer for the corresponding GPIO bit

6.2.37 GPIOF Data Register (0x0FA)

Field name	rscu	bit #	reset	Description
GPIOF_Data[7:0]	rw	7-0	8'b0	Write: GPIOF_Dout[7:0] Read: GPIOF_Din[7:0]

6.2.38 GPIOF Ctrl Register (0x0FB)

Field name	rscu	bit #	reset	Description
GPIOF_Ctrl[7:0]	rw	7-0	8'b0	1: Enable output buffer for the corresponding GPIO bit

7. Electrical Information:

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
Vcc	Power Supply	-0.3	3.6	V
Vin	Input Voltage	-0.3	Vcc+0.3	V
Vout	Output Voltage	-0.3	Vcc+0.3	V
Tstg	Storage Temperature	-55	150	°C

7.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input Voltage	0	-	Vcc	V
Tj	Commercial Junction Operating Temperature	0	25	115	°C
	Industrial Junction Operation Temperature	-40	25	125	°C

7.3 General DC Characteristics

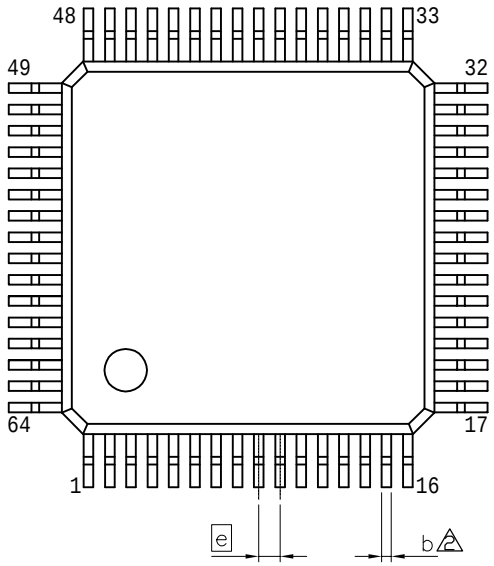
Symbol	Parameter	Min	Typ	Max	Units
Iil	Input Leakage Current	-1		1	μA
Ioz	Tristate Leakage Current	-1		1	μA
Cin	Input Capacitance		2.8		pF
Cout	Output Capacitance	2.7		4.9	pF
Cbid	Bi-directional Buffer Capacitance	2.7		4.9	pF

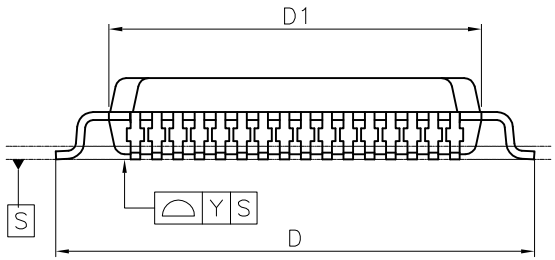
7.4 DC Electrical Characteristics for 3.3V Operation

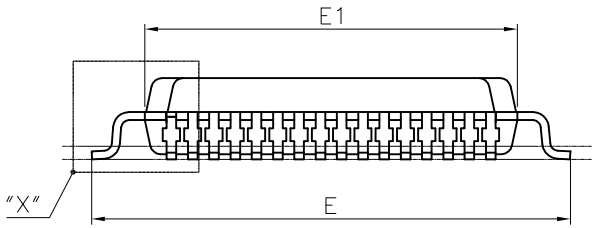
(Under Vcc=3.0-3.6V, Tj=0-115C)

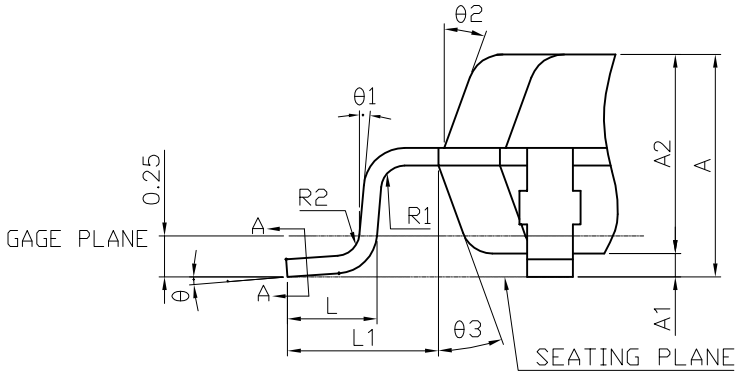
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input Low Voltage	CMOS			0.3*Vcc	V
		CMOS Schmitt Trigger		1.20	0.3*Vcc	V
Vih	Input High Voltage	CMOS	0.7*Vcc			V
		CMOS Schmitt Trigger		2.10		V
Vol	Output Low Voltage	Ioh-2-24mA			0.4	V
Voh	Output High Voltage	Ioh=2-24mA	2.4			V
Ri	Input Pullup/pulldown Resistance	Vil=0/Vih=Vcc		75		kΩ
Icc	Operating Supply Current	Vcc=3.3V		50	70	mA

8. Packaging Specification

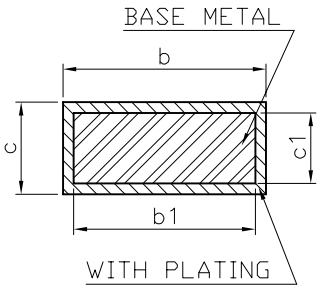








DETAIL "X"



SECTION A-A

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.40 BSC			15.8 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE C)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

REV.	DESCRIPTION	PAGE	DATE	
2	Modify the dimension value	1~1	2005-09-12	I

	PKG. CODE	DRAWING NUMBER	REV.
	T151	3388-010-0061	2

SIZE	A3		DATE
DRAWN			2005.09.12
DESIGNED			
CHECKED			2005.09.12
APPROVED			2005.09.12

TITLE: LQFP64 (7x7x1.4mm) PACKAGE OUTLINE Footprint 2.0mm

SCALE: 10 : 1 | SHEET: 1 OF 1 | PROJ.