# AKD4425A-SA

## AK4425A Evaluation Board Rev.0

### General Description

AKD4425A-SA is an evaluation board for AK4425A (192kHz sampling 24Bit Stereo ΔΣ DAC with 2Vrms Output). AKD4425A-SA has a digital audio interface (AK4118) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4425A.

■ **Ordering Guide**

AKD4425A-SA ---- AK4425A Evaluation Board

### Function

- **Compatible with 2 types of interface**
  **DIR with optical input and BNC input**
  **Direct interface with 10pin header**
- **BNC connector for Analog Output**

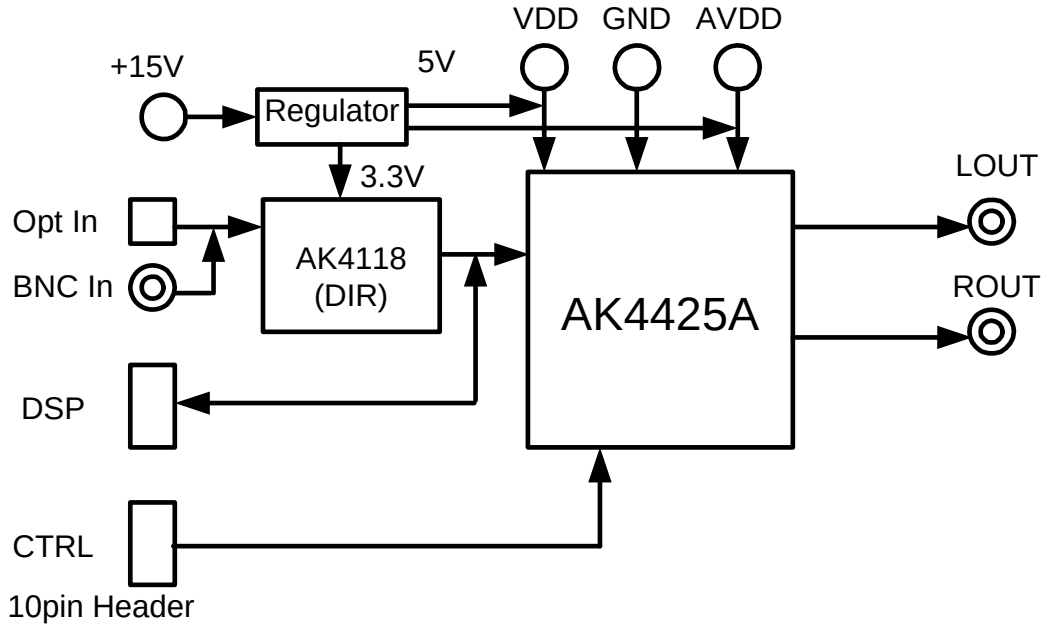


Figure 1. AKD4425A-SA Block diagram
(* Circuit diagram are attached at the end of this manual.)

## ■ Operation sequence

1) Set up the power supply lines.
Each supply line should be distributed from the power supply unit.

| Name of jack | Color of jack | Voltage Range | Using | Default Setting | Default |
|---|---|---|---|---|---|
| +15V | Red | +7~+20V | Regulator :<br>VDD and AVDD for AK4425A.<br>The power supply for AK4118, 74LVC541 and other logic circuit. | Should be connected. | +15V |
| VDD | Orange | +4.5~+5.5V | VDD of AK4425A | Should be connected.<br>(Default, Note1) | +5V |
| AVDD | Orange | +4.5~+5.5V | AVDD of AK4425A | Should be connected.<br>(Default, Note2) | +5V |
| GND | Black | 0V | Ground | Should be connected. | 0V |

Table 1. Set up of power supply lines

Note 1 ) VDD for AK4425A can supply to connect Regulator. In this case, should be to "short" of R58 and no connected "VDD" of jack.
Note 2 ) AVDD for AK4425A can supply to connect Regulator. In this case, should be to "short" of R59 and no connected "AVDD" of jack.

2) DIP Switch setting:
Refer to Table 2, Table 3 and Table 4.

3) Power Down:
The AK4118 should be reset once by bringing SW2 (AK4118 PDN) "L" upon power-up.

## ■ Evaluation mode

1. Using DIR (COAX) (Default)
The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4425A by using CD disk. Should be no connected to PORT1 (DSP).
Setting: R41: short (0Ω) ; R42: open
＊ COAX is recommended for an evaluation of the Sound quality.

2. Using DIR (Optical Link)
The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT2: TORX141). It is possible to evaluate the AK4425A by using CD disk. Should be no connected to PORT1 (DSP).
Setting: R41: open ; R42: short (0Ω)

3. Supply all interface signals that includ master clock via PORT1 from external equipments..
Setting: R43, R44, R45, R46: open
R47, R48, R49, R50: short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

## ■ Setting of DIP switch

[S1]: AK4118 setting (ON = "H", OFF = "L")

| No. | Pin | OFF | ON | Default |
|---|---|---|---|---|
| 1 | DIF1 | AK4118's Audio Data Format setting | | L |
| 2 | DIF0 | Refer to Table 3 | | L |
| 3 | OCKS1 | AK4118's Master Clock setting | | H |
| 4 | OCKS0 | Refer to Table 4 | | L |

Table 2. S1 setting

| Mode | DIF2 | DIF1 | DIF0 | SDTO | |
|---|---|---|---|---|---|
| 4 | H | L | L | 24bit, Left justified | Default |
| 5 | | L | H | 24bit, $I^2S$ | |

Table 3. Audio Data Format setting

| OCKS1 | OCKS0 | MCKO1 | fs (max.) | |
|---|---|---|---|---|
| L | L | 256fs | 96kHz | |
| H | L | 512fs | 48kHz | Default |
| H | H | 128fs | 192kHz | |

Table 4. MCLK clock setting

## ■ Setting of SW1 and SW2 switch

[SW1](SMUTE): Don't use. SW1 must be always "L".

[SW2](PDN): Reset of AK4118. Keep "H" during normal operation.

## ■ Serial Control (I²C-bus Control Mode)

The AK4425A can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (CTRL) with PC by 10 wire flat cable packed with the AKD4425A-SA

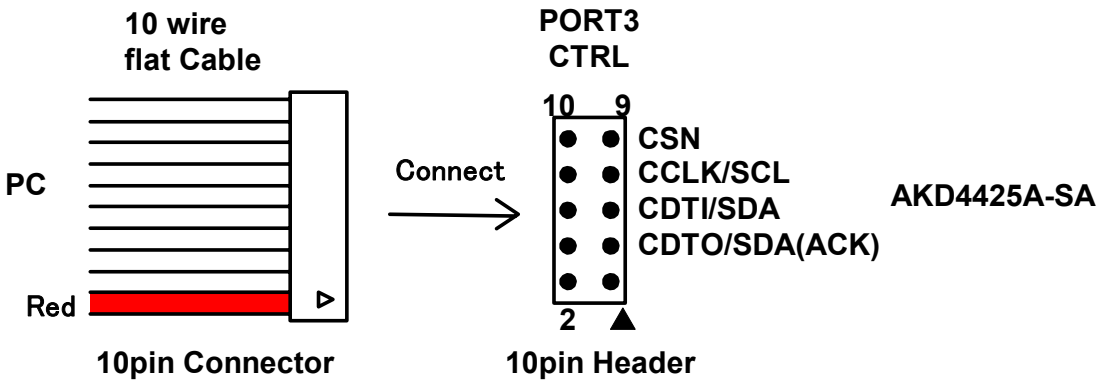


Figure 2. Connect of 10 wire flat cable

## ■ Analog Output Circuit

AOUTL and AOUTR pins are outputted from J1 (LOUT) and J2 (ROUT).

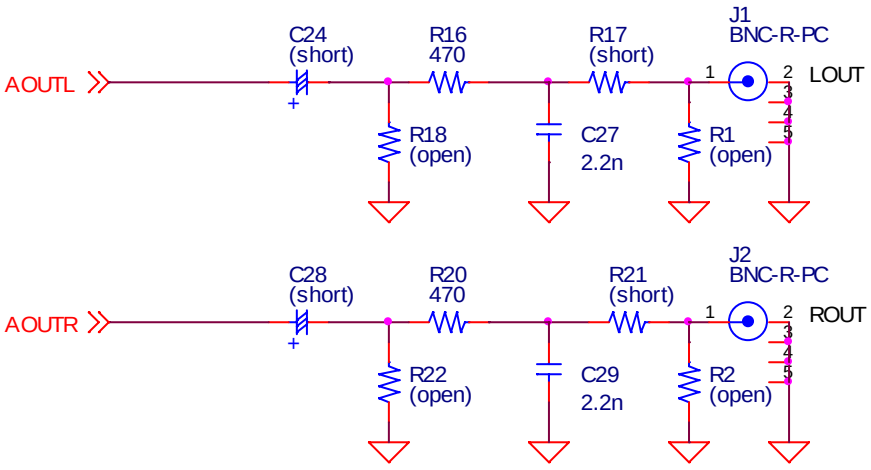


Figure 3. AOUTL / AOUTR Output Circuit

∗ AKM assumes no responsibility for the trouble when using the above circuit examples.

# Control Soft Manual

## ■ Evaluation Board and Control Soft Settings

1. Set an evaluation board properly.
2. Connect the evaluation board to an IBM PC/AT compatible PC by a 10wire flat cable. Be aware of the direction of the 10pin header. When running this control soft on the Windows 2000/XP, the driver which is included in the CD must be installed. Refer to the "Driver Control Install Manual for AKM Device Control Software" for installing the driver. When running this control soft on the windows 95/98/ME, driver installing is not necessary. This control soft does not support the Windows NT.
3. Proceed evaluation by following the process below.

## ■ Operation Screen

1. Start up the control program following the process above.

The operation screen is shown below.

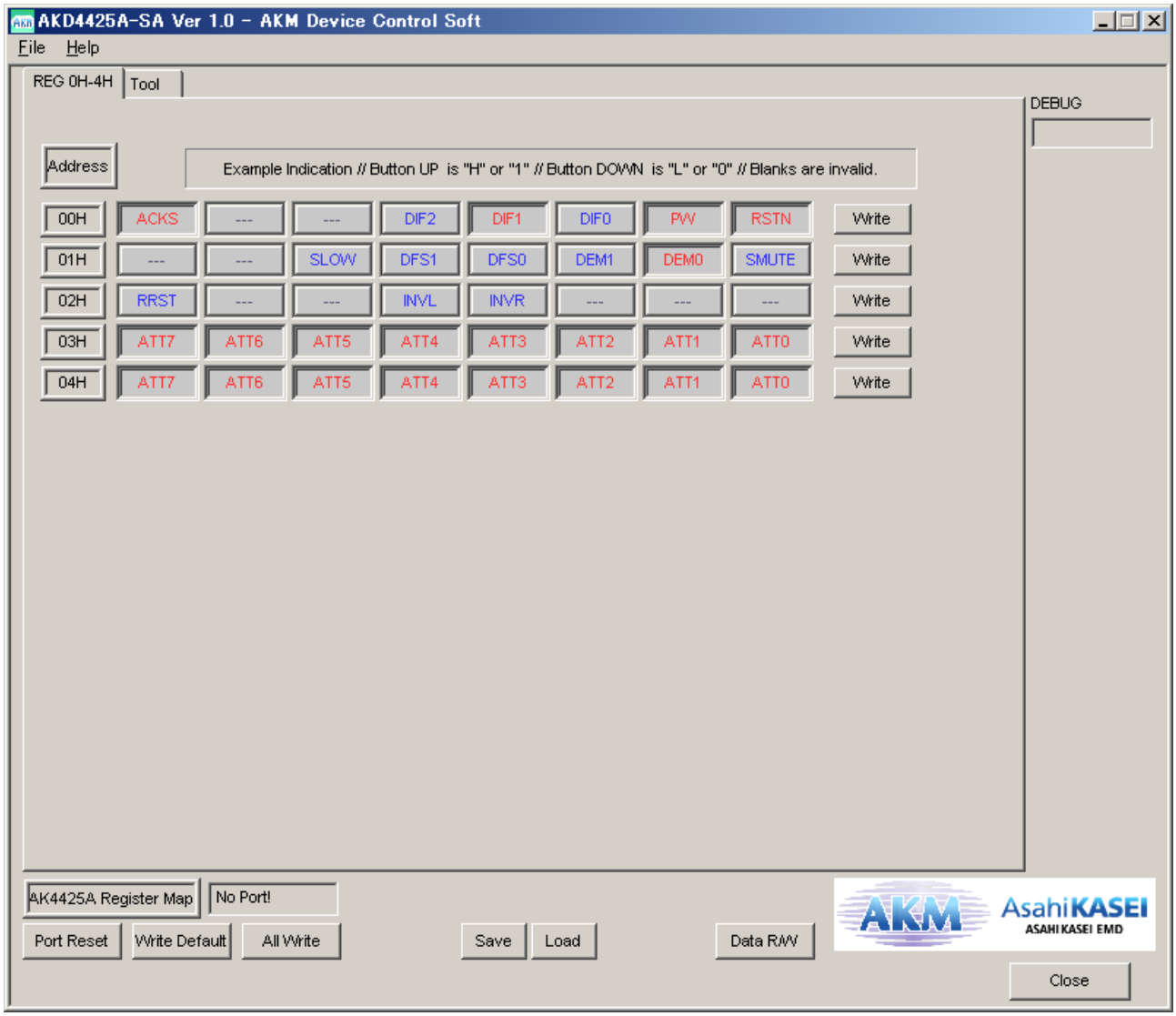


Figure 4. Window of [ FUNCTION]

## ■ Operation Overview

Function, register map and testing tool can be controlled by this control soft. These controls are selected by upper tabs.

Buttons which are frequently used such as register initializing button “Write Default”, are located outside of the switching tab window. Refer to the “■ Dialog Boxes” for details of each dialog box setting.

1. [Port Reset]: For when connecting to USB I/F board (AKDUSBIF-A)
   Click this button after the control soft starts up when connecting USB I/F board (AKDUSBIF-A).
2. [Write Default]: Register Initializing
   When the device is reset by a hardware reset, use this button to initialize the registers.
3. [All Write]: Executing write commands for all registers displayed.
4. [Save]: Saving current register settings to a file.
5. [Load]: Executing data write from a saved file.
6. [Data R/W]: “Data R/W” dialog box is popped up.

## ■ Tab Functions

### [Data R/W]

Click the [Data R/W] button in the main window for data read/write dialog box.
Data write is available to specified address.

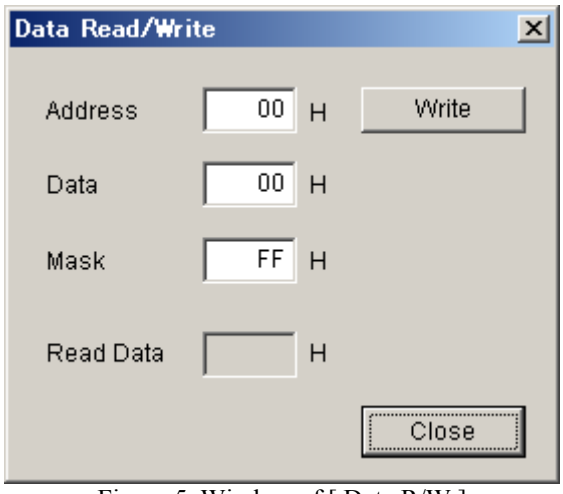


Figure 5. Window of [ Data R/W ]

Address Box : Input data address in hexadecimal numbers for data writing.
Data Box : Input data in hexadecimal numbers.
Mask Box : Input mask data in hexadecimal numbers.
This is “AND” processed input data.

[Write] : Writing to the address specified by “Address” box.
[Close] : Closing the dialog box and finish the process.
Data writing can be cancelled by this button instead of [Write] button.

*The register map will be updated after executing [Write] or [Read] commands.

## [REG]: Register Map

This tab is for a register writing and reading.

Each bit on the register map is a push-button switch.
Button Down indicates “H” or “1” and the bit name is in red (when read only it is in deep red).
Button Up indicates “L” or “0” and the bit name is in blue (when read only it is in gray)

Grayout registers are Read Only registers. They can not be controlled.

The registers which is not defined in the datasheet are indicated as “---”.

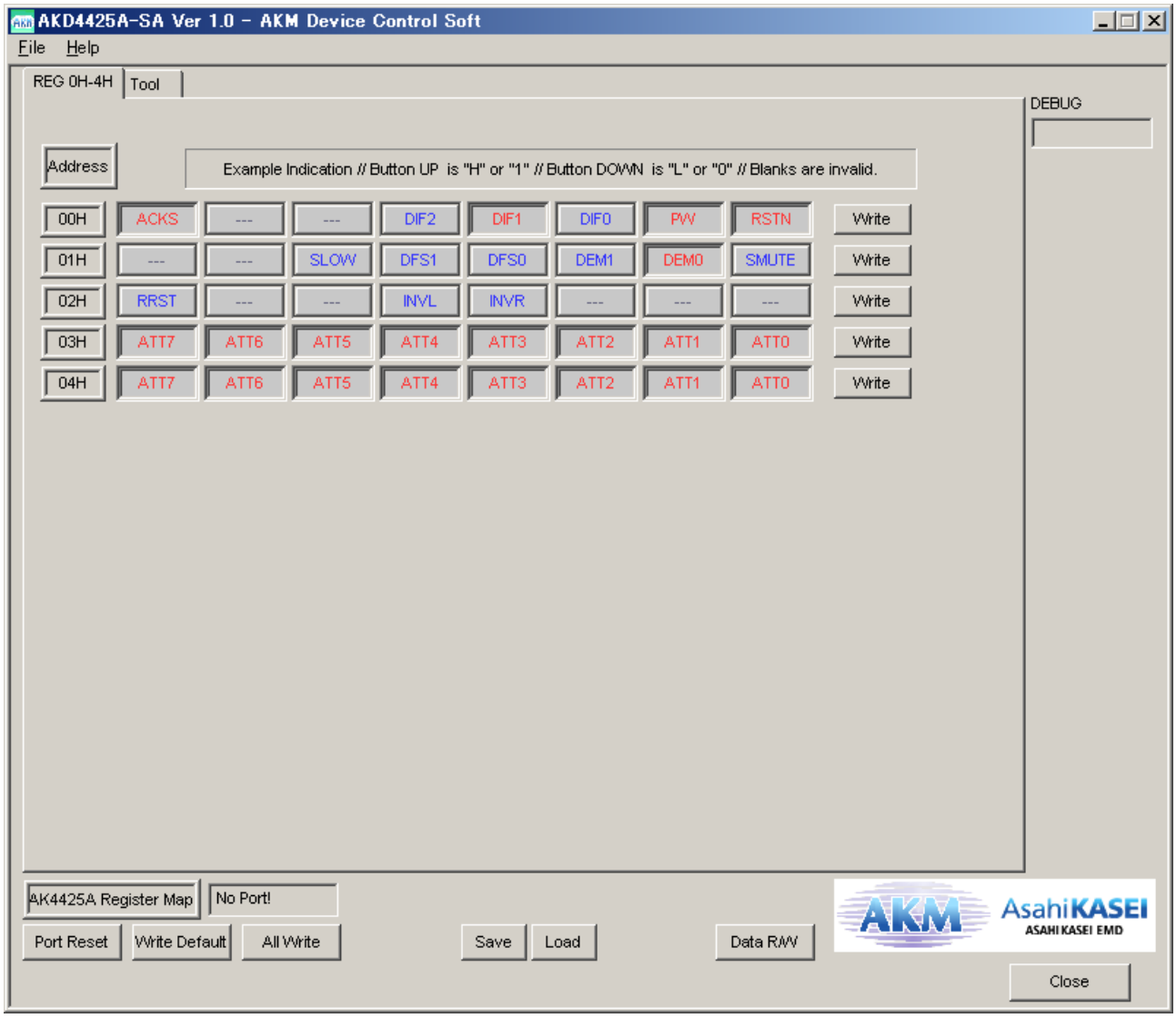


Figure 6. Window of [ REG]

### [Write]: Data Writing Dialog

It is for when changing two or more bits on the same address at the same time.

Click [Write] button located on the right of the each corresponded address for a pop-up dialog box.
When checking the checkbox, the register will be “H” or “1”, when not checking the register will be “L” or ”0”.
Click [OK] to write setting value to the registers, or click [Cancel] to cancel this setting.

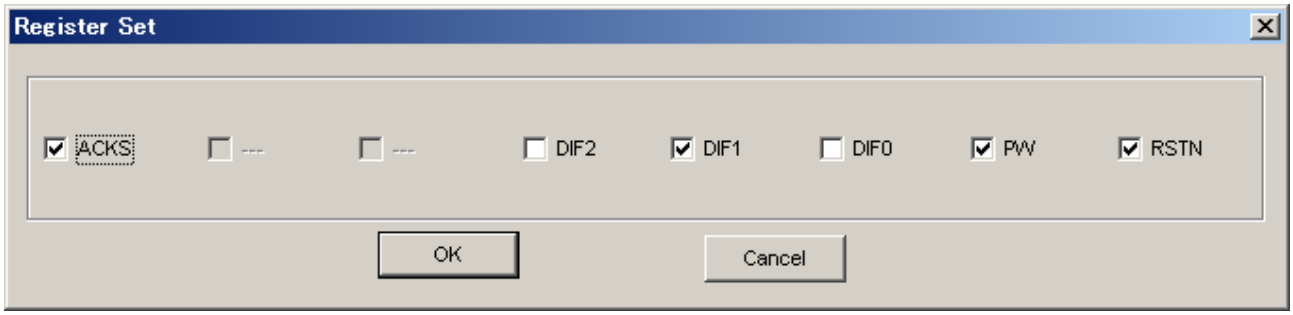


Figure 7. Window of [ Register Set ]

### [Tool]: Testing Tools

This tab screen is for evaluation testing tool.
Click buttons for each testing tool.

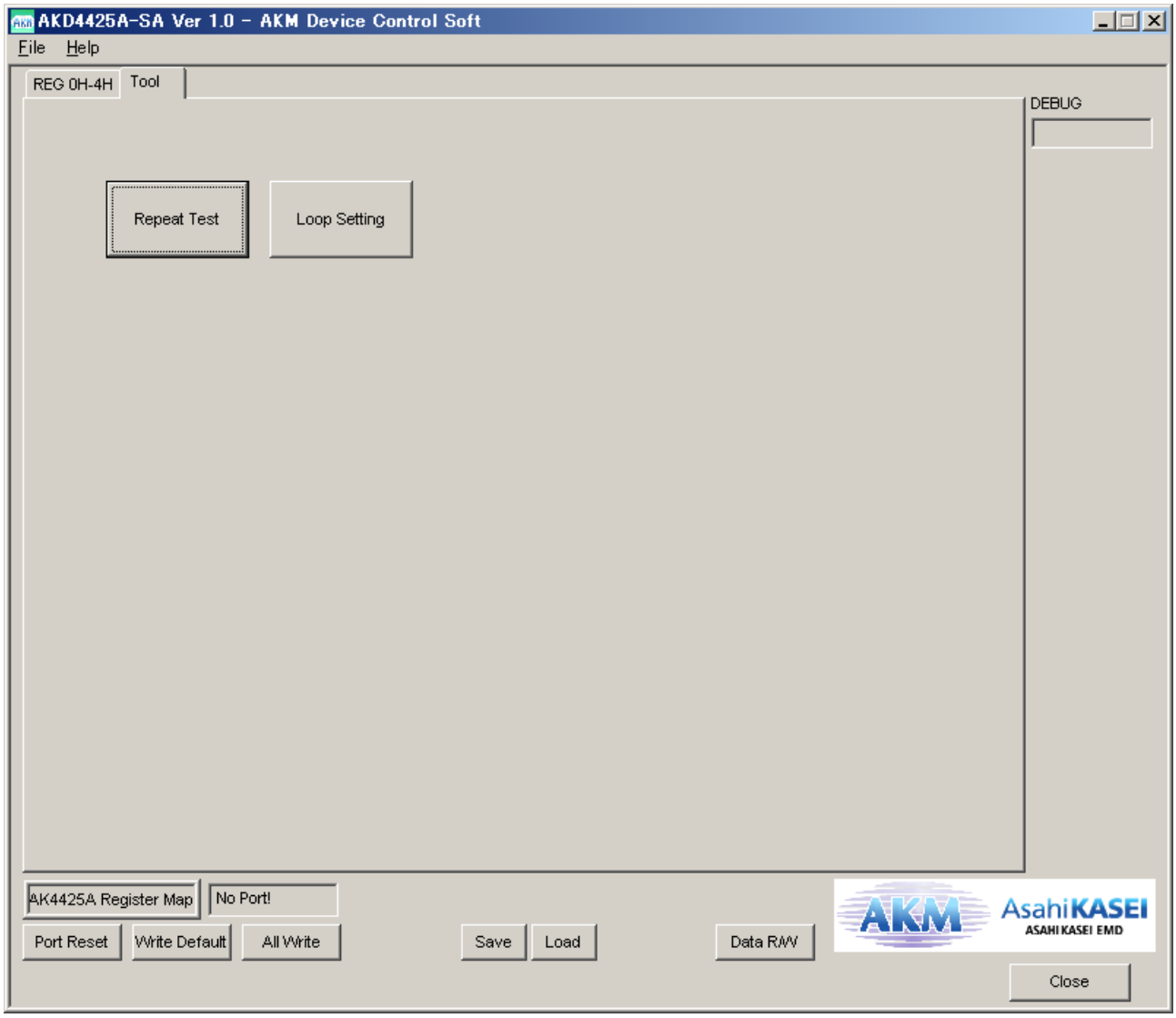


Figure 8. Window of [ Tool]

### [Repeat Test]: Repeat Test Dialog

Click [Repeat Test] button to open repeat test setting dialog box.

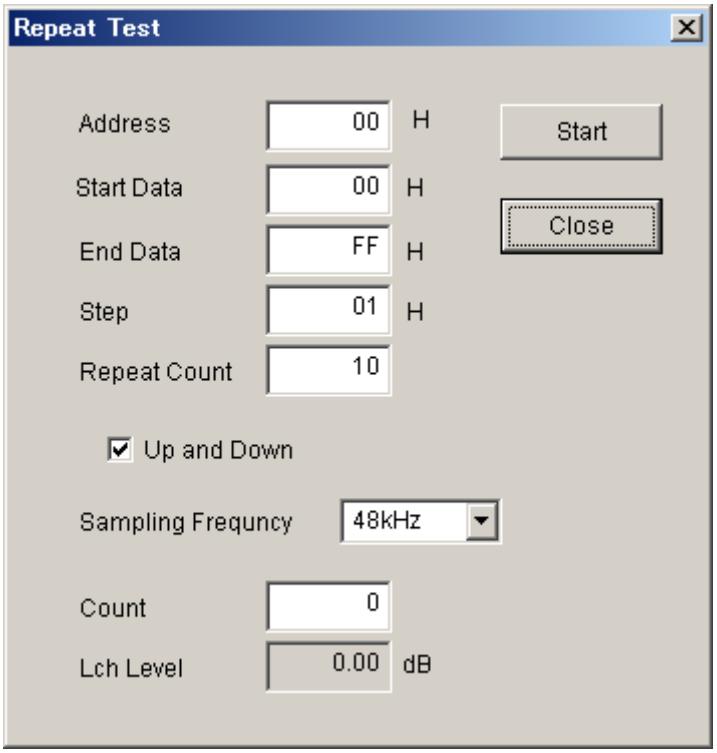


Figure 9. Window of [ Repeat Test]

### [Loop Setting]: Loop Setting Dialog

Click [Loop Setting] button to open loop setting dialog box.

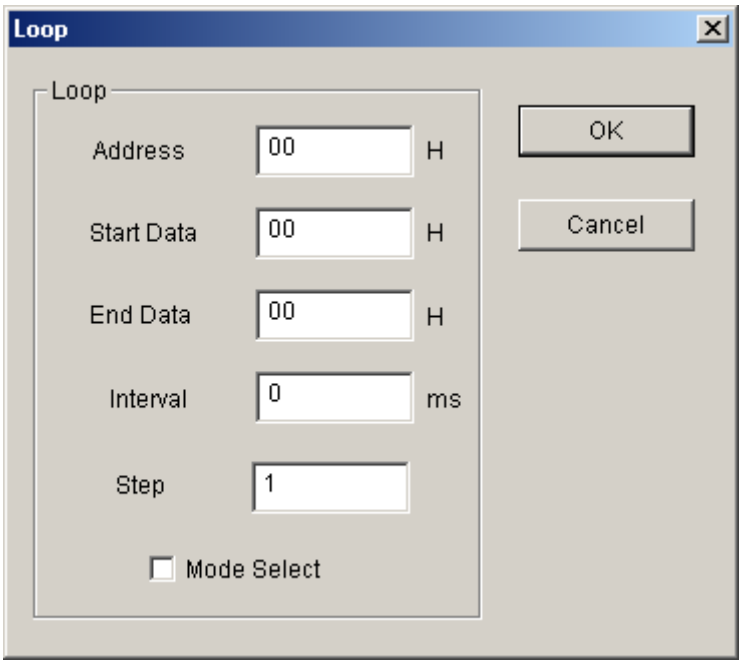


Figure 10. Window of [ Loop]

## Measurement Results

[Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (fs = 44.1kHz), 256fs (fs = 96kHz), 128fs (fs = 192kHz)
- BICK : 64fs
- fs : 44.1kHz, 96kHz, 192kHz
- Bit : 24bit
- Power Supply : VDD=AVDD=5V
- Interface : DIR
- Temperature : Room

### Table Data

fs=44.1kHz

| Parameter | Input signal | Filter condition | Lch | Rch | Unit |
|---|---|---|---|---|---|
| S/(N+D) | 1kHz, 0dB | 20kHz SPCL,<br>20kHz Brick-wall LPF | 91.6 | 91.1 | dB |
| DR | 1kHz, -60dB | 20kHz SPCL, A-weighted | 106.1 | 106.0 | dB |
| S/N | "0" data | 20kHz SPCL, A-weighted | 106.5 | 106.3 | dB |

fs=96kHz

| Parameter | Input signal | Filter condition | Lch | Rch | Unit |
|---|---|---|---|---|---|
| S/(N+D) | 1kHz, 0dB | 40kHz SPCL,<br>40kHz Brick-wall LPF | 91.6 | 91.1 | dB |
| DR | 1kHz, -60dB | 40kHz SPCL, A-weighted | 106.2 | 106.0 | dB |
| S/N | "0" data | 40kHz SPCL, A-weighted | 106.4 | 106.3 | dB |

fs=192kHz

| Parameter | Input signal | Filter condition | Lch | Rch | Unit |
|---|---|---|---|---|---|
| S/(N+D) | 1kHz, 0dB | 40kHz SPCL,<br>40kHz Brick-wall LPF | 91.5 | 91.0 | dB |
| DR | 1kHz, -60dB | 40kHz SPCL, A-weighted | 106.3 | 106.1 | dB |
| S/N | "0" data | 40kHz SPCL, A-weighted | 106.4 | 106.3 | dB |

**Plot Data**

**(1) fs = 44.1kHz (MCLK=512fs)**

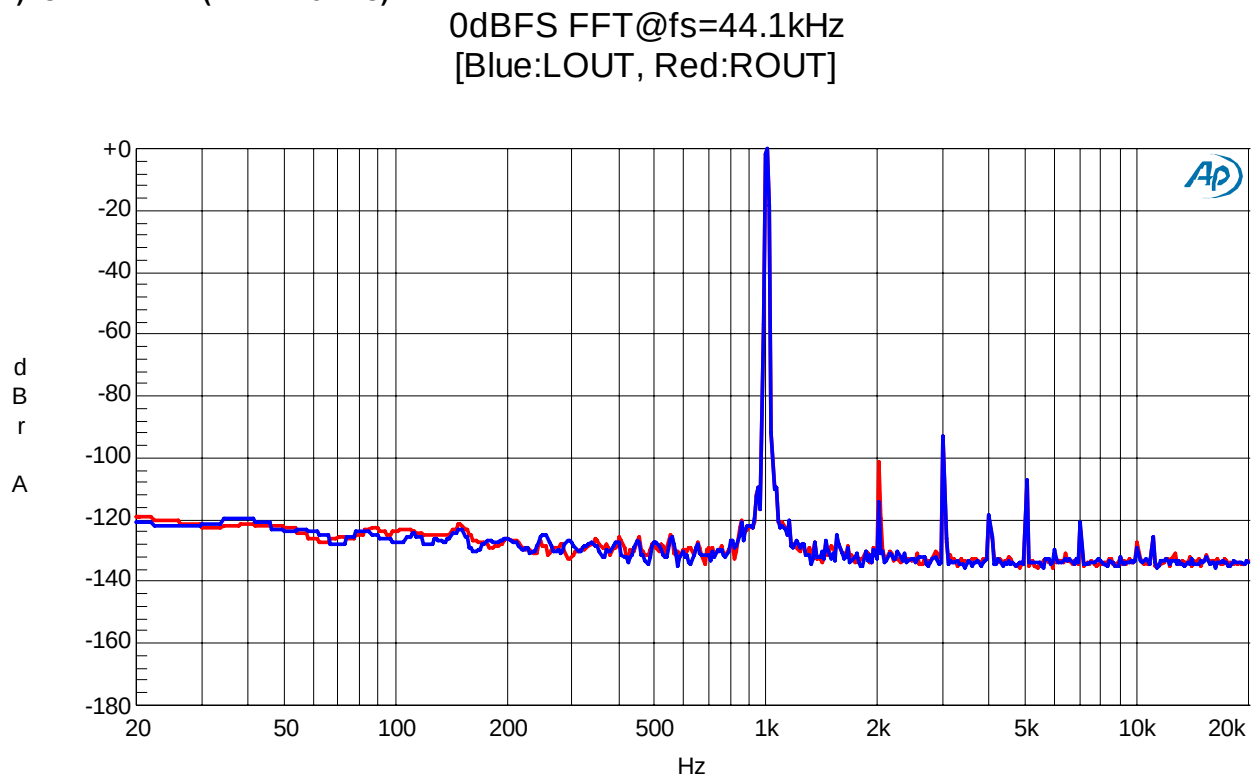


Figure 11. FFT (fin=1kHz, Input Level=0dBFS)

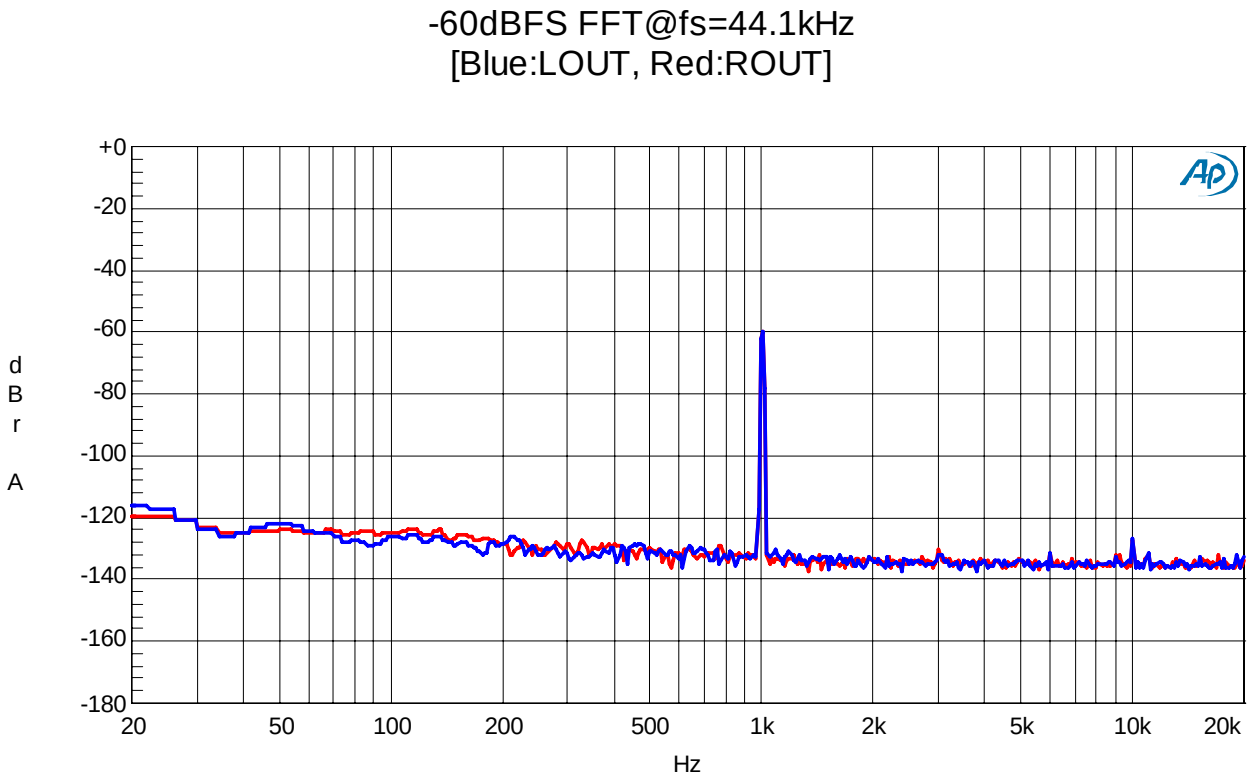


Figure 12. FFT (fin=1kHz, Input Level=-60dBFS)

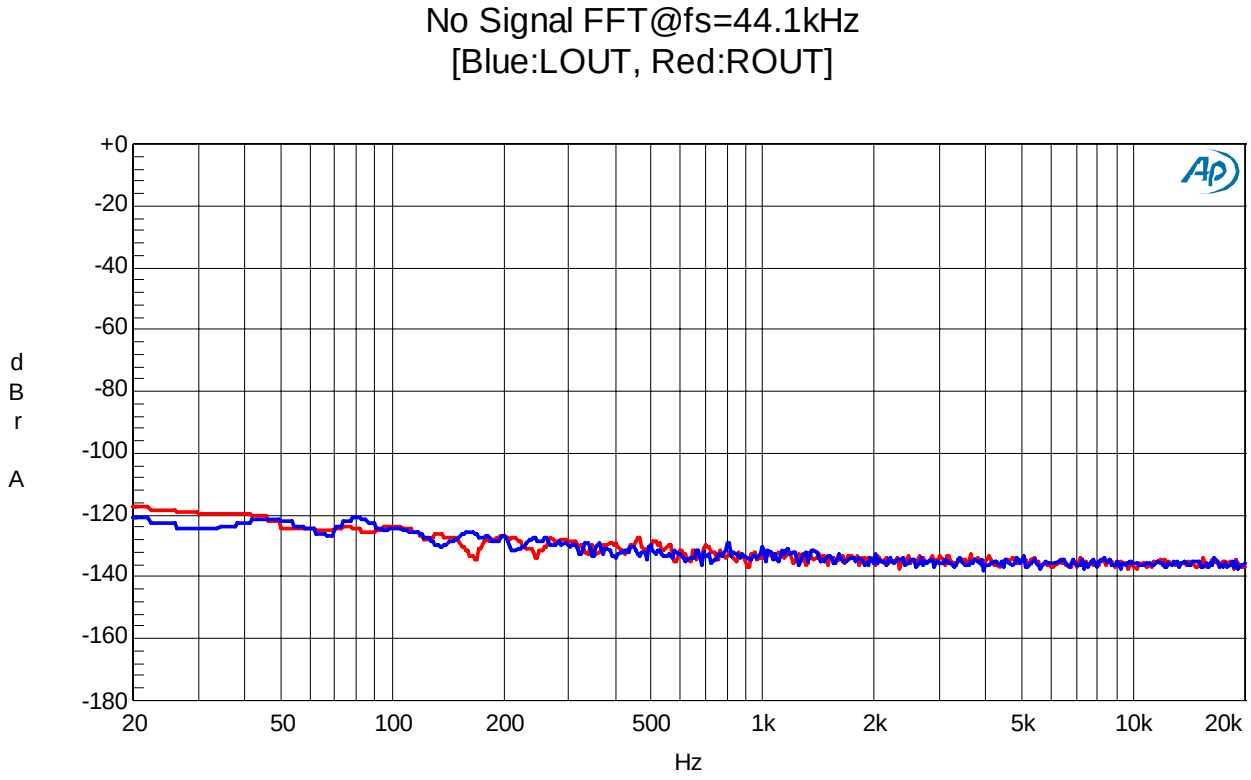


Figure 13. FFT (No Signal)

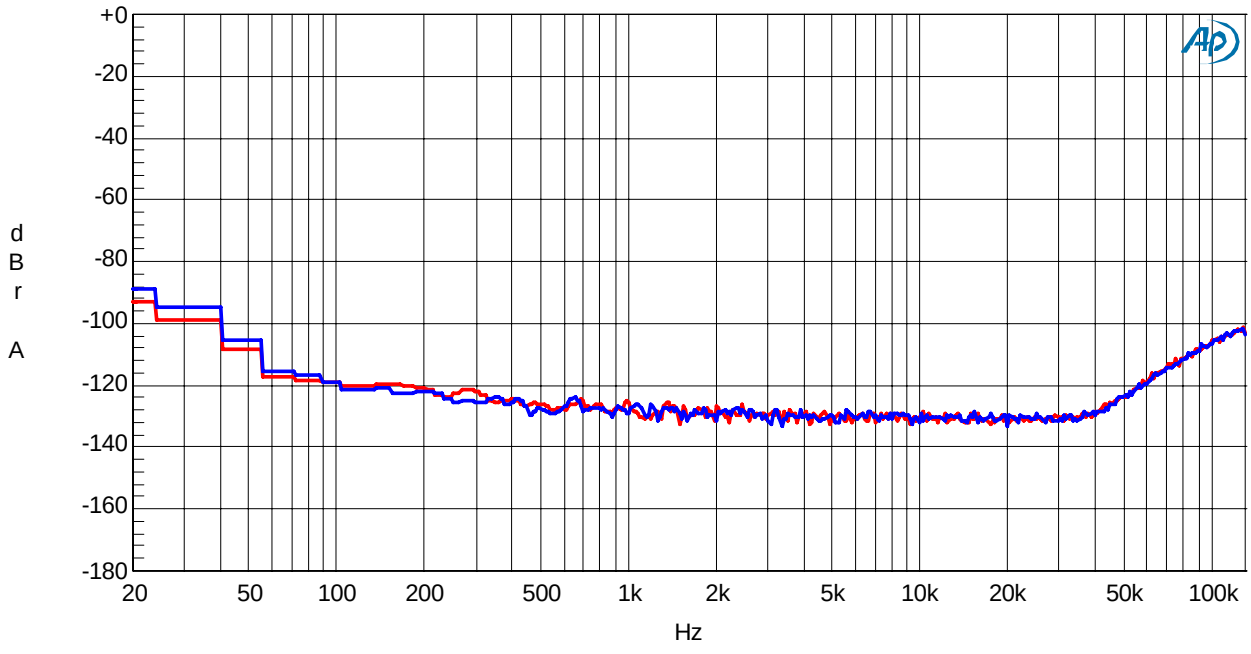


Figure 14. FFT (Out of band noise)

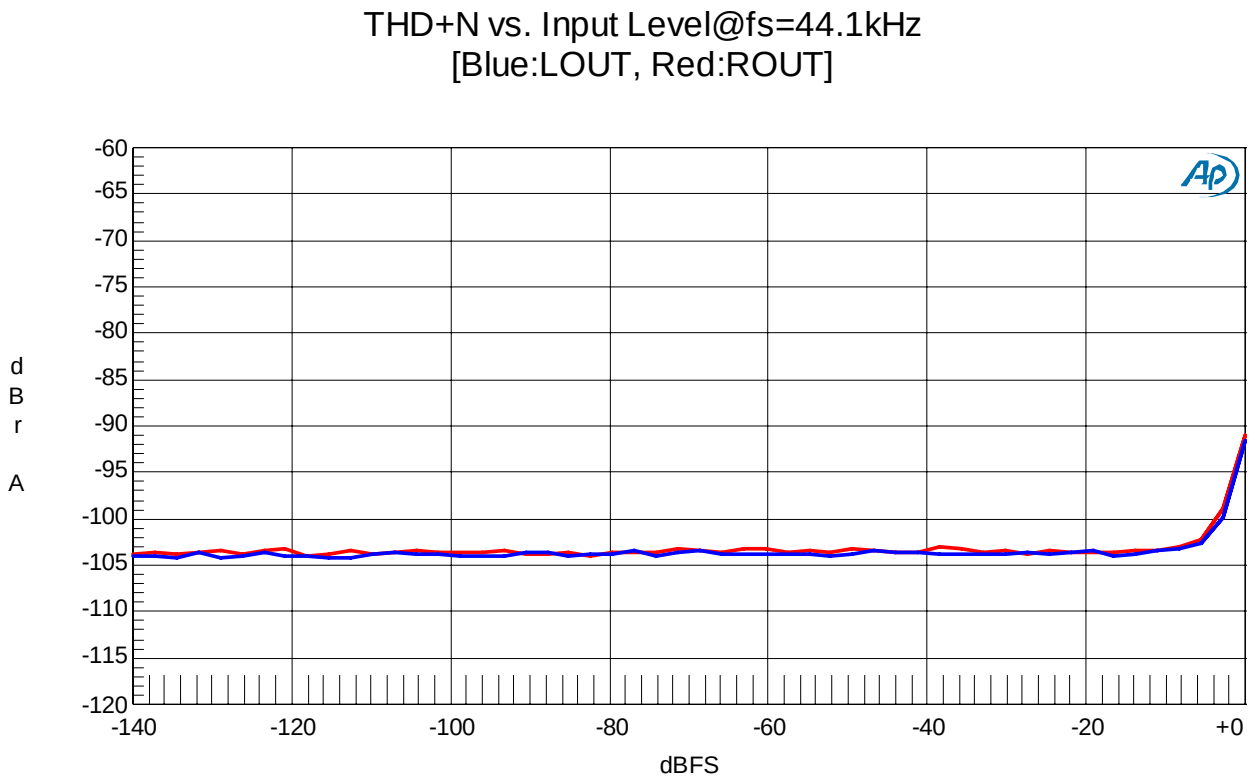


Figure 15. THD+N vs. Input level (fin=1kHz, 20kHz SPCL)

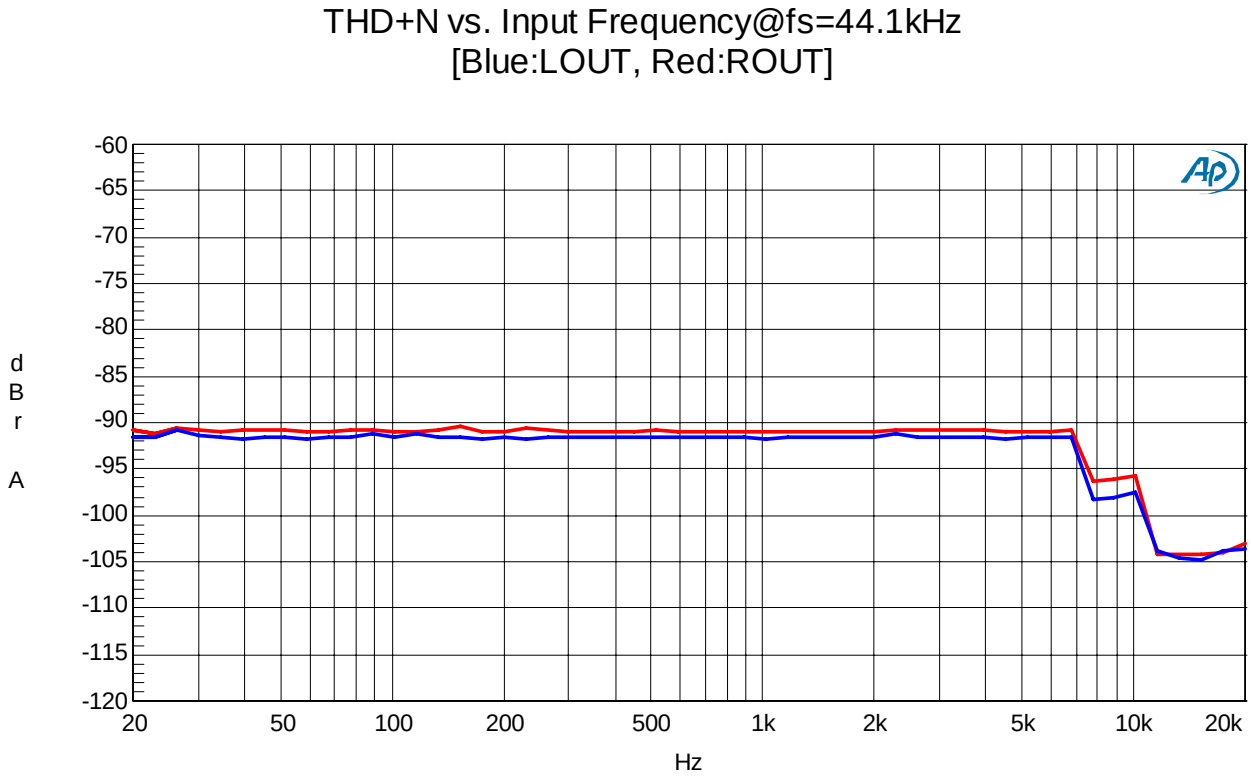


Figure 16. THD+N vs. Input Frequency (Input level=0dBFS, 20kHz SPCL)

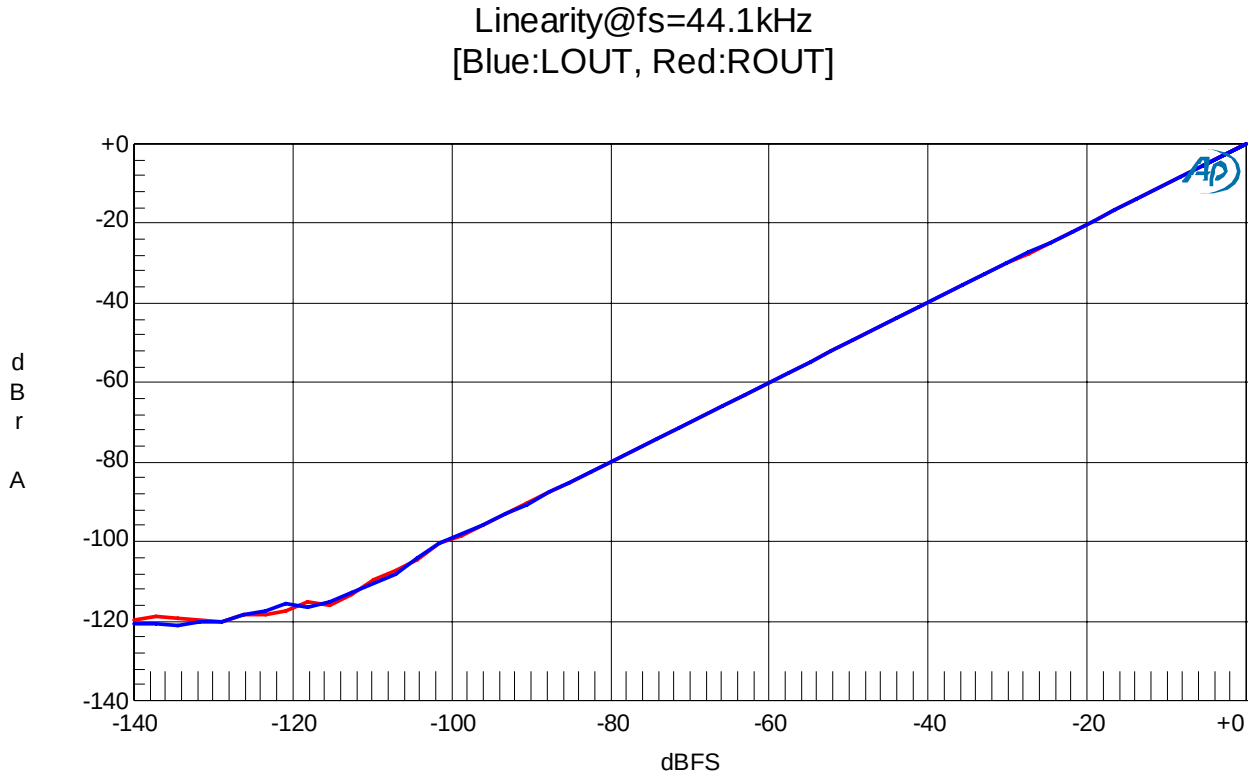


Figure 17. Linearity (fin=1kHz)

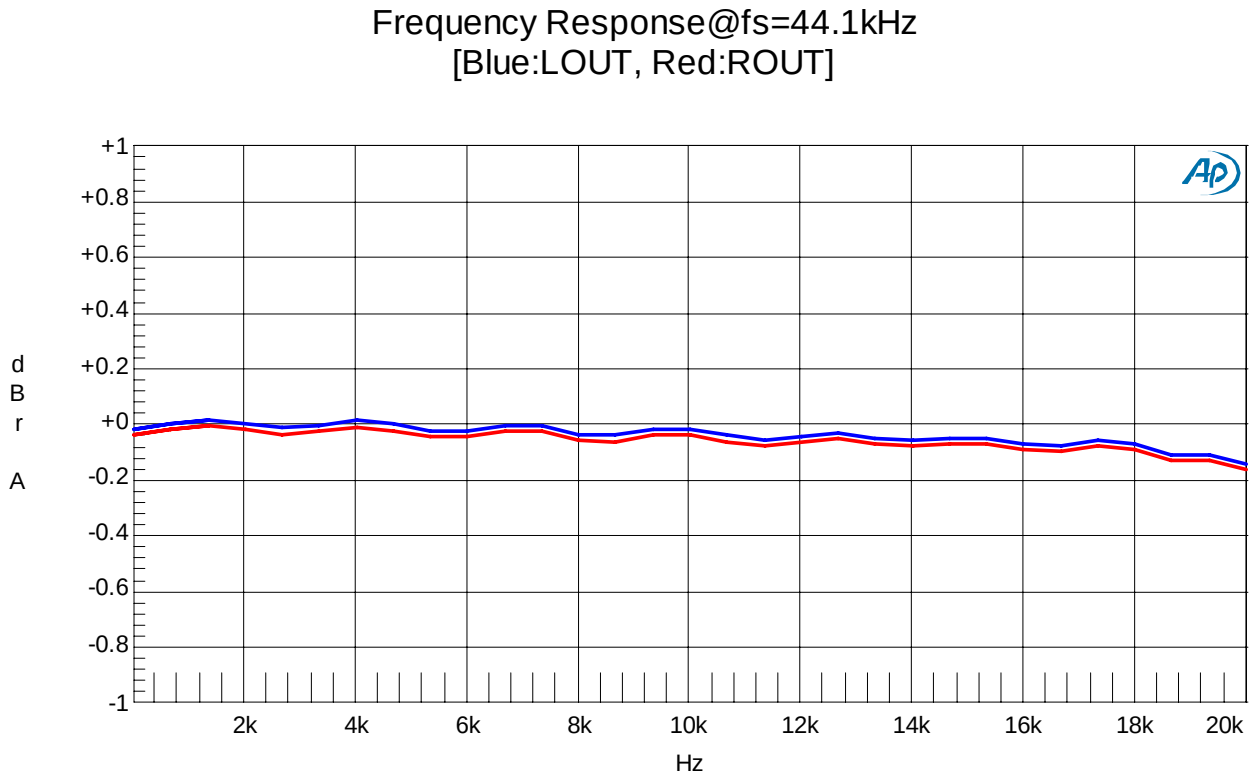


Figure 18. Frequency Response (Input level=0dBFS)

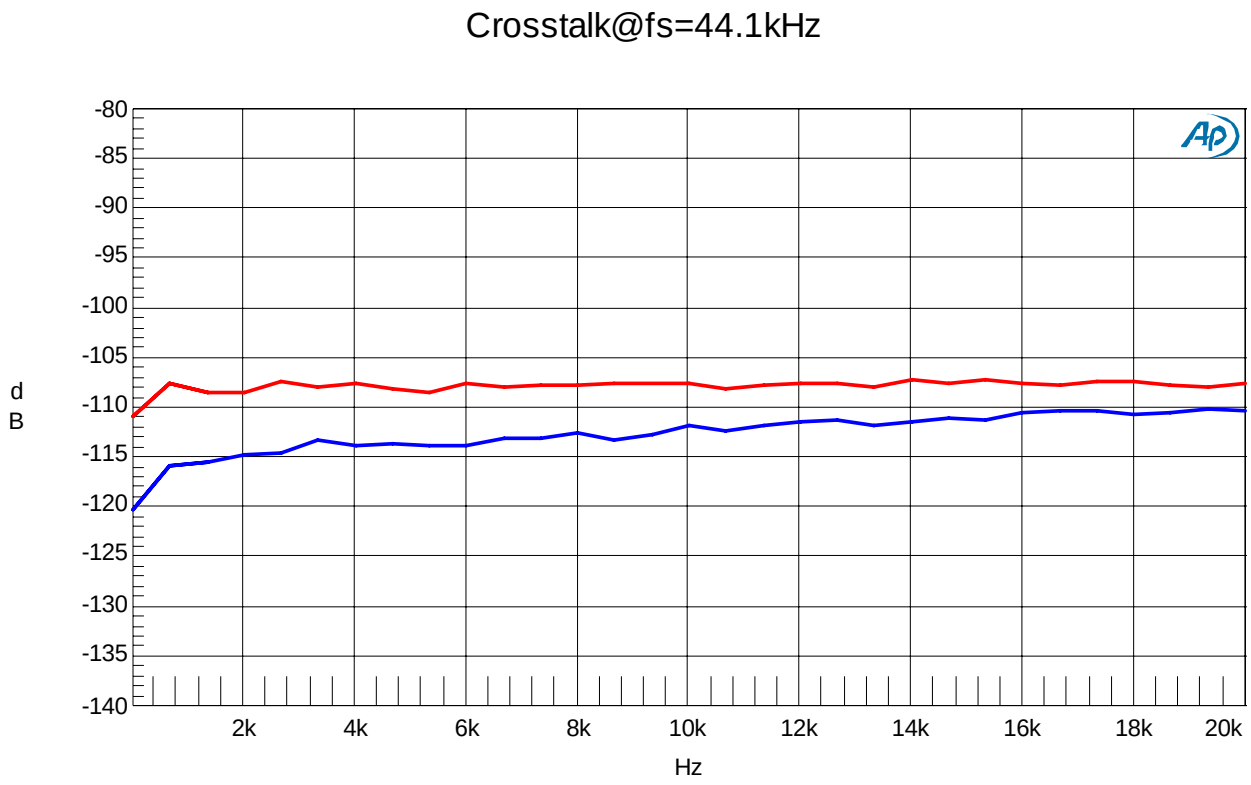


Figure 19. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

**(2) fs = 96kHz (MCLK=256fs)**

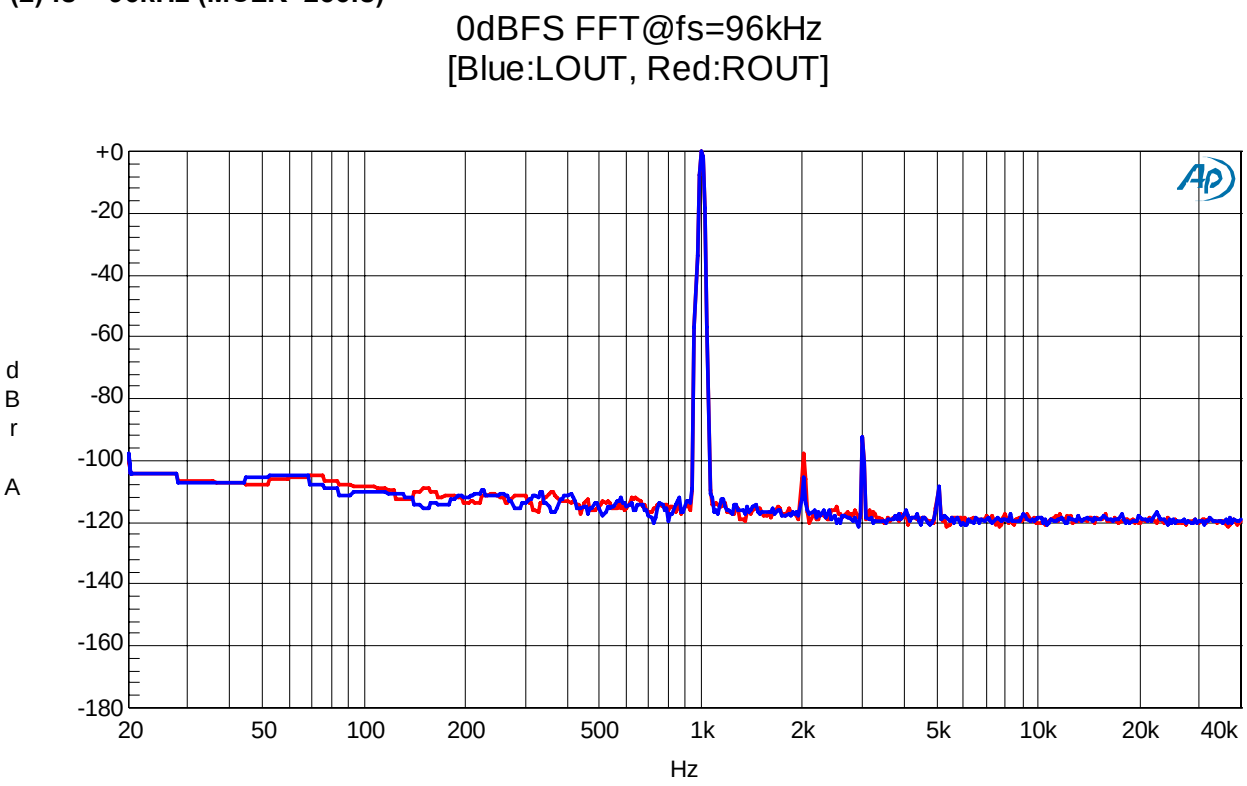


Figure 20. FFT (fin=1kHz, Input Level=0dBFS)

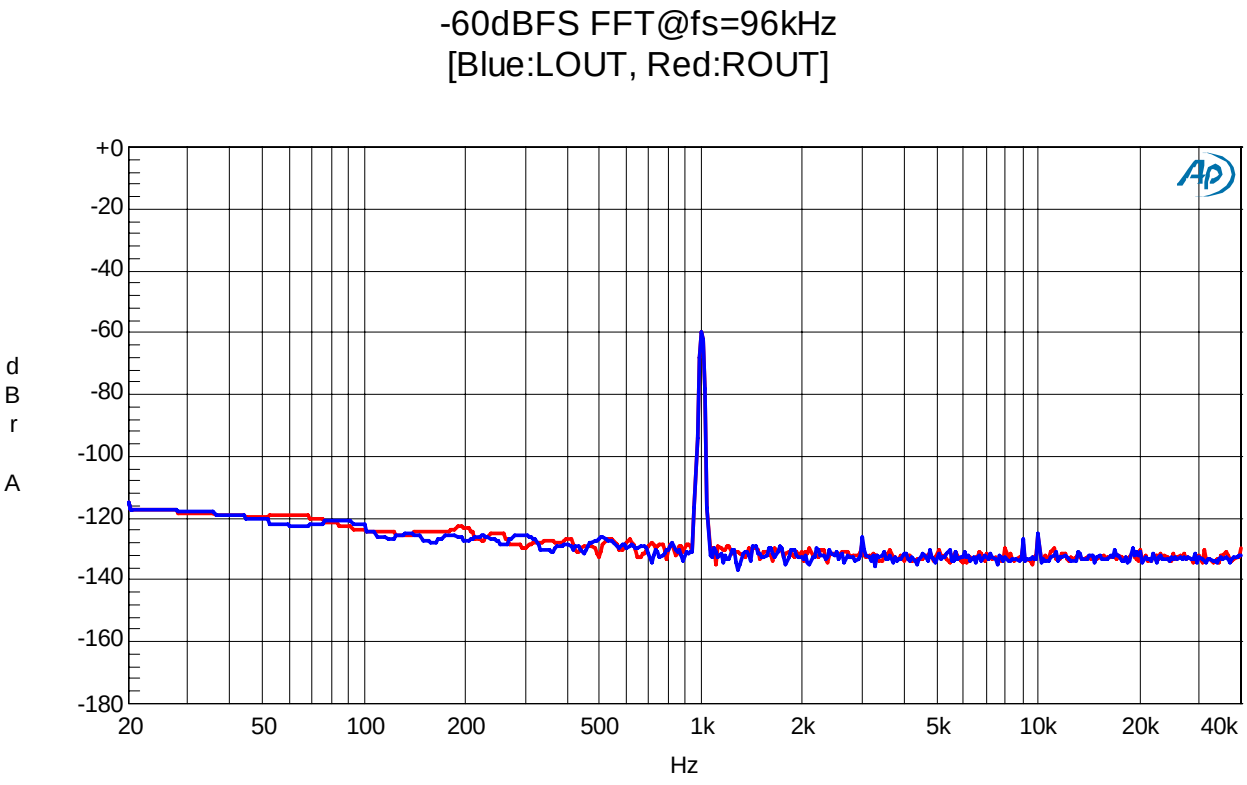


Figure 21. FFT (fin=1kHz, Input Level=-60dBFS)

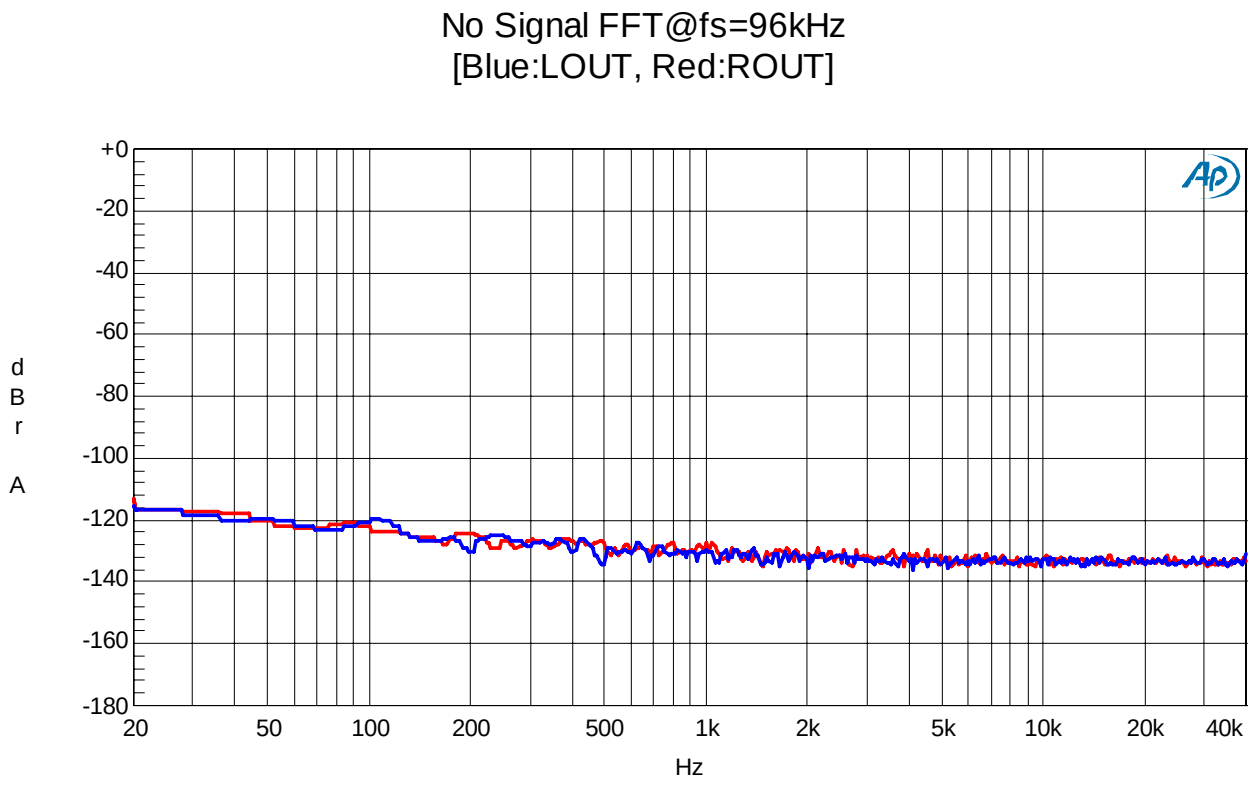


Figure 22. FFT (No Signal)

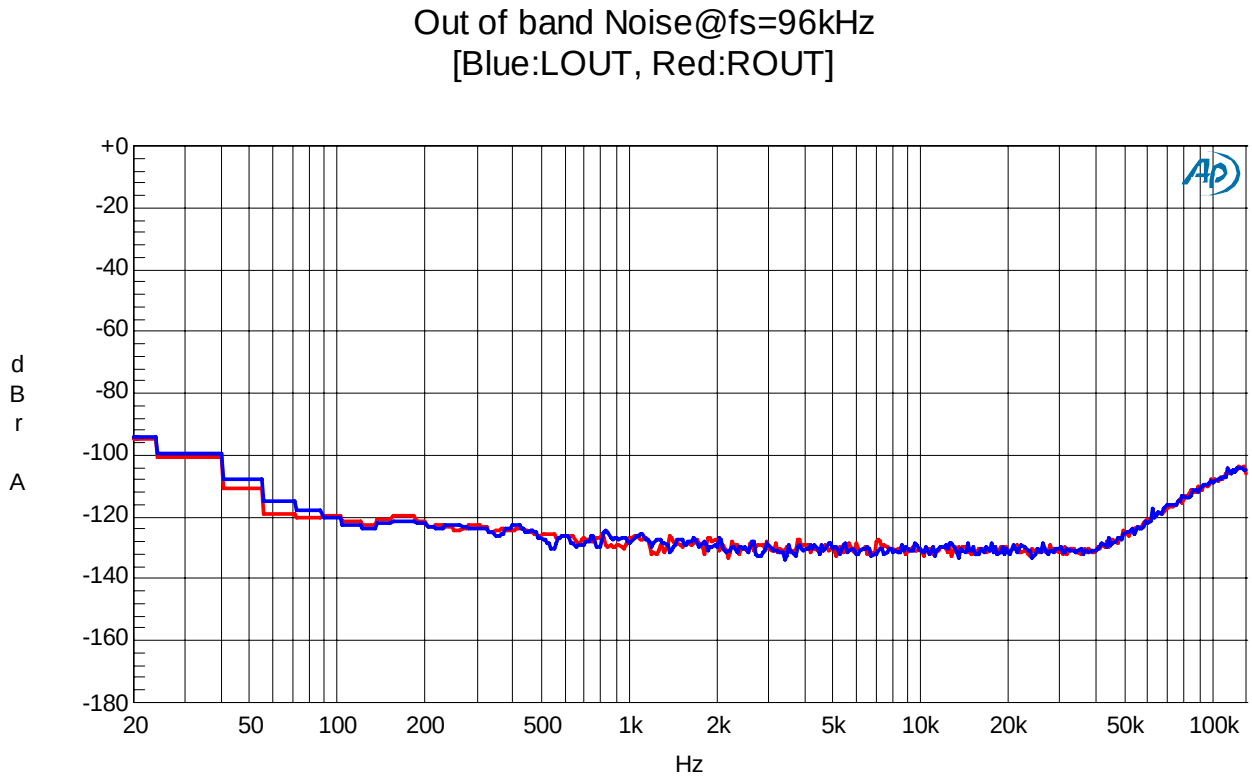


Figure 23. FFT (Out of band noise)

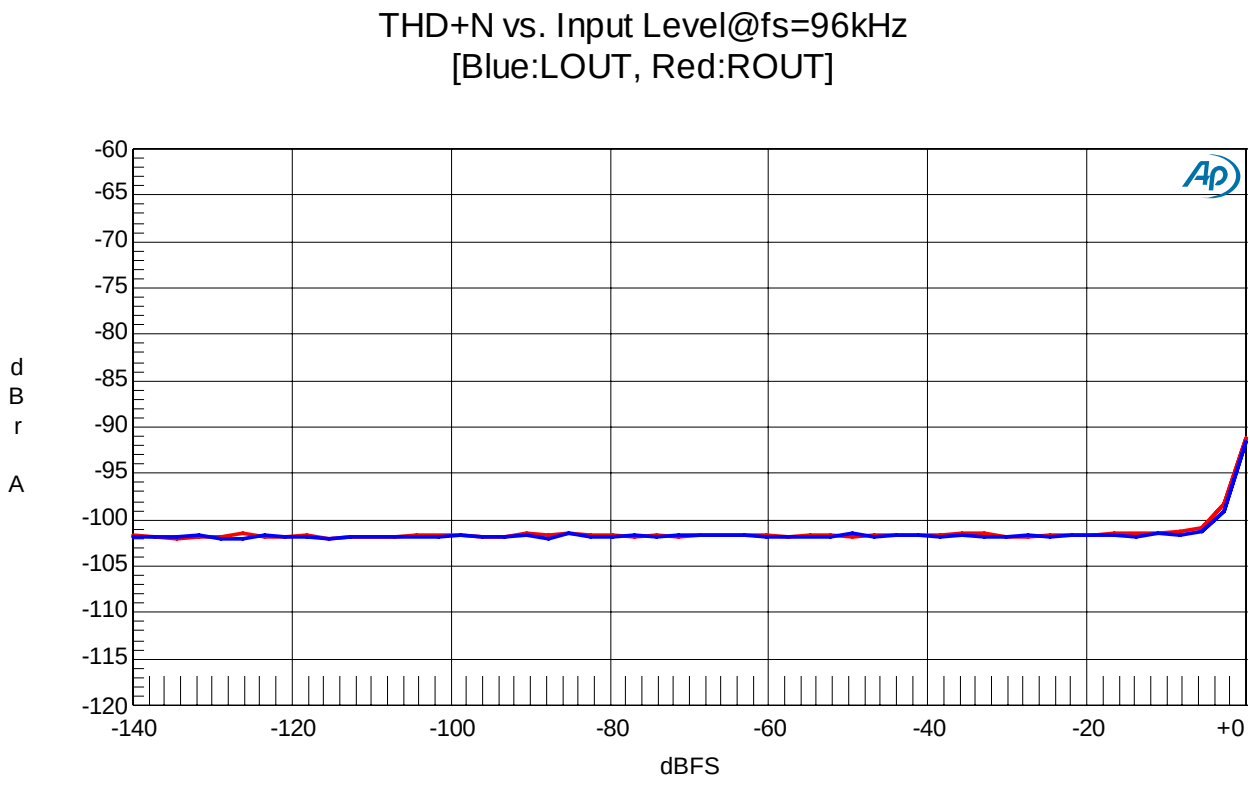


Figure 24. THD+N vs. Input level (fin=1kHz)

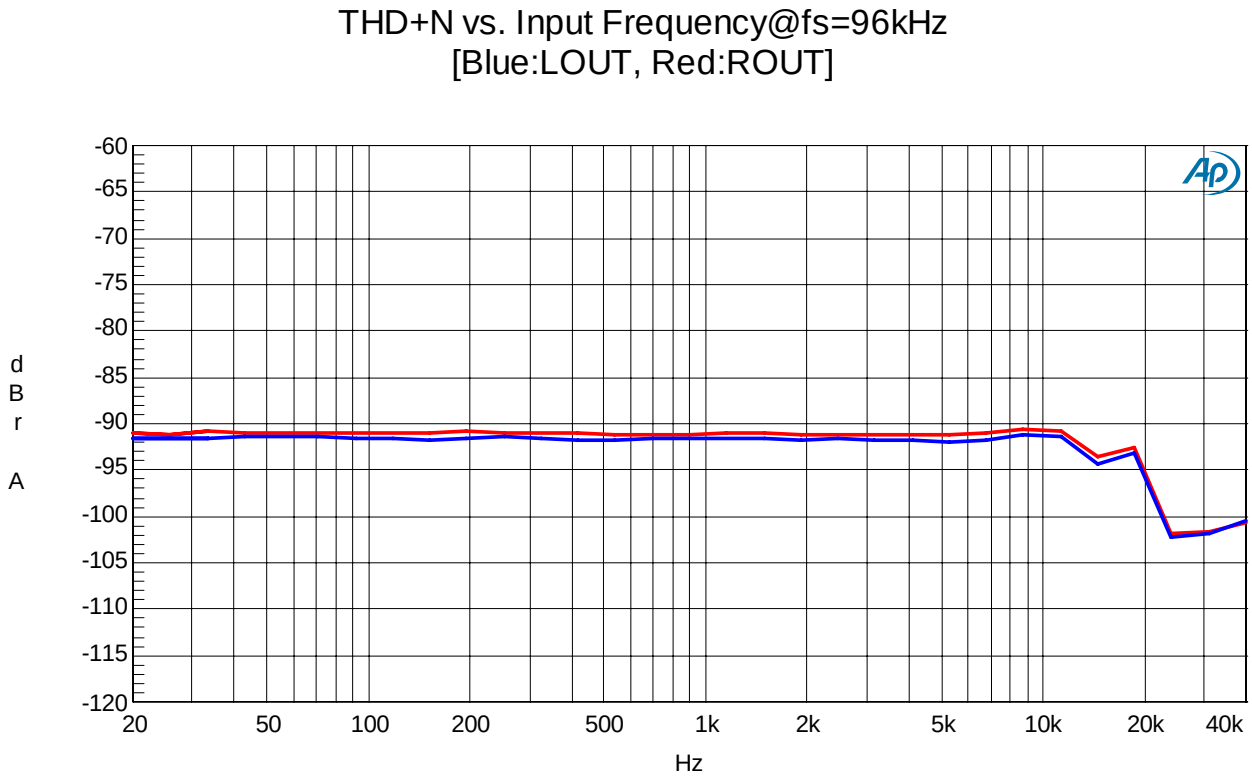


Figure 25. THD+N vs. Input Frequency (Input level=0dBFS)

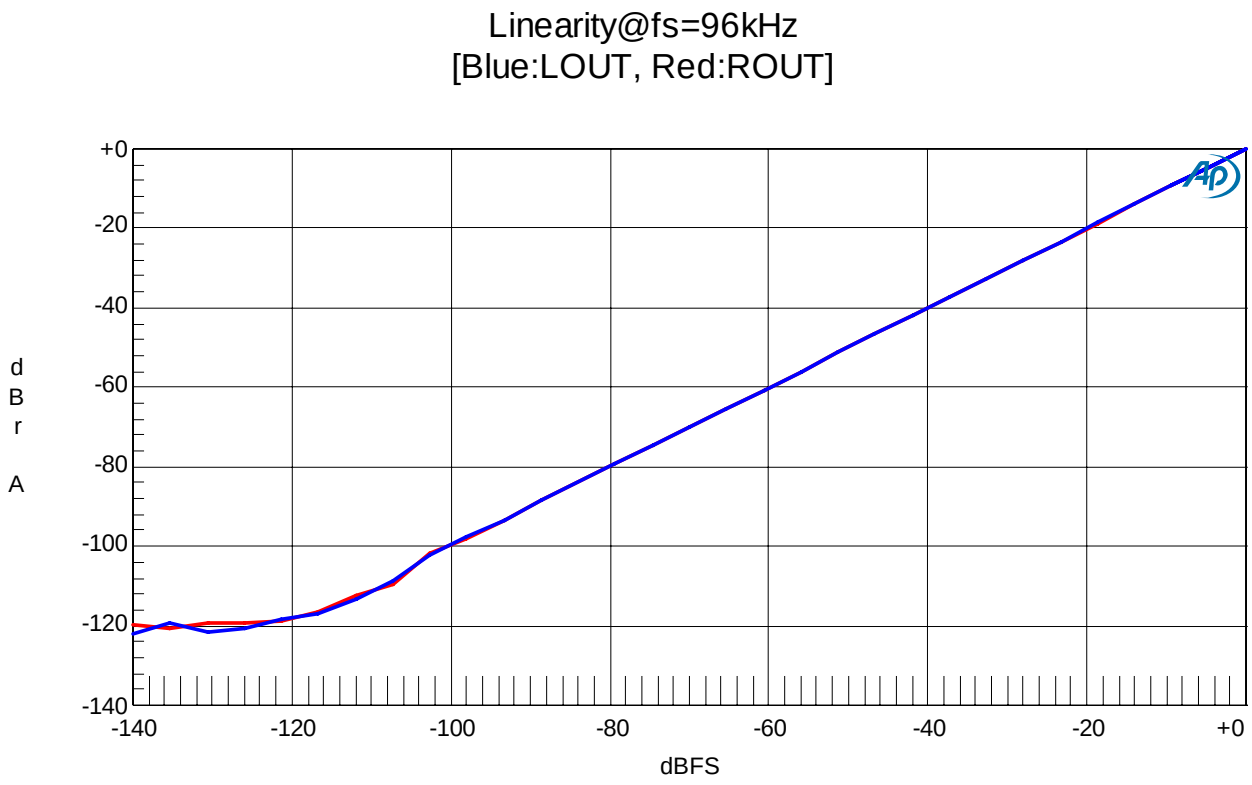


Figure 26. Linearity (fin=1kHz)

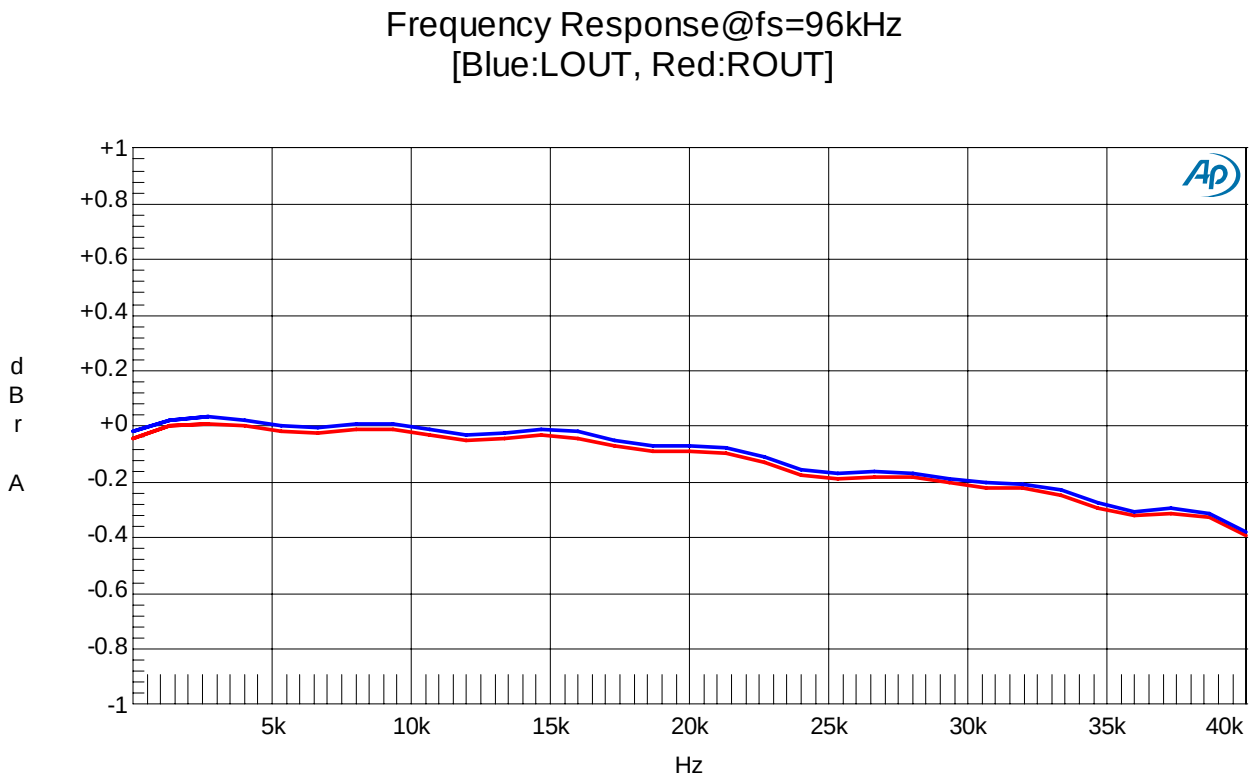


Figure 27. Frequency Response (Input level=0dBFS)

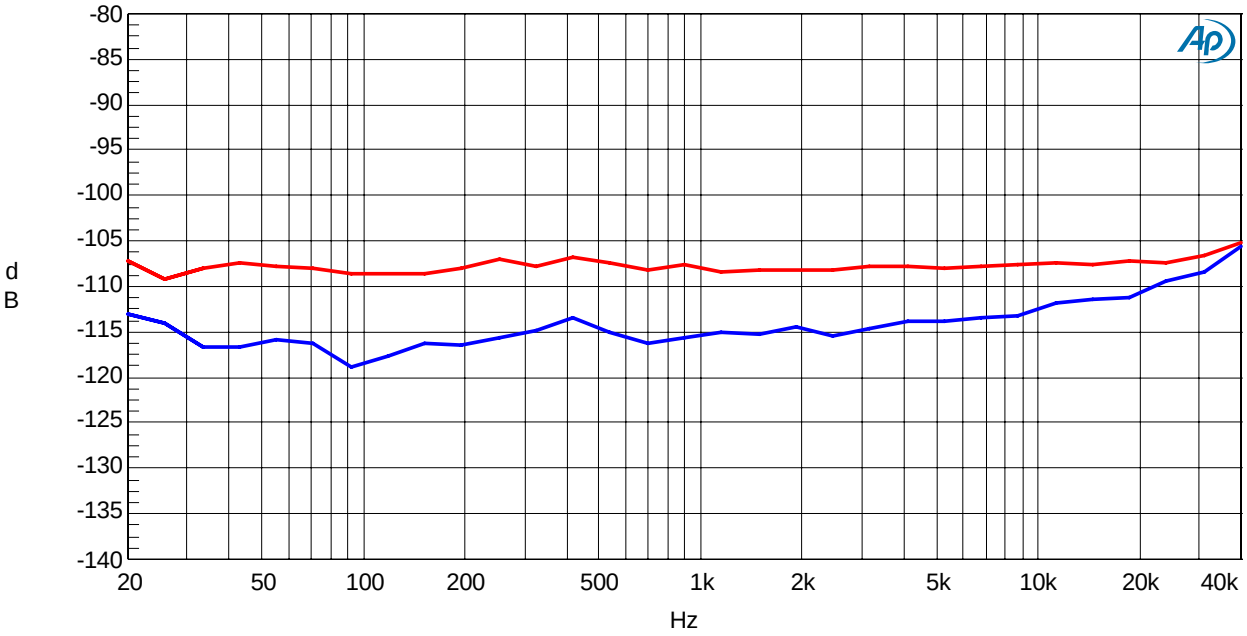


Figure 28. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

**(3) fs = 192kHz (MCLK=128fs)**

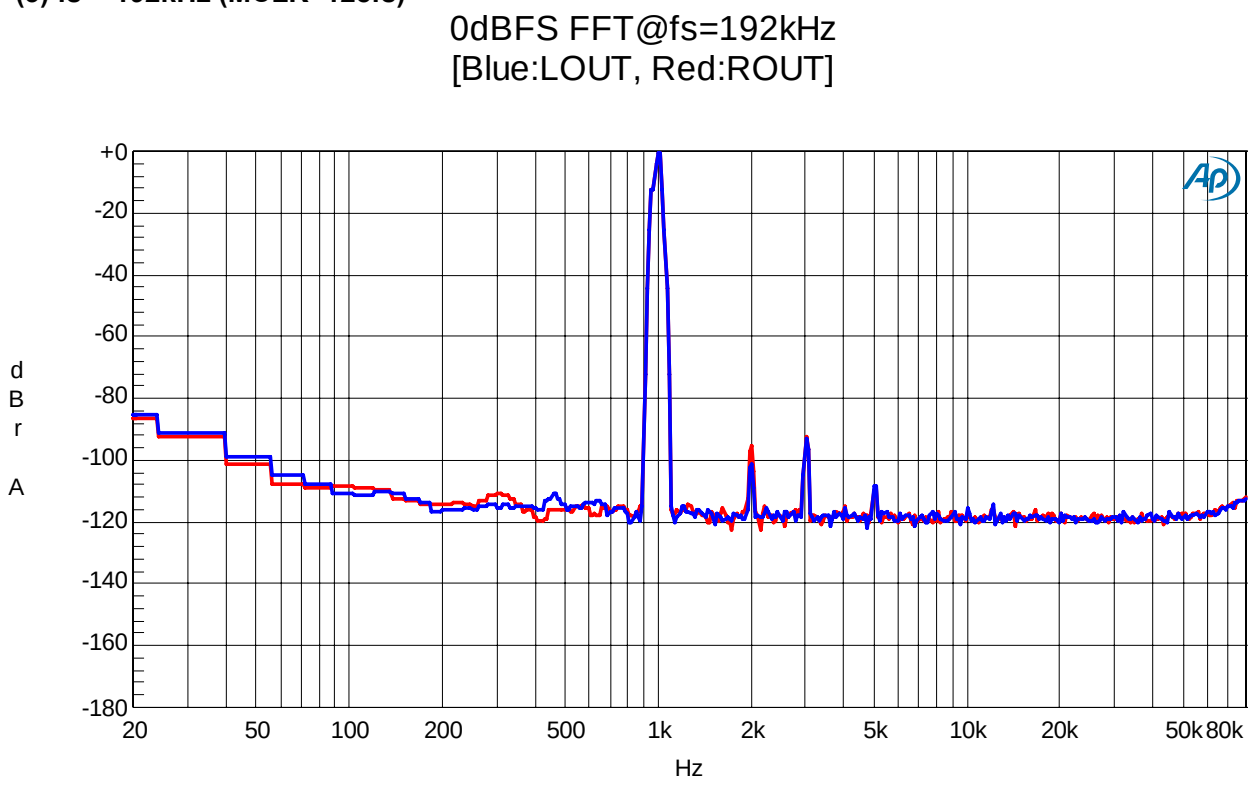


Figure 29. FFT (fin=1kHz, Input Level=0dBFS)

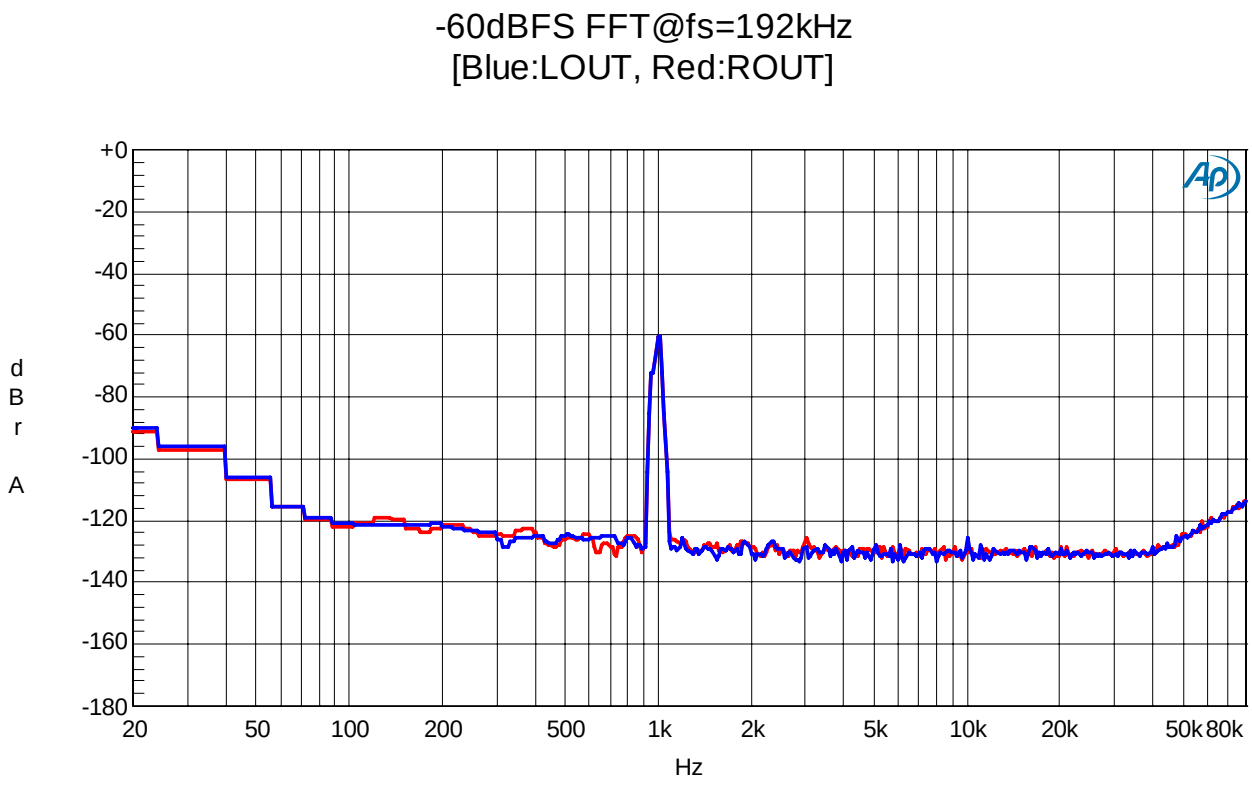


Figure 30. FFT (fin=1kHz, Input Level=-60dBFS)

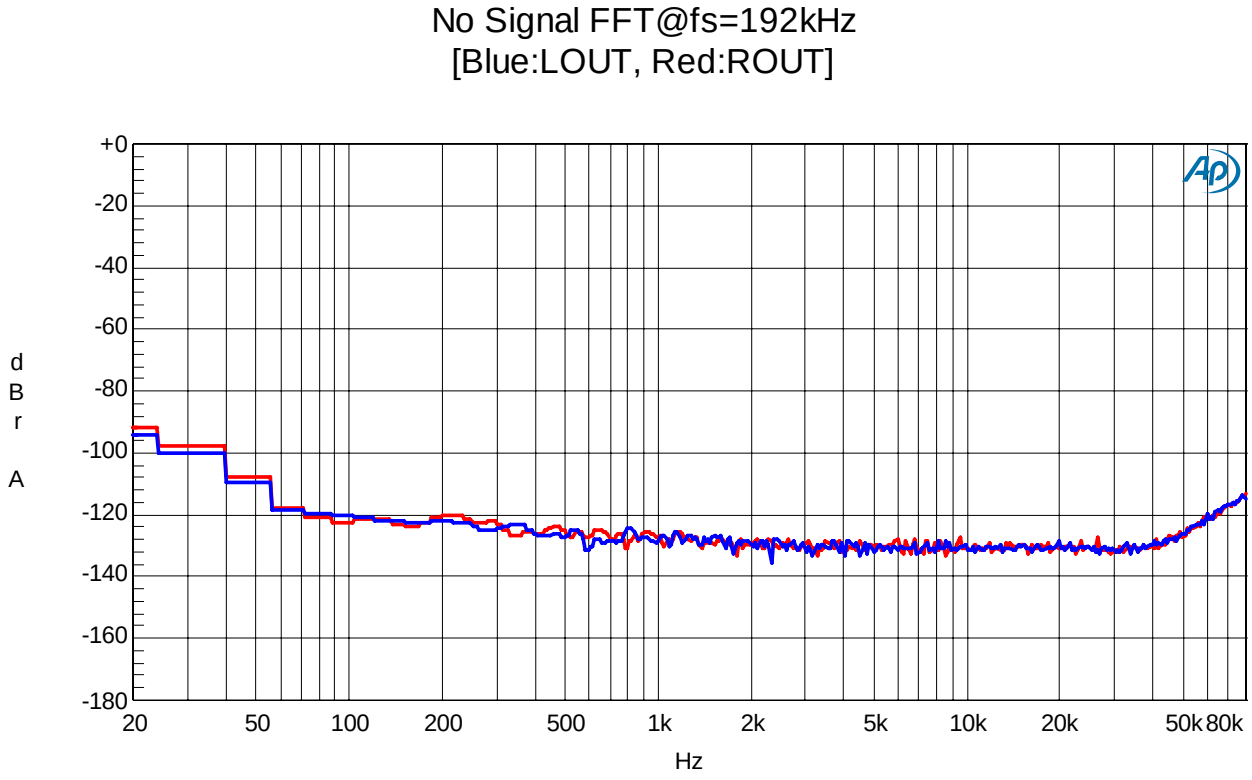


Figure 31. FFT (No Signal)

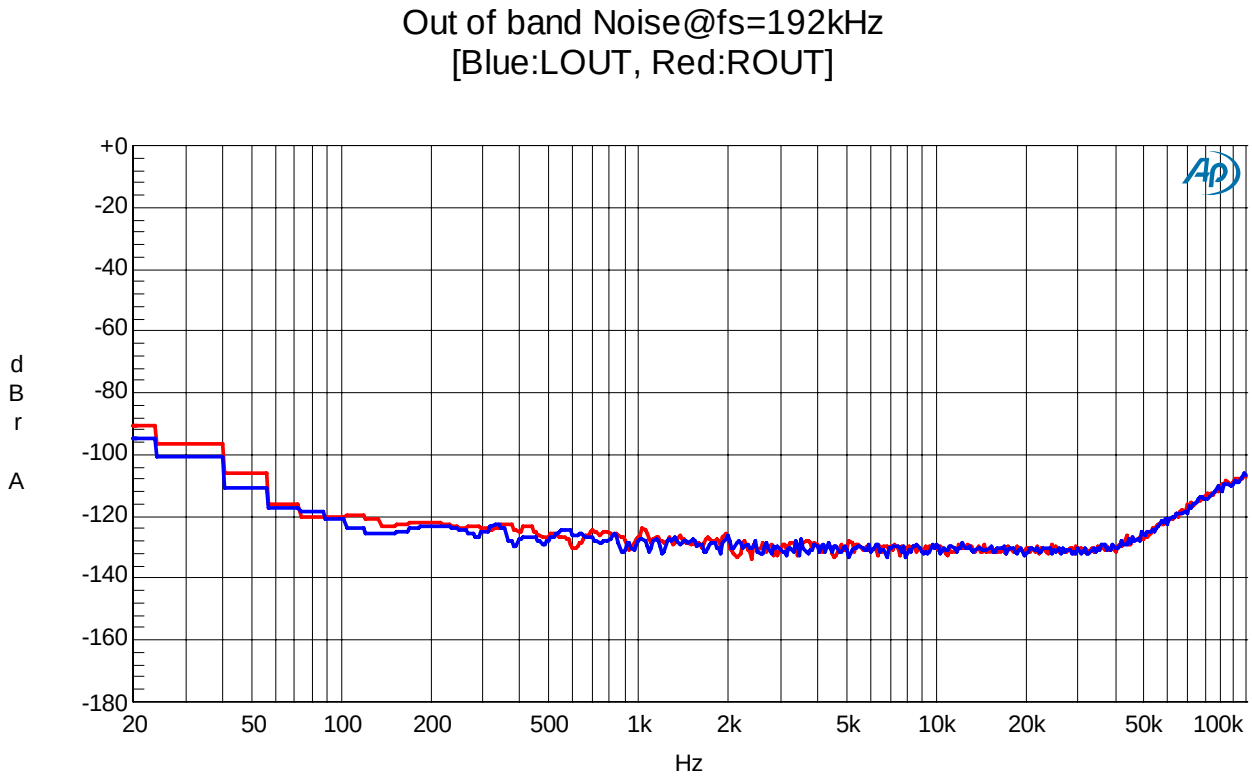


Figure 32. FFT (Out of band noise)

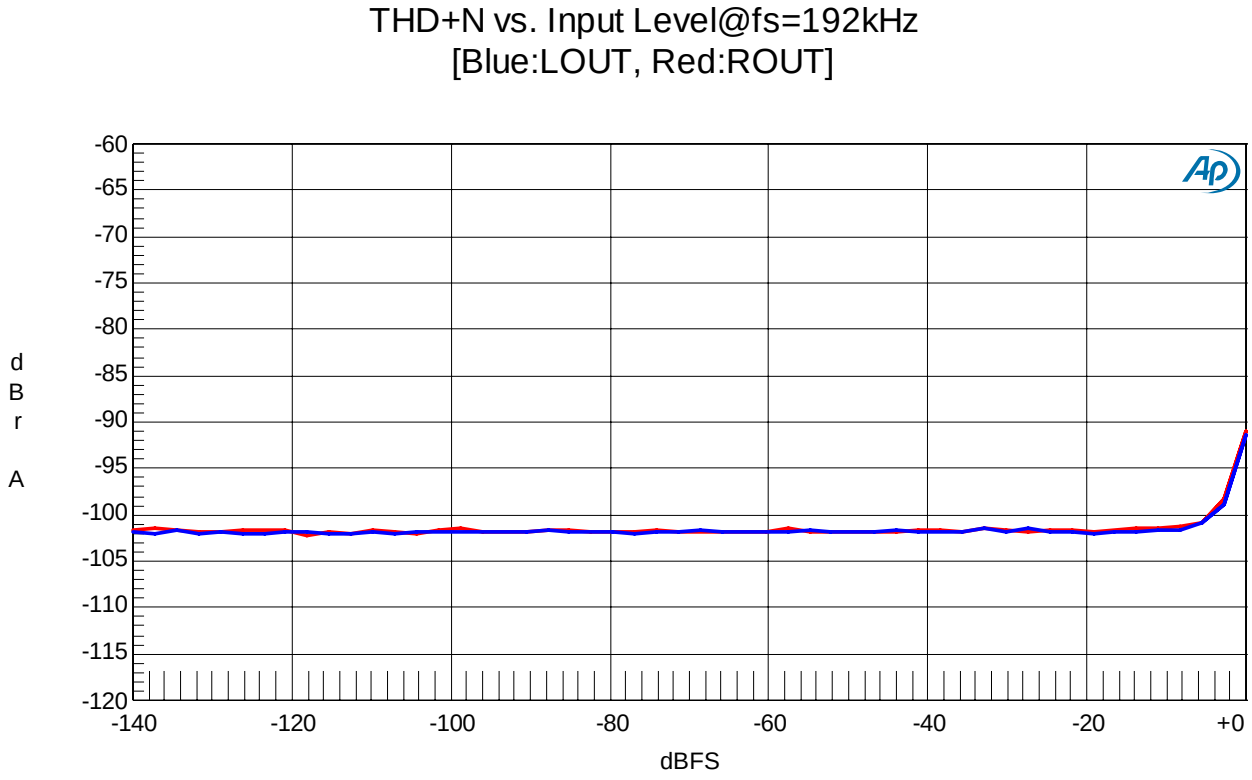


Figure 33. THD+N vs. Input level (fin=1kHz)

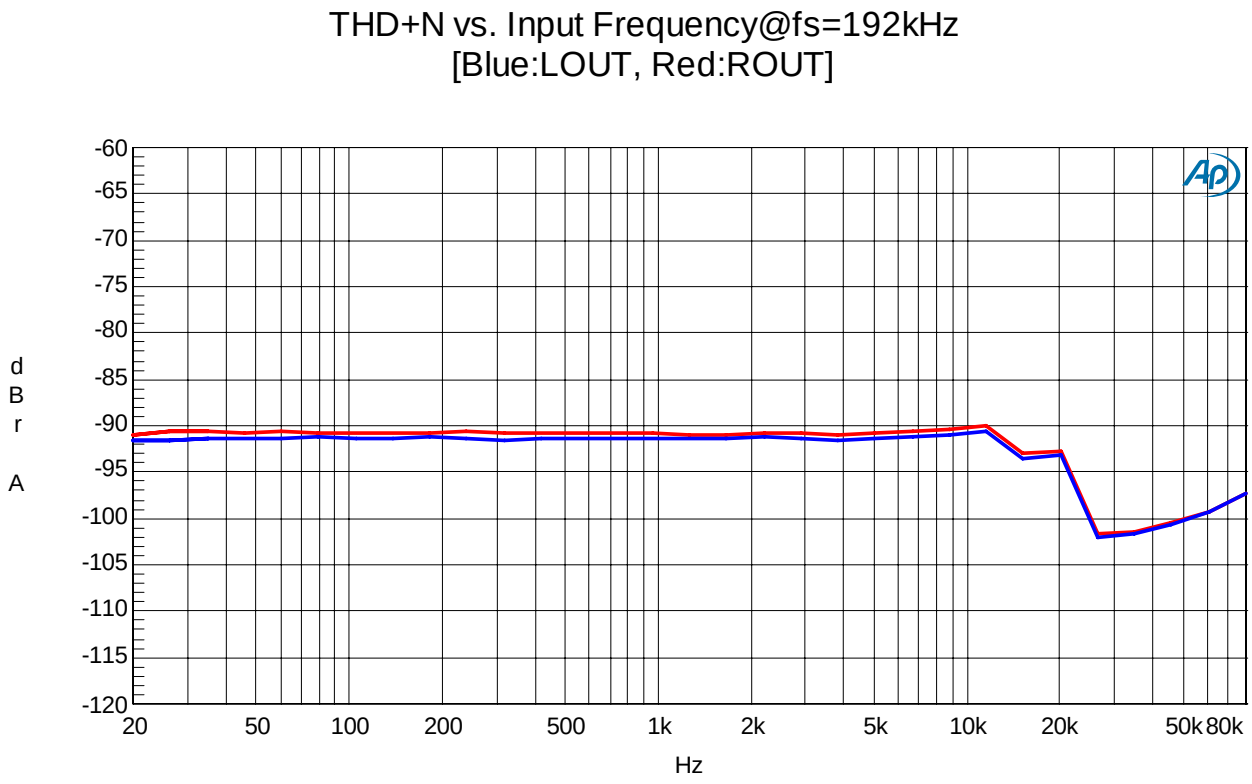


Figure 34. THD+N vs. Input Frequency (Input level=0dBFS)

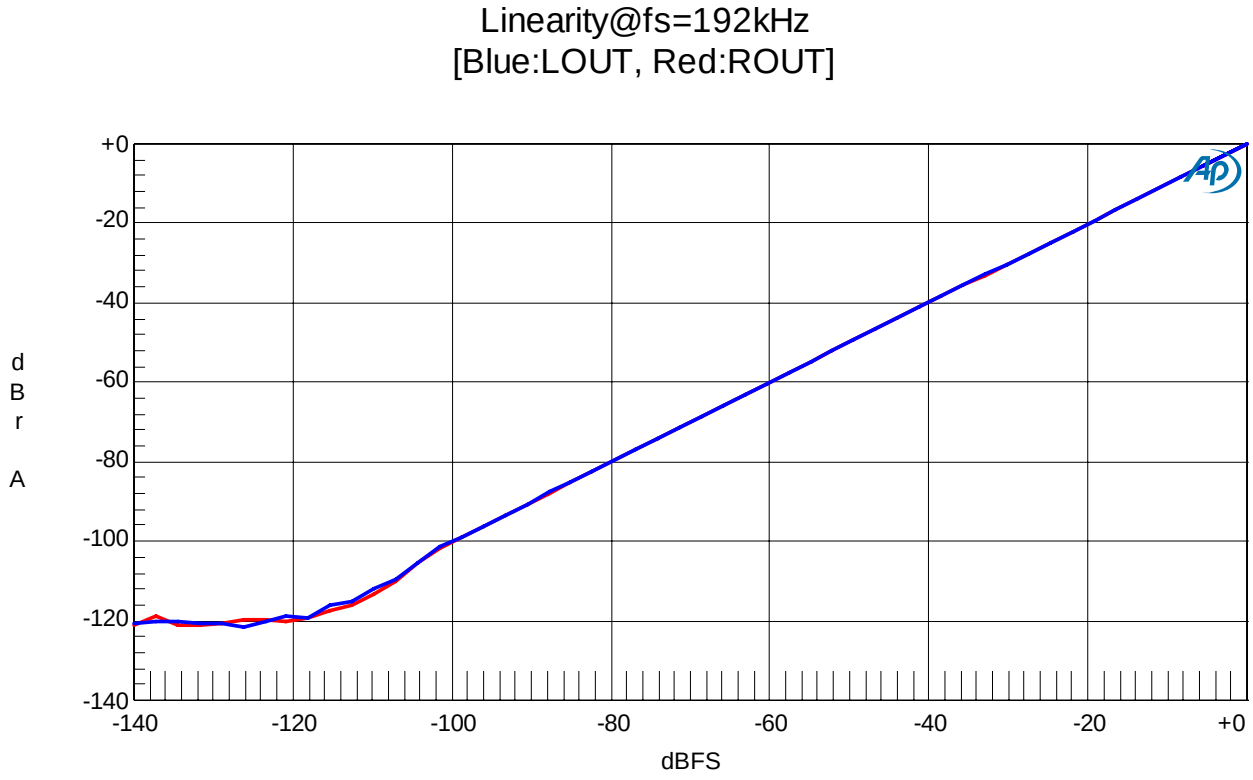


Figure 35. Linearity (fin=1kHz)

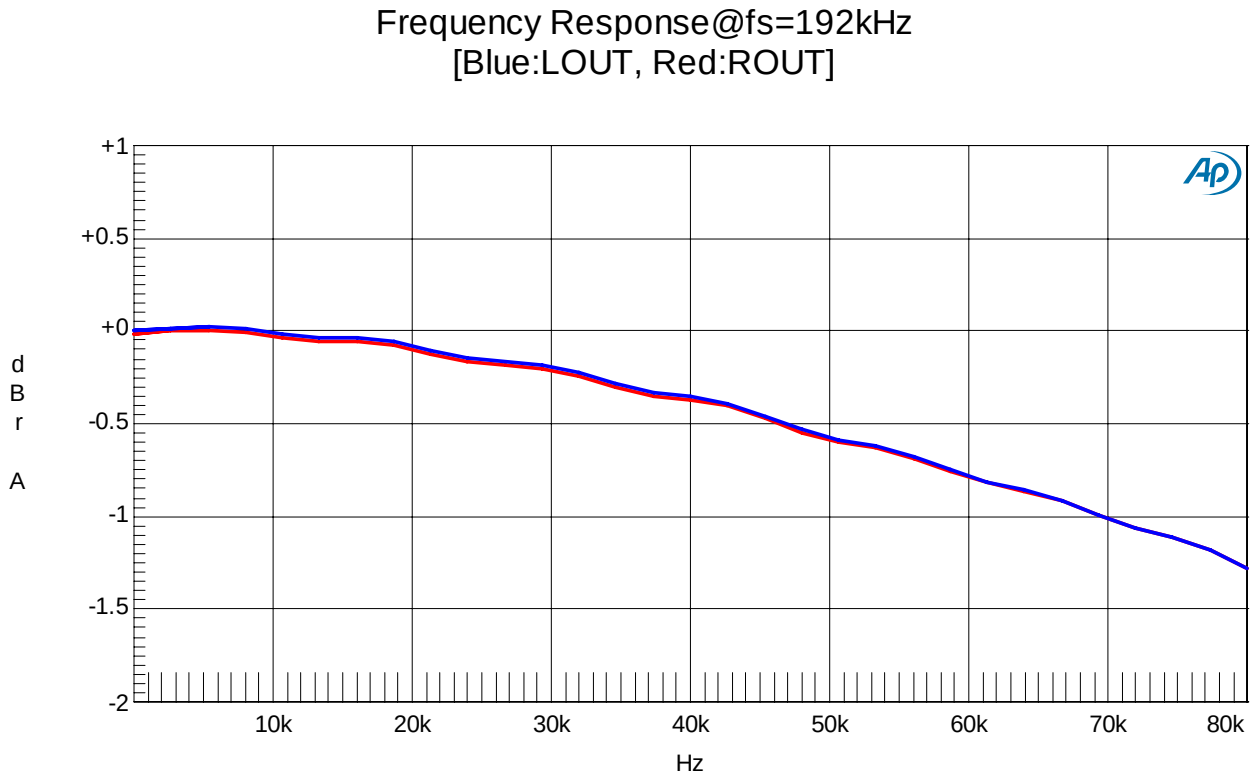


Figure 36. Frequency Response (Input level=0dBFS)

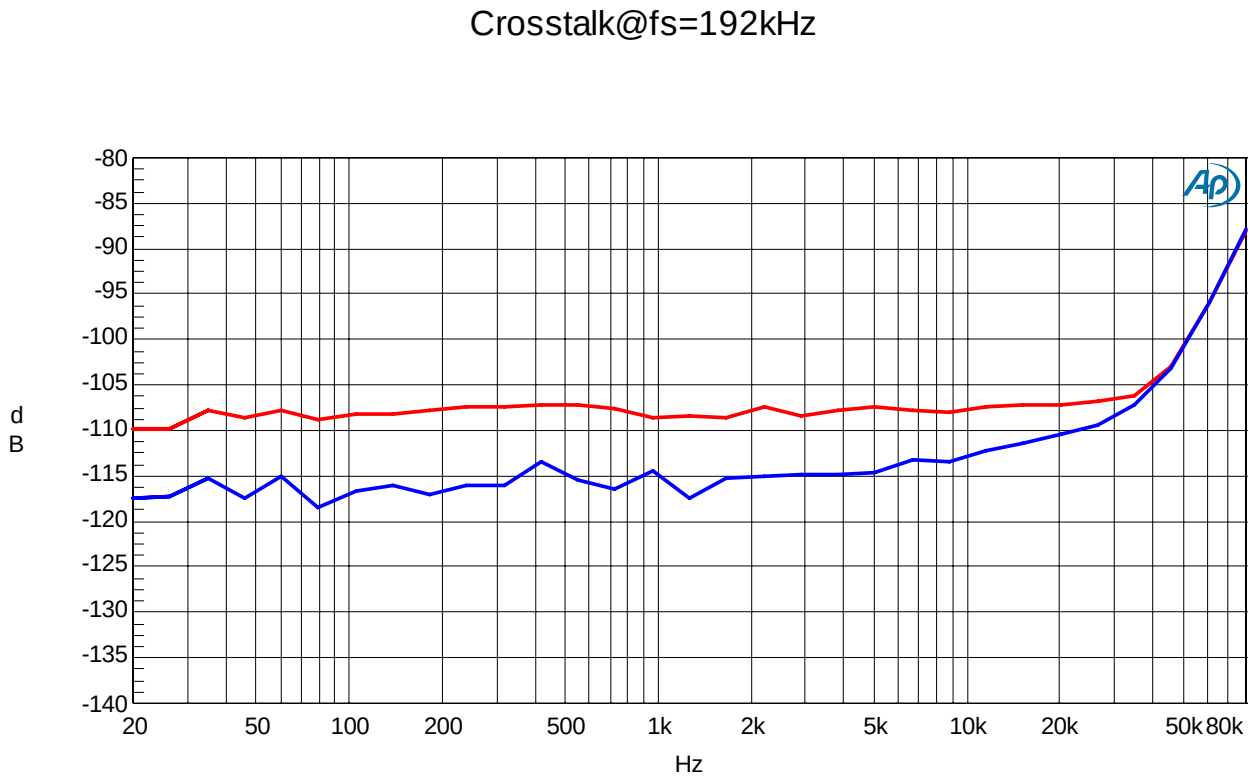


Figure 37. Crosstalk (Input level=0dBFS)
Red: Lch ← Rch, Blue: Rch ← Lch

## REVISION HISTORY

| Date (yy/mm/dd) | Manual Revision | Board Revision | Reason | Page | Contents |
|---|---|---|---|---|---|
| 09/09/02 | KM100600 | 0 | First Edition | | |

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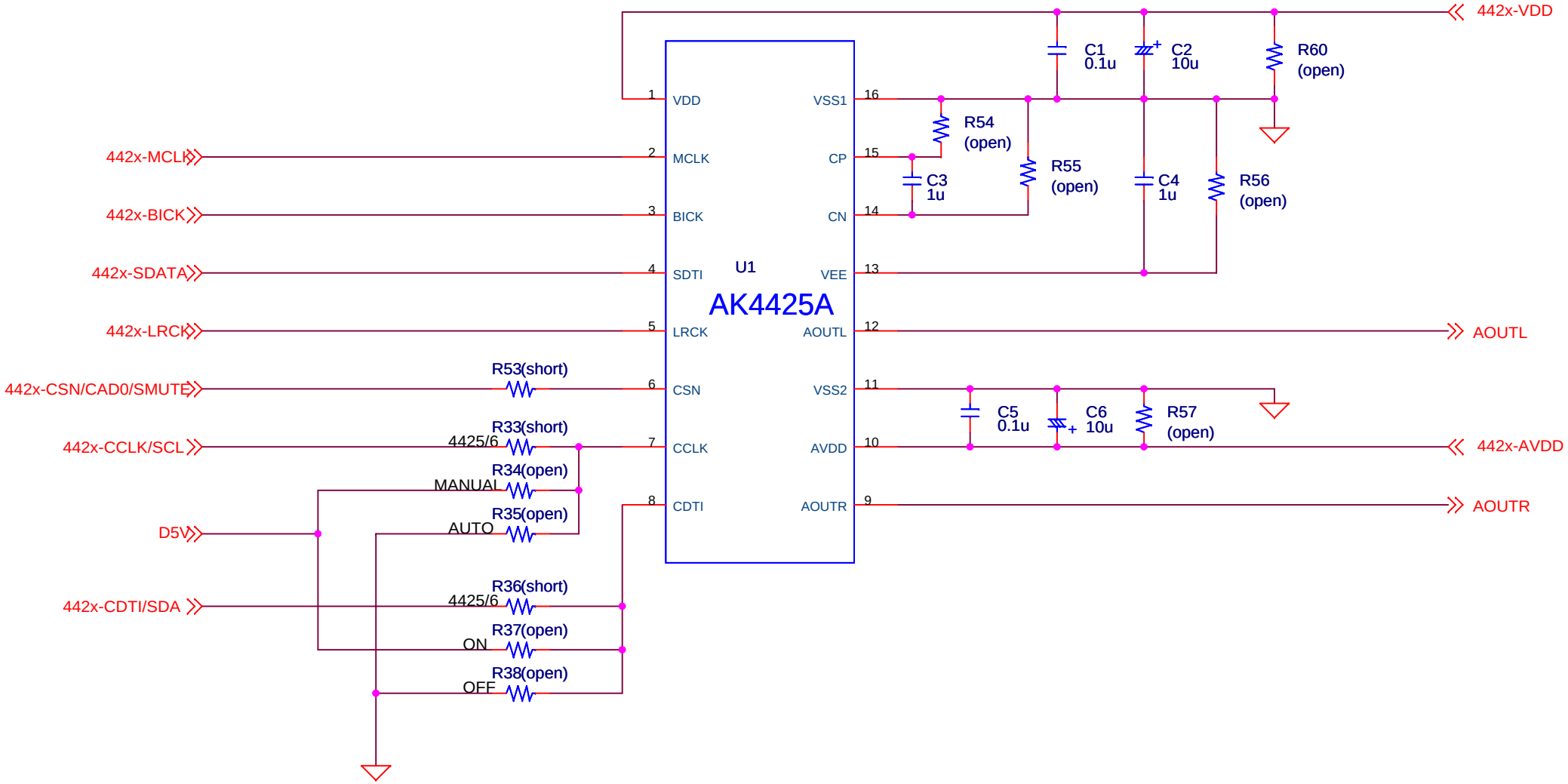


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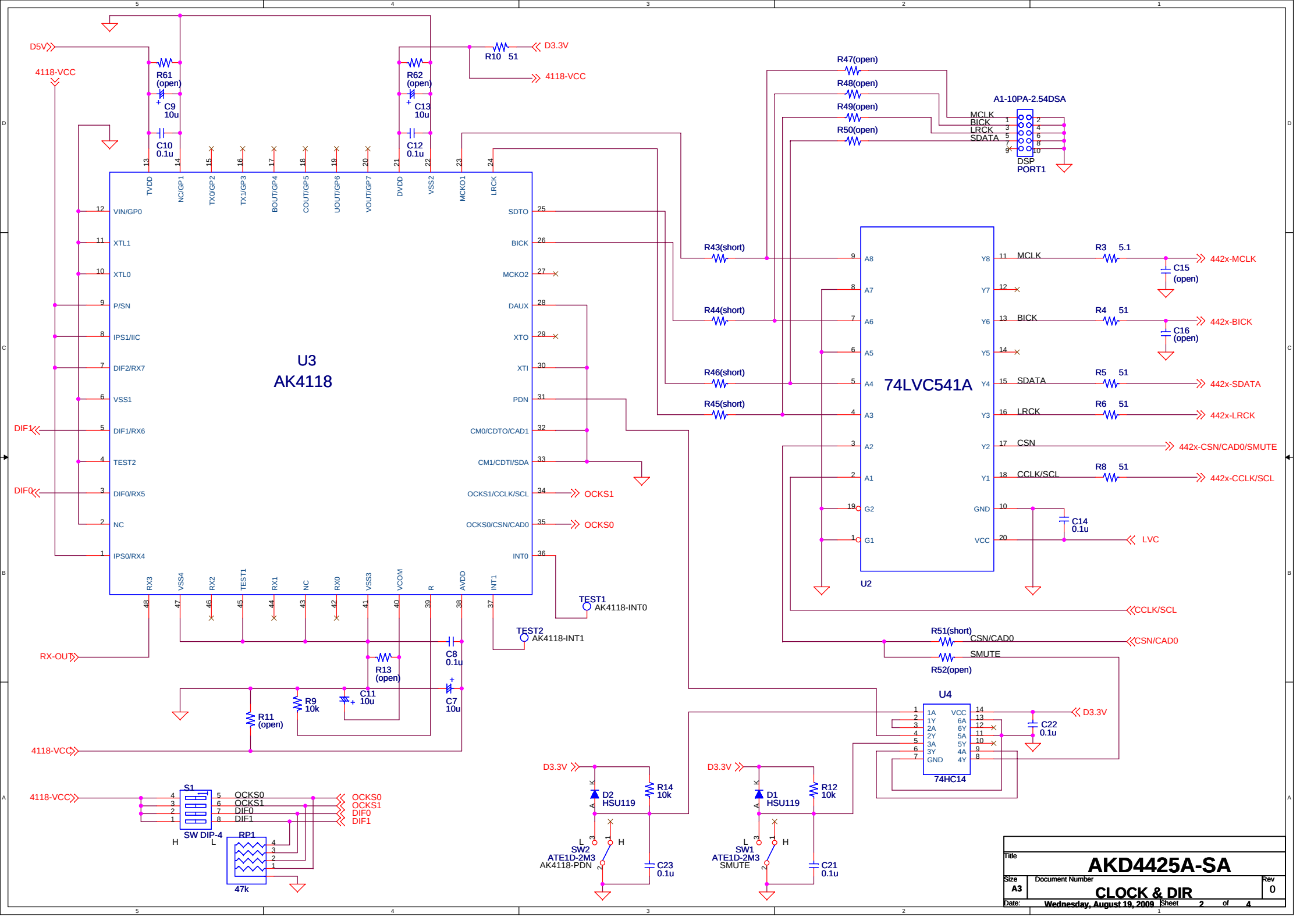
| Date: Wednesday, August 19, 2009 | Sheet 1 of 4 | |

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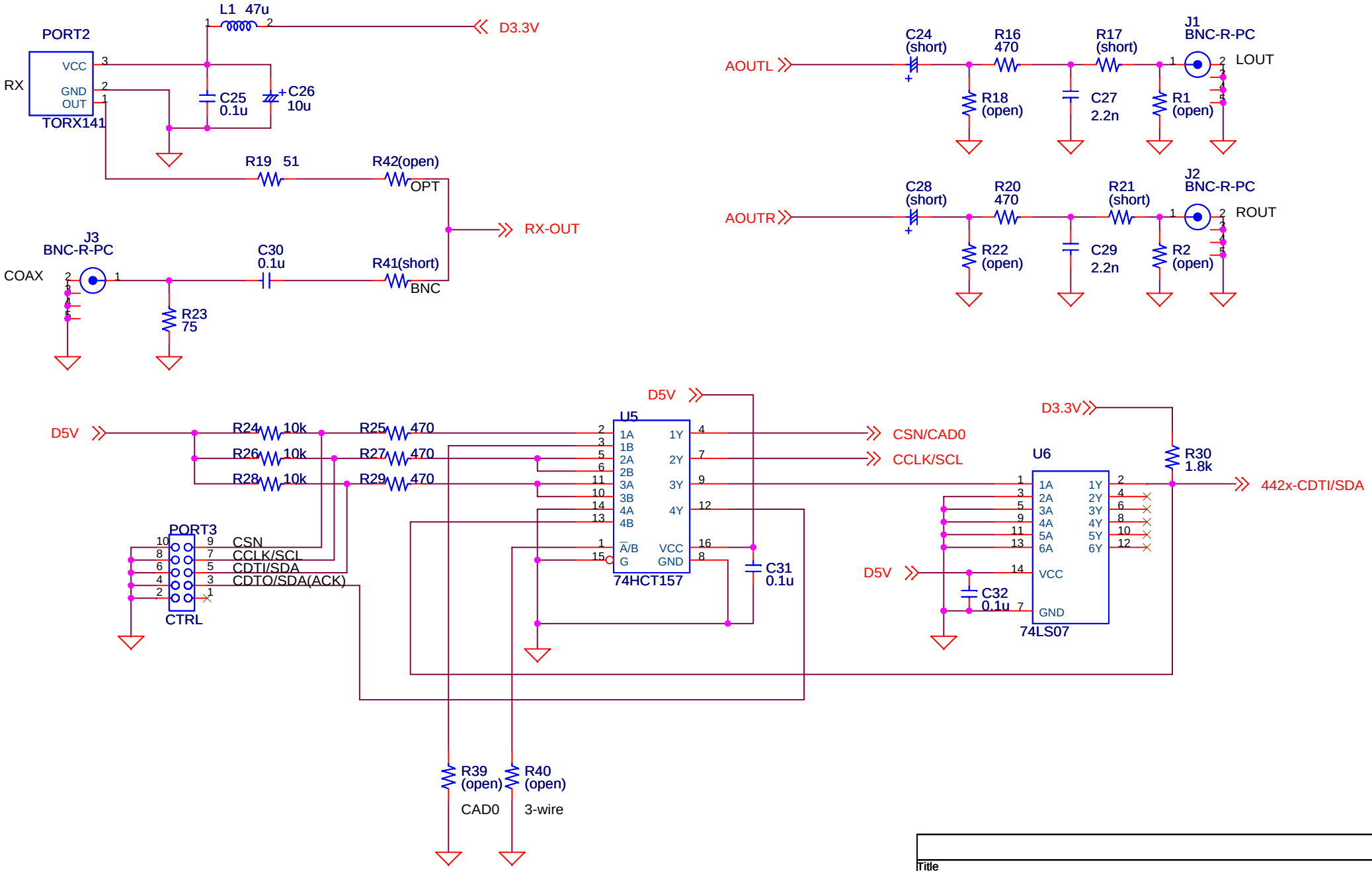


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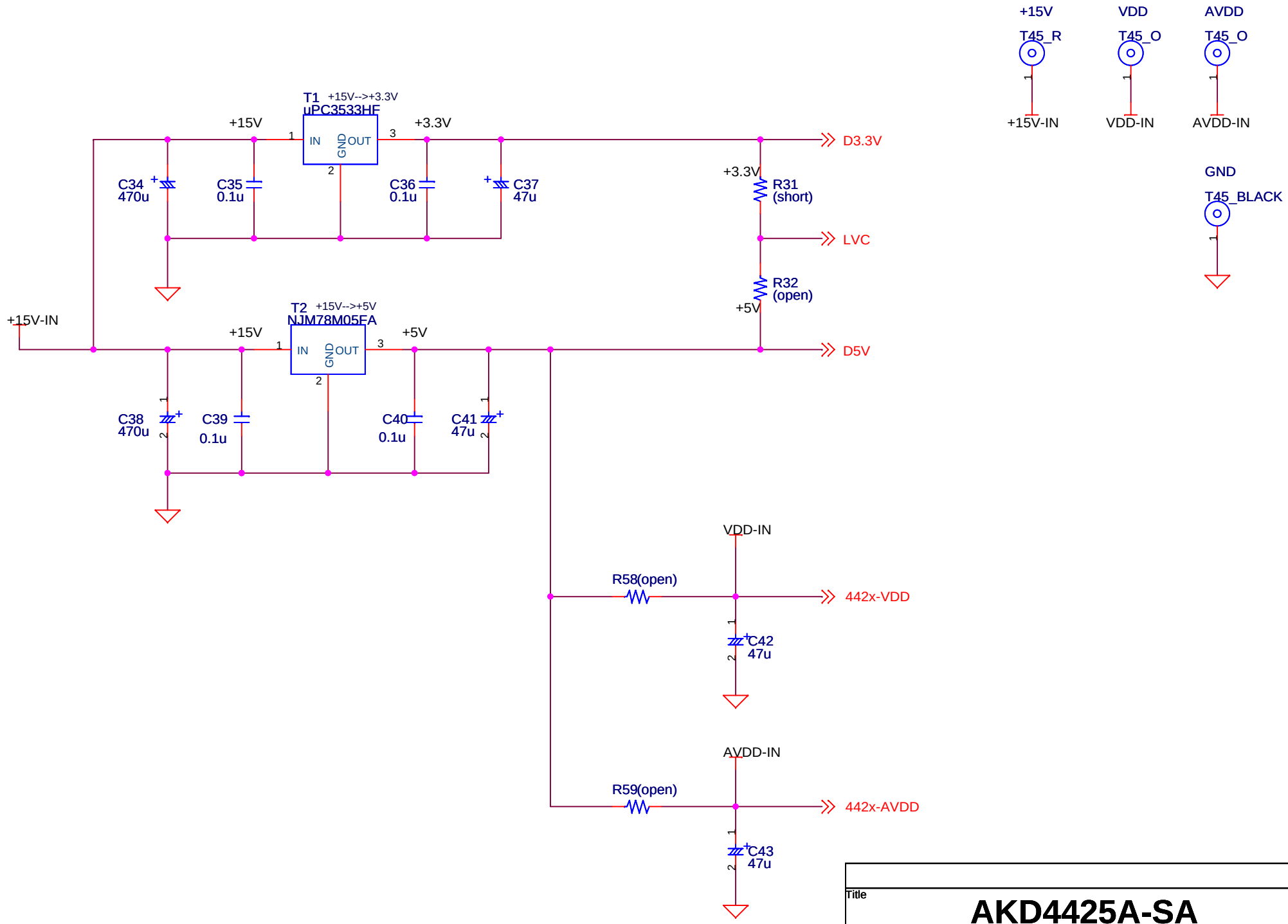


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| Size: A4 | Document Number: Power Supply | Rev: 0 |
| Date: Wednesday, August 19, 2009 | Sheet 4 of 4 | |