μPD27C256A
32,768 x 8-BIT
CMOS UV EPROM

Description

The μPD27C256A is a 262,144-bit ultraviolet erasable and electrically programmable read-only memory fabricated with double-polysilicon CMOS technology. The device is organized as 32K words by 8 bits and operates from a single +5-volt power supply.

The μPD27C256A has a single-location programming feature, three-state outputs, fully TTL-compatible inputs and outputs, and a program voltage (V_{PP}) of 12.5 volts.

The μPD27C256A is available in a cerdip package with a quartz window as an ultraviolet (UV) erasable EPROM.

Features

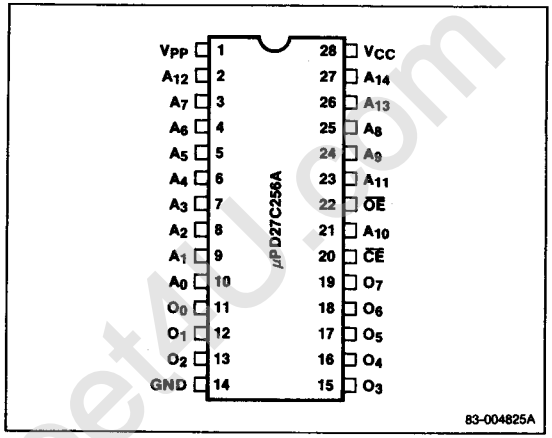
- ☐ 32K-word by 8-bit organization
- ☐ Ultraviolet erasable and electrically programmable
- ☐ Single location programming
- ☐ High-speed programming
- ☐ Low power dissipation
  - — 165 mW (active)
  - — 550 μW (standby)
- ☐ TTL-compatible I/O for reading and programming
- ☐ Single +5-volt power supply
- ☐ JEDEC vendor identification
- ☐ Double-polysilicon CMOS technology
- ☐ 28-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD27C256AD-15	150 ns	28-pin cerdip
D-20	200 ns	

Pin Configuration

28-Pin Cerdip



Pin Identification

Symbol	Function
A_0-A_{14}	Address inputs
O_0-O_7	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
GND	Ground
V_{CC}	+5-volt power supply
V_{PP}	Program voltage

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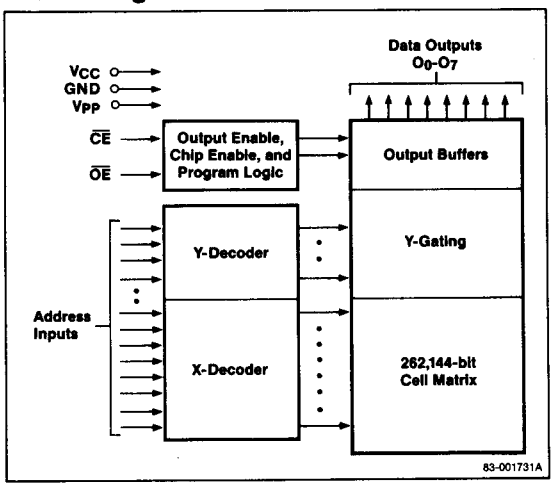
Block Diagram



Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.6 V to V_{CC} + 0.6 V
Output voltage, V_{OUT}	−0.6 V to V_{CC} + 0.6 V
Operating temperature, T_{OPR}	−25 to 85°C
Storage temperature, T_{STG}	−65 to 125°C
Program voltage, V_{PP}	−0.6 to +13.0 V
ID read voltage on pin 24, V_{ID}	−0.6 to +13.5 V

Note:

(1) V_{IN} = −3.0 V min for 20 ns pulse.

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1)

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input capacitance	C_{IN}		4	6	pF	V_{IN} = 0 V
Output capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0 V

Notes:

(1) This parameter is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; V_{PP} = V_{CC}

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read and Standby Modes						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Output leakage current	I_{LO}			10	μA	$\overline{OE}$ = V_{IH}; V_{OUT} = 0 V to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
Operating supply current	I_{CCA1}			30	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
Operating supply current	I_{CCA2}			30	mA	f = 5 MHz; I_{OUT} = 0 mA
Standby supply current	I_{SB1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}		1	100	μA	$\overline{CE}$ = V_{CC}
Program voltage current	I_{PP1}		1	100	μA	V_{PP} = V_{CC}

DC Characteristics (cont)

T_A = 25 ±5°C; V_{CC} = +6 ±0.25 V; V_{PP} = +12.5 ±0.3 V

		Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Program, Program Verify, and Program Inhibit Modes						
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
ID read voltage	V_{ID}	11.5		12.5	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = V_{IL} or V_{IH}
Operating supply current	I_{CC}			30	mA	
Program voltage current	I_{PP2}			30	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%; V_{PP} = V_{CC}

Parameter	Symbol	Limits μPD27C256A-15 Min	Limits μPD27C256A-15 Max	Limits μPD27C256A-20 Min	Limits μPD27C256A-20 Max	Unit	Test Conditions (Note 2)
Read and Standby Modes							
Address to output delay	t_{ACC}		150		200	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		150		200	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ low to data output delay	t_{OE}		75		75	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ high to data output float delay	t_{DF}	0	60	0	60	ns	$\overline{CE}$ = V_{IL}
Address to output hold time	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Notes:

(1) See figure 1 for output load; input rise and fall times = 0.45 V to 2.4 V; input and output timing measurement levels = 0.8 V and 2.0 V.

AC Characteristics (cont)

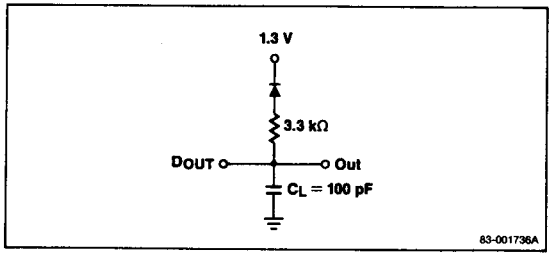
T_A =25 ±5°C; V_{CC} = +6 ±0.25 V; V_{PP} = +12.5 ±0.3 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Program, Program Verify, and Program Inhibit Modes						
Address setup time	t_{AS}	2			μs	(Note 1)
Data setup time	t_{DS}	2			μs	(Note 1)
Address hold time	t_{AH}	2			μs	(Note 1)
Data hold time	t_{DH}	2			μs	(Note 1)
Output enable to output float delay	t_{DF}	0		130	ns	(Note 1)
V_{PP} setup time	t_{VPS}	2			μs	(Note 1)
Program pulse width	t_{PW}	0.95	1	1.05	ms	(Note 1)
V_{CC} setup time	t_{VCS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	(Note 1)
Overprogram pulse width	t_{OPW}	2.85		78.75	ms	
Data valid from $\overline{OE}$	t_{OE}			150	ns	

Notes:

(1) Input pulse levels = 0.45 V to 2.4 V; input and output timing reference levels = 0.8 V and 2.0 V; input rise and fall times = 20 ns.

Figure 1. Loading Conditions Test Circuit



Truth Table

Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Ag (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	D_{OUT}
Read disable	V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High-Z
Standby	V_{IH}	X	X	V_{CC}	V_{CC}	High-Z
Program	V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	D_{IN}
Program verify	V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	D_{OUT}
Program inhibit	V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High-Z
ID read	V_{IL}	V_{IL}	V_{ID}	V_{CC}	V_{CC}	D_{OUT}

Notes:

(1) X can be either V_{IL} or V_{IH}.

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Programming Operation

High-Speed Programming Mode

Begin programming by erasing all data; this sets all bits at a high logic level (1). To enter data, program a low-level (0) TTL signal into the chosen bit location.

Address the first location and apply valid data at the eight output pins. Raise V_{CC} to +6 ±0.25 V; then raise V_{PP} to +12.5 ±0.3 V.

Apply a 1-ms (±5%) program pulse to $\overline{CE}$ as shown in the programming portion of the timing waveform. Verify the bit prior to making a program/no-program decision. If the bit is not programmed, apply another 1-ms pulse to $\overline{CE}$, up to a maximum of 25 times. If the bit is programmed within 25 tries, apply an additional overprogram pulse of 3x ms (where "x" equals the number of tries) and input the next address. If the bit is not programmed in 25 tries, reject the device as a program failure.

After all bits are programmed, lower both V_{CC} and V_{PP} to +5 V ±10% and verify all data again.

Programming Inhibit Mode

Use the programming inhibit mode to program multiple μPD27C256As connected in parallel. All like inputs (except $\overline{CE}$, but including $\overline{OE}$) may be common. Program individual devices by applying a low-level (0) TTL pulse to the $\overline{CE}$ input of the device to be programmed. Applying a high level (1) to the $\overline{CE}$ input of the other devices prevents them from being programmed.

Program Verify Mode

To verify that the device was correctly programmed, set $\overline{OE}$ at logic level 0. To verify data on multiple μPD27C256As connected in parallel with a common $\overline{OE}$ input applied to all devices, first reduce V_{PP} to V_{CC}. Then the normal read mode can be used with a logic level 0 applied to the $\overline{CE}$ input of the device to be verified. Apply a logic level 1 to the $\overline{CE}$ input of all other devices.

Erasure

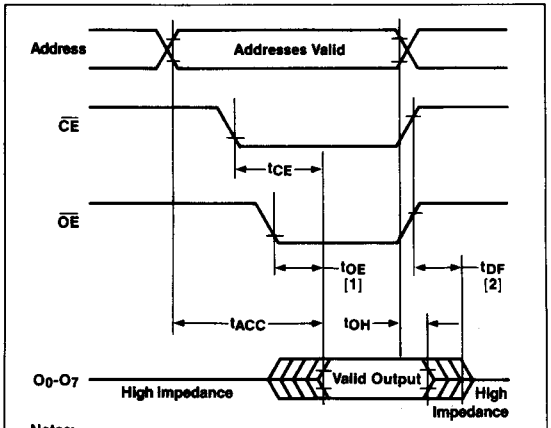
Erase data on the μPD27C256A by exposing it to light with a wavelength shorter than 400 nm. Exposure to direct sunlight or fluorescent light could also erase the data. Consequently, mask the window to prevent unintentional erasure by ultraviolet rays.

Data is typically erased by ultraviolet rays of 254 nm. A lighting level of 15 W-sec/cm^2 (min) is required to completely erase written data (ultraviolet ray intensity multiplied by exposure time).

An ultraviolet lamp rated at 12,000 μW/cm^2 takes approximately 15 to 20 minutes to complete erasure. Place the μPD27C256A within 2.5 cm of the lamp tubes. Remove any filter on the lamp.

Timing Waveforms

Read Mode



Notes:
[1] $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the falling edge of $\overline{CE}$ for read mode without impact on t_{ACC}.
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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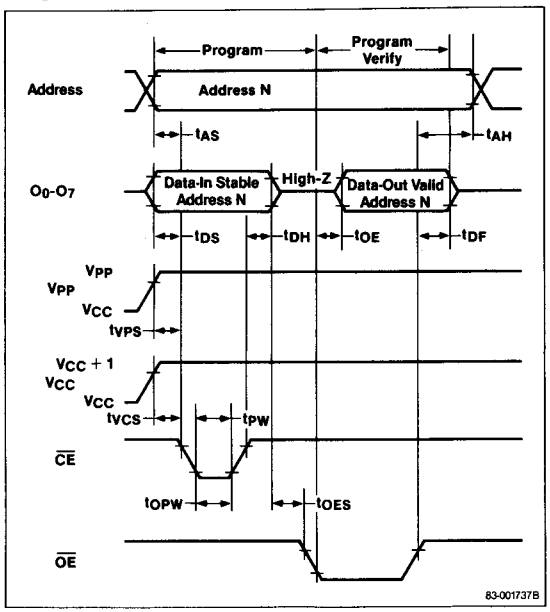
Program Mode



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