TS4999

Filter-free stereo 2.8 W class D audio power amplifier with selectable 3D sound effects

Features

- Operates from V_{CC} = 2.4 to 5.5 V
- Dedicated standby mode active low/channel
- Output power per channel: 2.8 W at 5 V into 4 Ωwith 10% THD+N or 0.7 W at 3.6 V into 8 Ω with 1% THD+N max.
- Selectable 3D sound effect
- Four gain setting steps: 3.5, 6, 9.5 and 12 dB
- Low current consumption
- PSSR: 63 dB typical at 217 Hz.
- Fast start up phase: 7.8 ms
- Short-circuit and thermal shutdown protection
- Flip chip 18-bump lead-free package

Applications

- Cellular phones
- PDAs
- Notebook PCs

Description

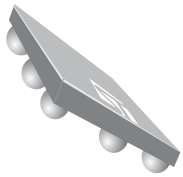
The TS4999 is a stereo fully-differential class D power amplifier. It can drive up to 1.35 W into a 8 Ω load at 5 V per channel. The device has four different gain settings utilizing two discrete pins, G0 and G1.

Pop and click reduction circuitry provides low on/off switch noise while allowing the device to start within 8 ms. 3D enhancement effects are selected through one digital input pin that allows more amazing stereo audio sound.

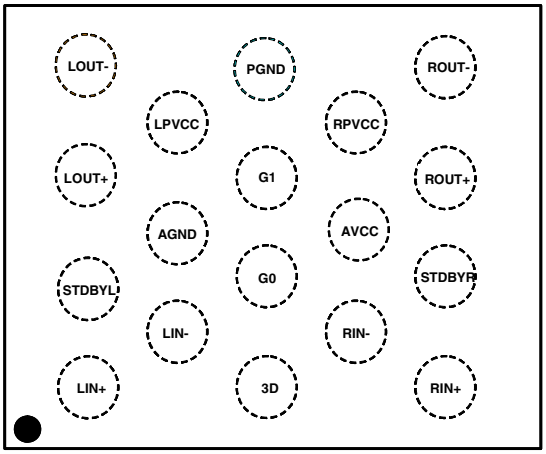
Two standby pins (active low) allow each channel to be switched off separately.

The TS4999 is available in a flip chip, 18-bump, lead-free package.

Flip chip 18-bump package



Pin connections (top view)



Contents

1 Absolute maximum ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	6	V
V_{in}	Input voltage(2)	GND to V_{CC}	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient (3)	200	°C/W
Pd	Power dissipation	Internally Limited(4)	
ESD	HBM: human body model(5)	2	kV
ESD	MM: machine model(6)	200	V
Latch-up	Latch-up immunity	200	mA
V_{STBY}	Standby pin voltage maximum voltage	GND to V_{CC}	V
	Lead temperature (soldering, 10 secs)	260	°C
	Output short-circuit protection(7)		

1. All voltages values are measured with respect to the ground pin.
2. The magnitude of input signal must never exceed V_{CC} + 0.3 V / GND - 0.3 V
3. Device is protected in case of over temperature by a thermal shutdown active at 150° C.
4. Exceeding the power derating curves during a long period, involves abnormal operating condition.
5. Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
6. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.
7. Implemented short-circuit protection protects the amplifier against damage by short-circuit between positive and negative outputs of each channel and between outputs and ground.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage(1)	2.4 to 5.5	V
V_{in}	Input voltage range	GND to V_{CC}	
VSTBY	Standby voltage input(2) Device ON Device OFF	 $1.4 \leq V_{STBY} \leq V_{CC}$ $GND \leq V_{STBY} \leq 0.4$(3)	V
RL	Load resistor	≥4	Ω
VIH	G0, G1, 3D, High Level Input Voltage(4)	$1.4 \leq V_{IH} \leq V_{CC}$	V
VIL	G0, G1, 3D, Low Level Input Voltage	$GND \leq V_{IL} \leq 0.4$	V
R_{thja}	Thermal Resistance Junction to Ambient (5)	90	°C/W

1. For V_{CC} from 2.4 to 2.5 V, the operating temperature range is reduced to $0° C \leq T_{amb} \leq 70° C$
2. Without any signal on V_{STBY}, the device will be in standby (internal 300 kΩ (+/-20 %) pull down resistor)
3. Minimum current consumption is obtained when V_{STBY} = GND
4. Between G0, G1, 3D pins and GND, there is an internal 300 kΩ (+/-20 %) pull-down resistor. When pins are floating, the gain is 3.5 dB and 3D effect is off. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).
5. With a 4-layer PCB.

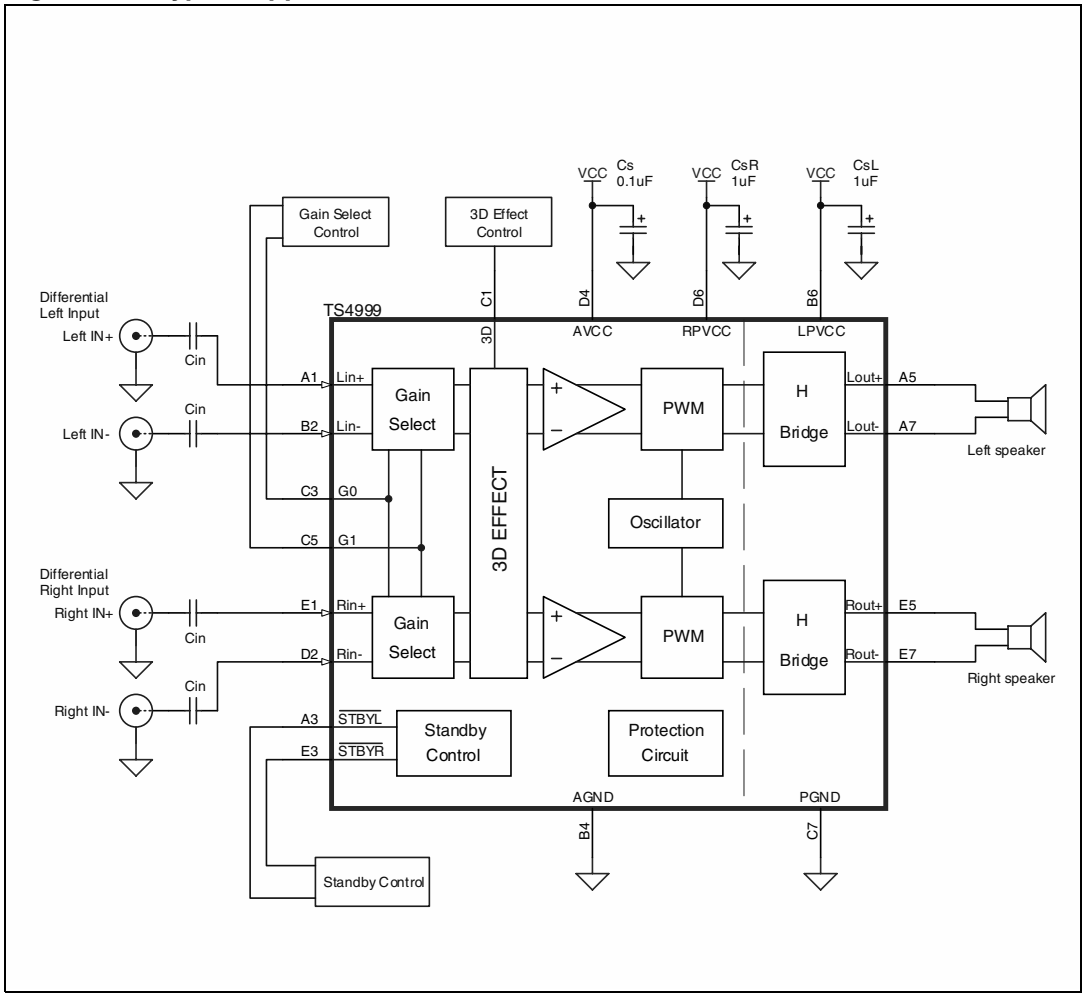
Table 3. 3D effect pin and STANDBY pins setting truth table

3D	STBYL	STBYR	3D Effect	Left channel	Right channel
0	0	0	X	STDBY	STDBY
0	0	1	OFF	STDBY	ON
0	1	0	OFF	ON	STDBY
0	1	1	OFF	ON	ON
1	0	0	X	STDBY	STDBY
1	0	1	N/A	N/A	N/A
1	1	0	N/A	N/A	N/A
1	1	1	ON	ON	ON

Note: When the 3D effect is switched on, both channels must be in operation or in shutdown mode at the same time.

2 Application information

Figure 1. Typical application schematic



Note: *See Section 4.9: Output filter considerations on page 29.*

Table 4. External component description

Components	Functional description
C_S, C_{SL}, C_{SR}	Supply capacitor that provides power supply filtering.
C_{in}	Input coupling capacitors that block the DC voltage at the amplifier input terminal. The capacitors also form a high pass filter with Z_{in} ($F_{cl} = 1 / (2 \times \pi \times Z_{in} \times C_{in})$). Note that the value of Z_{in} changes with each gain setting. These coupling capacitors are mandatory.

Table 5. Pin description

Bump	Name	Function
A1	LIN+	Left channel positive differential input
B2	LIN-	Left channel negative differential input
C1	3D	3D effect digital input pin
E1	RIN+	Right channel *positive* differential input
D2	RIN-	Right channel *negative* differential input
A3	STBYL	Standby input pin (active low) for left channel output
C3	G0	Gain select input pin (LSB)
E3	STBYR	Standby input pin (active low) for right channel output
B4	AGND	Analog ground
D4	AVCC	Analog supply voltage
A5	LOUT+	Left channel negative output
C5	G1	Gain select input pin (MSB)
E5	ROUT+	Right channel positive output
B6	LPVCC	Left channel power supply voltage
D6	RPVCC	Right channel power supply voltage
A7	LOUT-	Left channel negative output
C7	PGND	Power ground
E7	ROUT-	Right channel negative output

Table 6. Truth table for output gain settings

G1	G0	Gain value (dB)
0	0	3.5
0	1	6
1	0	9.5
1	1	12

Note: See Table 3 on page 4.

Table 7. Truth table for 3D effects pin settings

3D	3D effect
0	OFF
1	ON

3 Electrical characteristics

Table 8. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, both channels		5	7	mA
$I_{STANDBY}$	Standby current	No input signal, Vstdby = GND		1	2	µA
Voo	Output offset voltage	Floating inputs, RL = 8Ω, G = 3.5dB, 3D effect off			20	mV
Po	Output power	THD = 1% max, F = 1kHz, R_L = 4Ω		2.25		W
		THD = 1% max, F = 1kHz, R_L = 8Ω		1.35		
		THD = 10% max, F = 1kHz, R_L = 4Ω		2.8		W
		THD = 10% max, F = 1kHz, R_L = 8Ω		1.7		W
THD+N	Total harmonic distortion + noise	Po = 0.9W/Ch, G = 6dB, F=1kHz, R_L = 8Ω		0.2		%
Efficiency	Efficiency per channel	Po = 2.3 W_{RMS}, R_L = 4Ω +15µH		82		%
		Po = 1.4 W_{RMS}, R_L = 8Ω + 15µH		89		
PSRR	Power supply rejection ratio with inputs grounded	C_{in} = 1µF (1),3D effects off F = 217Hz, R_L = 8Ω, gain = 6dB, Vripple = 200mVpp, Inputs grounded		65		dB
Crosstalk	Channel separation	F = 1kHz, R_L = 8Ω, 3D effects off		100		dB
CMRR	Common mode rejection ratio	C_{in}=1µF, F = 217Hz, R_L = 8Ω, gain = 6dB, ΔV_{IC} = 200mV_{pp}, 3D effects OFF		57		dB
Gain	Gain value with no load	G1 = G0 = "0"	3	3.5	4	dB
		G1 = "0" & G0 = "1"	5.5	6	6.5	
		G1 = "1" & G0 = "0"	9	9.5	10	
		G1 = G0 = "1"	11.5	12	12.5	
Z_{IN}	Single-ended input impedance referred to GND	G1 = G0 = 3D = "0" or G1 = "0" & G0 = "1" & 3D = "0" or G1 = "1" & G0 = "0" & 3D = "0"	24	30	36	kΩ
		G1 = "1" & G0 = "1" & 3D = "0"	12	15	18	kΩ
		G1 = G0 = "0" & 3D = "1" or G1 = "0" & G0 = "1" & 3D = "1" or G1 = "1" & G0 = "0" & 3D = "1"	13.5	17.1	20.5	kΩ
		G1 = "1" & G0 = "1" & G3D = "1"	6.5	8.6	10.5	
F_{PWM}	Pulse width modulator base frequency		190	280	370	kHz
SNR	Signal to noise ratio	P_o = 1.3W, A-weighting, R_L = 8Ω, Gain = 6dB, 3D effects OFF		99		dB
t_{WU}	Wake-up time	Total wake-up time(2)	9	13	16.5	ms

Table 8. V_{CC} = +5 V, GND = 0 V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time	Standby time[2]	11	15.8	20	ms
V_N	Output voltage noise	F = 20Hz to 20kHz, A-weighted, Gain = 3.5dB Filterless, 3D effect off, R_L = 4Ω Filterless, 3D effect on, R_L = 4Ω With LC output filter, 3D effect off, R_L = 4Ω With LC output filter, 3D effect on, R_L = 4Ω Filterless, 3D effect off, R_L = 8Ω Filterless, 3D effect on, R_L = 8Ω With LC output filter, 3D effect off, R_L = 8Ω With LC output filter, 3D effect on, R_L = 8Ω		31 50 30 48 32 51 31 50		μV_{RMS}

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the super-imposed sinus signal to V_{CC} at f = 217 Hz with fixed Cin cap (input decoupling capacitor).
2. See *Section 4.6: Wakeup (t_{WU}) and shutdown (t_{STBY}) times on page 26*.

Table 9. V_{CC} = +3.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, both channels		3.5	5.5	mA
$I_{STANDBY}$	Standby current	No input signal, Vstdby = GND		1	2	µA
Voo	Output offset voltage	Floating inputs, RL = 8Ω, G = 3.5dB, 3D effect off			20	mV
Po	Output power	THD = 1% max, F = 1kHz, R_L = 4Ω		1.15		W
		THD = 1% max, F = 1kHz, R_L = 8Ω		0.7		
		THD = 10% max, F = 1kHz, R_L = 4Ω		1.45		W
		THD = 10% max, F = 1kHz, R_L = 8Ω		0.86		W
THD+N	Total harmonic distortion + noise	Po = 0.45W/Ch, G = 6dB, F=1kHz, R_L = 8Ω		0.15		%
Efficiency	Efficiency per channel	Po = 1.15 W_{RMS}, R_L = 4Ω +15µH		82		%
		Po = 0.7 W_{RMS}, R_L = 8Ω + 15µH		89		
PSRR	Power supply rejection ratio with inputs grounded	C_{in} = 1µF (1),3D effects off F = 217Hz, R_L = 8Ω, gain = 6dB, Vripple = 200mVpp, inputs grounded		64		dB
Crosstalk	Channel separation	F = 1kHz, R_L = 8Ω, 3D effects off		102		dB
CMRR	Common mode rejection ratio	C_{in}=1µF, F = 217Hz, R_L = 8Ω, gain = 6dB, ΔV_{IC} = 200mV_{pp}, 3D effects off		55		dB
Gain	Gain value with no load	G1 = G0 = "0"	3	3.5	4	dB
		G1 = "0" & G0 = "1"	5.5	6	6.5	
		G1 = "1" & G0 = "0"	9	9.5	10	
		G1 = G0 = "1"	11.5	12	12.5	
Z_{IN}	Single-ended input impedance referred to GND	G1 = G0 = 3D = "0" or G1 = "0" & G0 = "1" & 3D = "0" or G1 = "1" & G0 = "0" & 3D = "0"	24	30	36	kΩ
		G1 = "1" & G0 = "1" & 3D = "0"	12	15	18	kΩ
		G1 = G0 = "0" & 3D = "1" or G1 = "0" & G0 = "1" & 3D = "1" or G1 = "1" & G0 = "0" & 3D = "1"	13.5	17.1	20.5	kΩ
		G1 = "1" & G0 = "1" & G3D = "1"	6.5	8.6	10.5	kΩ
F_{PWM}	Pulse width modulator base frequency		190	280	370	kHz
SNR	Signal to noise ratio	P_o = 0.67W, A-weighting, R_L = 8Ω, Gain = 6dB, 3D effects OFF		97		dB
t_{WU}	Wake-up time	Total wake-up time(2)	7.5	11.3	15	ms

Table 9. V_{CC} = +3.6V, GND = 0V, T_{amb} = 25°C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time	Standby time[2]	10	13.8	18	ms
V_N	Output voltage noise	F = 20Hz to 20kHz, A-Weighted, Gain = 3.5dB Filterless, 3D effect off, R_L = 4Ω Filterless, 3D effect on, R_L = 4Ω With LC output filter, 3D effect off, R_L = 4Ω With LC output filter, 3D effect on, R_L = 4Ω Filterless, 3D effect off, R_L = 8Ω Filterless, 3D effect on, R_L = 8Ω With LC output filter, 3D effect off, R_L = 8Ω With LC output filter, 3D effect on, R_L = 8Ω		29 49 28 48 29 50 29 50		μV_{RMS}

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the super-imposed sinus signal to V_{CC} at f = 217 Hz with fixed Cin cap (input decoupling capacitor).
2. See *Section 4.6: Wakeup (t_{WU}) and shutdown (t_{STBY}) times on page 26*.

Table 10. V_{CC} = +2.5 V, GND = 0V, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply current	No input signal, no load, both channels		2.8	4	mA
$I_{STANDBY}$	Standby current	No input signal, Vstdby = GND		1	2	µA
Voo	Output offset voltage	Floating inputs, RL = 8Ω, G = 3.5dB, 3D effect off			20	mV
Po	Output power	THD = 1% max, F = 1kHz, R_L = 4Ω		0.53		W
		THD = 1% max, F = 1kHz, R_L = 8Ω		0.33		
		THD = 10% max, F = 1kHz, R_L = 4Ω		0.67		W
		THD = 10% max, F = 1kHz, R_L = 8Ω		0.4		W
THD+N	Total harmonic distortion + noise	Po = 0.2W/Ch, G = 6dB, F=1kHz, R_L = 8Ω		0.07		%
Efficiency	Efficiency per channel	Po = 0.52 W_{RMS}, R_L = 4Ω+15µH		81		%
		Po = 0.33 W_{RMS}, R_L = 8Ω+ 15µH		88		
PSRR	Power supply rejection ratio with inputs grounded	C_{in} = 1µF (1),3D effects off F = 217Hz, R_L = 8Ω, gain = 6dB, Vripple = 200mVpp, Inputs grounded		63		dB
Crosstalk	Channel separation	F = 1kHz, R_L = 8Ω, 3D effects off		104		dB
CMRR	Common mode rejection ratio	C_{in}=1µF, F = 217Hz, R_L = 8Ω, gain = 6dB, ΔV_{IC} = 200mV_{pp}, 3D effects off		55		dB
Gain	Gain value with no load	G1 = G0 = "0"	3	3.5	4	dB
		G1 = "0" & G0 = "1"	5.5	6	6.5	
		G1 = "1" & G0 = "0"	9	9.5	10	
		G1 = G0 = "1"	11.5	12	12.5	
Z_{IN}	Single-ended input impedance referred to GND	G1 = G0 = 3D = "0" or G1 = "0" & G0 = "1" & 3D = "0" or G1 = "1" & G0 = "0" & 3D = "0"	24	30	36	kΩ
		G1 = "1" & G0 = "1" & 3D = "0"	12	15	18	kΩ
		G1 = G0 = "0" & 3D = "1" or G1 = "0" & G0 = "1" & 3D = "1" or G1 = "1" & G0 = "0" & 3D = "1"	13.5	17.1	20.5	kΩ
		G1 = "1" & G0 = "1" & G3D = "1"	6.5	8.6	10.5	kΩ
F_{PWM}	Pulse width modulator base frequency		190	280	370	kHz
SNR	Signal to noise ratio	P_o = 0.3W, A-weighting, R_L = 8Ω, Gain = 6dB, 3D effects OFF		94		dB
t_{WU}	Wake-up time	Total wake-up time(2)	3	7.8	12	ms

Table 10. V_{CC} = +2.5 V, GND = 0V, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{STBY}	Standby time	Standby time(2)	8	12	16	ms
V_N	Output voltage noise	F = 20Hz to 20kHz, A-Weighted, Gain = 3.5dB Filterless, 3D effect off, R_L = 4Ω Filterless, 3D effect on, R_L = 4Ω With LC output filter, 3D effect off, R_L = 4Ω With LC output filter, 3D effect on, R_L = 4Ω Filterless, 3D effect off, R_L = 8Ω Filterless, 3D effect on, R_L = 8Ω With LC output filter, 3D effect off, R_L = 8Ω With LC output filter, 3D effect on, R_L = 8Ω		28 47 27 45 28 48 28 47		μV_{RMS}

1. Dynamic measurements - 20*log(rms(Vout)/rms(Vripple)). Vripple is the super-imposed sinus signal to V_{CC} at f = 217 Hz with fixed Cin cap (input decoupling capacitor).
2. See *Section 4.6: Wakeup (t_{WU}) and shutdown (t_{STBY}) times on page 26*.

3.1 Electrical characteristic curves

The graphs shown in this section use the following abbreviations.

- R_L+ 15 µH or 30 µH = pure resistor + very low series resistance inductor.
- Filter = LC output filter (1 µF+ 30 µH for 4 Ω and 0.5 µF+15 µH for 8 Ω).

All measurements are done with C_{SL}= C_{SR}=1 µF and C_S = 100 nF (see *Figure 2*), except for the PSRR where C_{SL}, C_{SR} is removed (see *Figure 3*).

Figure 2. Measurement test diagram

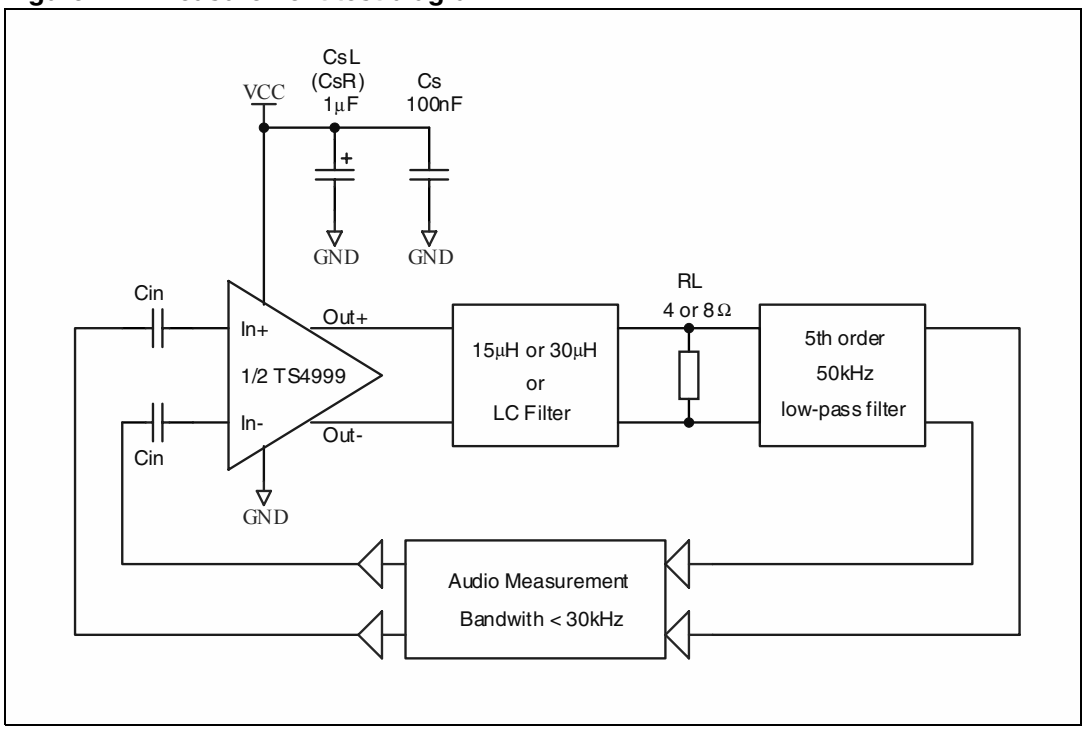


Figure 3. PSRR measurement test diagram

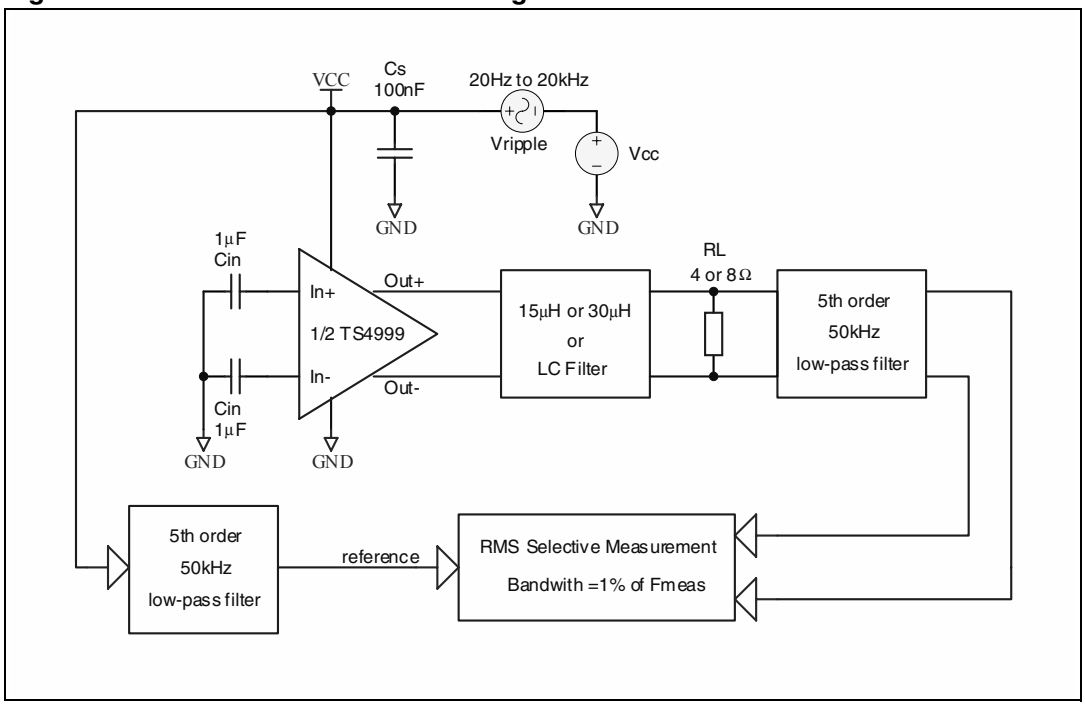


Figure 4. Current consumption vs. power supply voltage

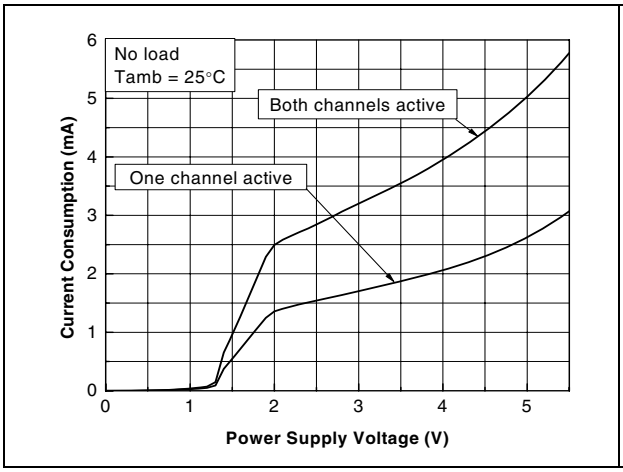


Figure 5. Current consumption vs. standby voltage (one channel)

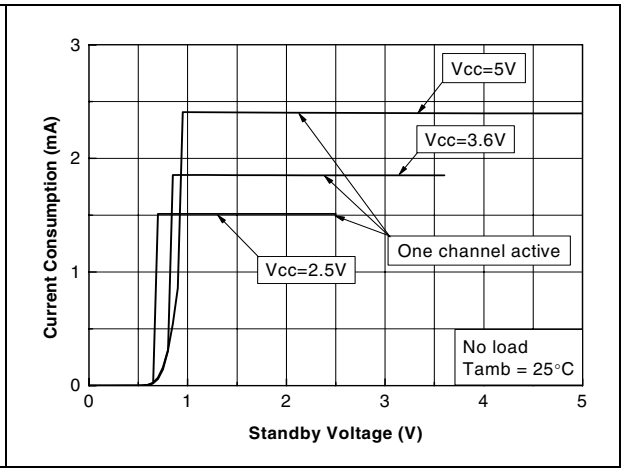


Figure 6. Standby current consumption vs. power supply voltage

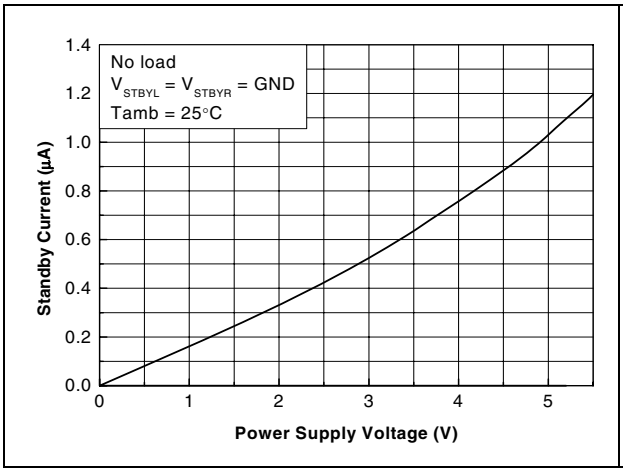


Figure 7. Efficiency vs. output power (one channel)

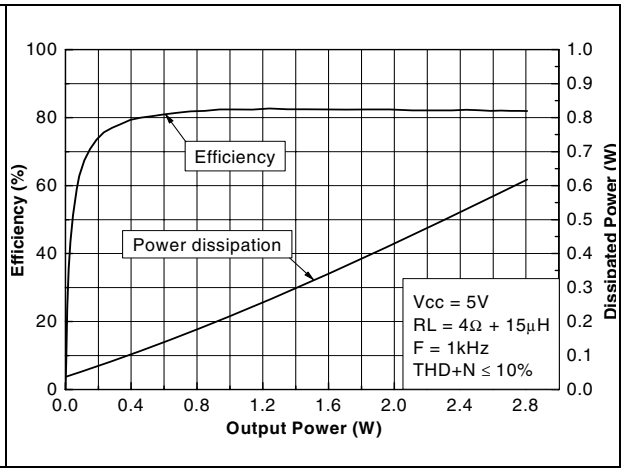


Figure 8. Efficiency vs. output power (one channel)

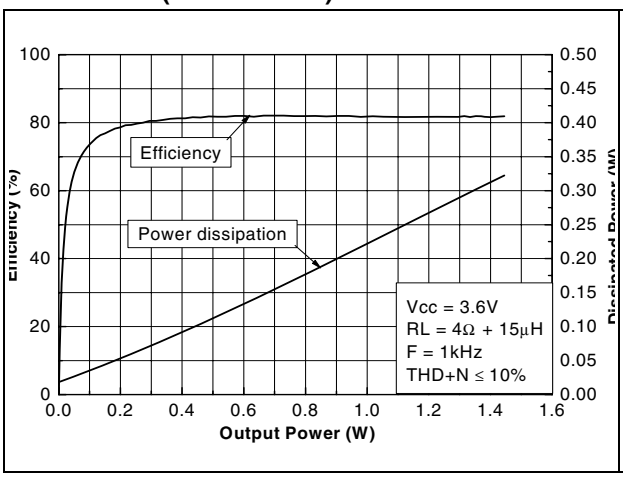


Figure 9. Efficiency vs. output power (one channel)

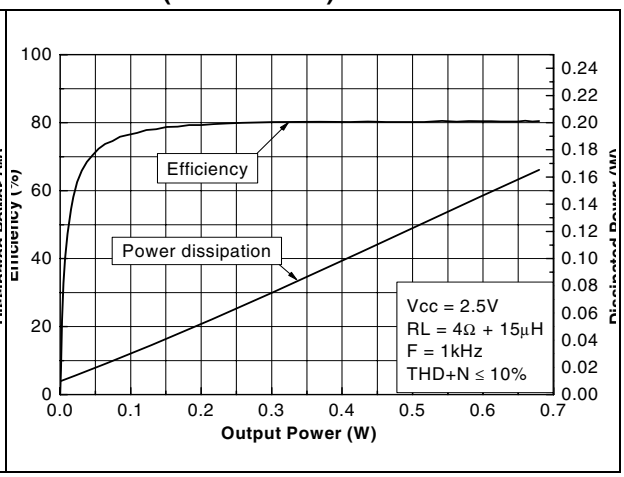


Figure 10. Efficiency vs. output power (one channel)

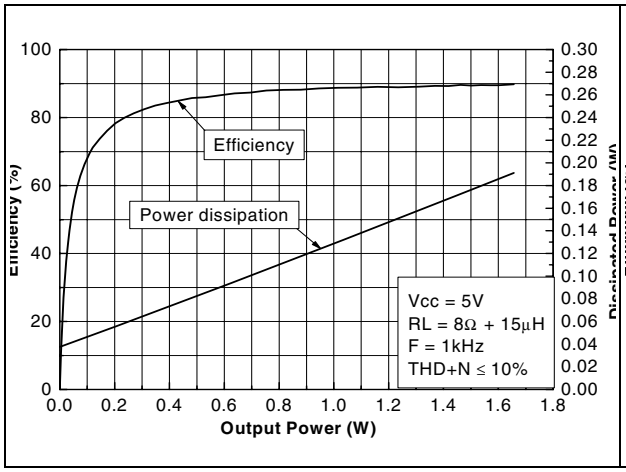


Figure 11. Efficiency vs. output power (one channel)

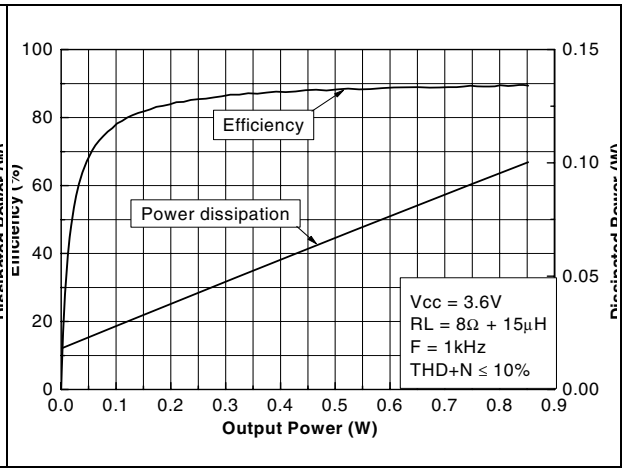


Figure 12. Efficiency vs. output power (one channel)

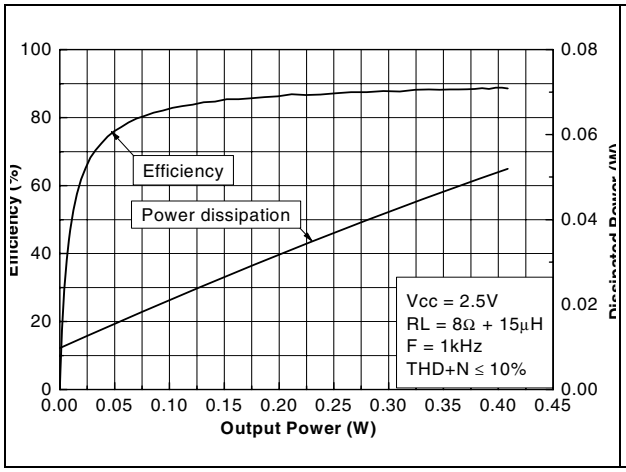


Figure 13. THD+N vs. output power

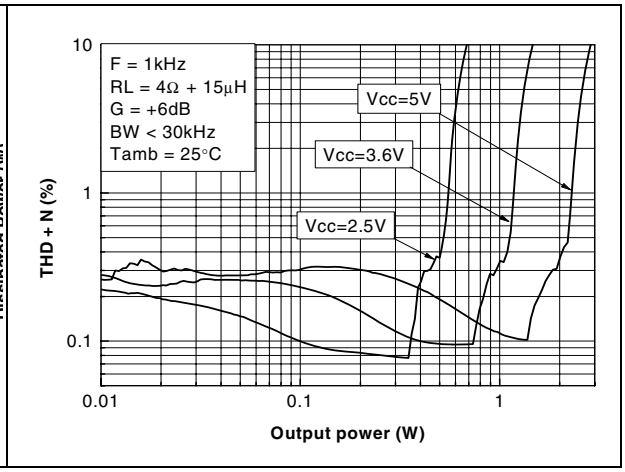


Figure 14. THD+N vs. output power

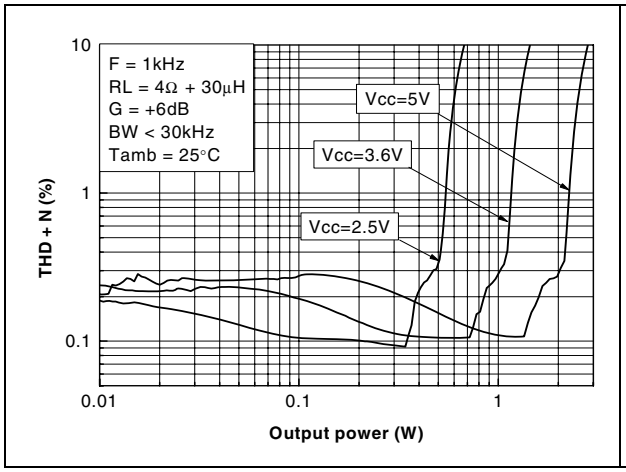


Figure 15. THD+N vs. output power

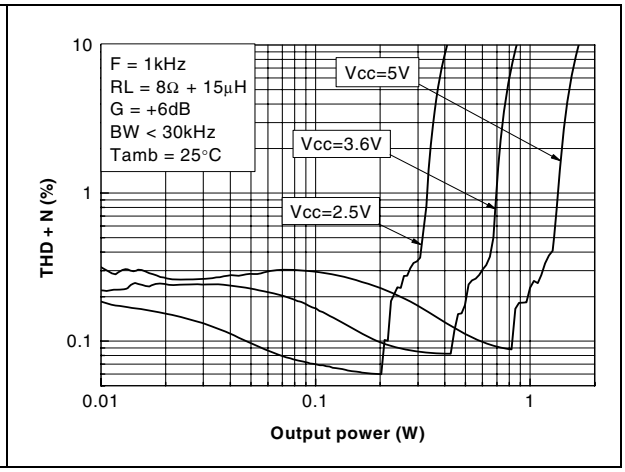


Figure 16. THD+N vs. output power

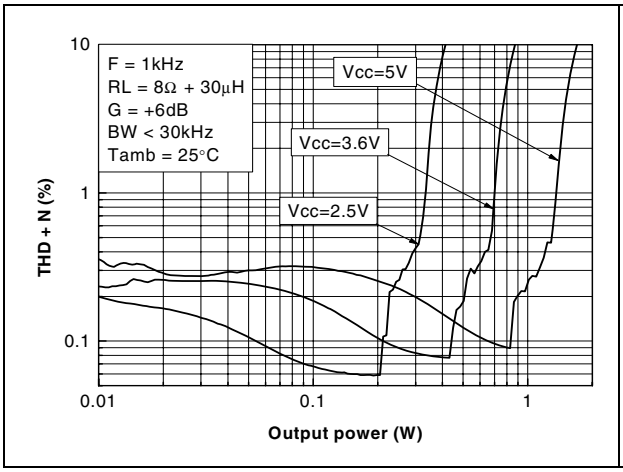


Figure 17. THD+N vs. frequency

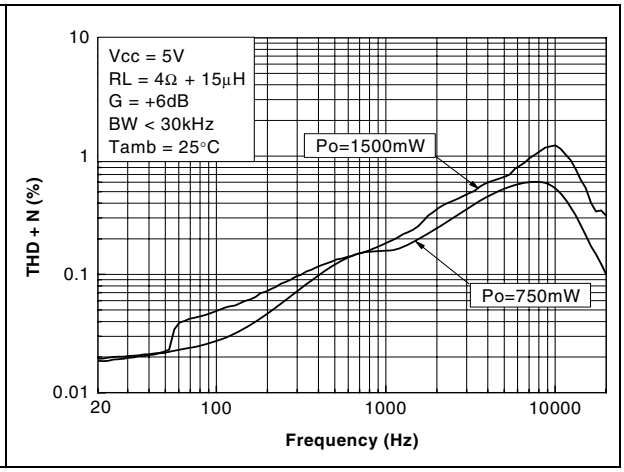


Figure 18. THD+N vs. frequency

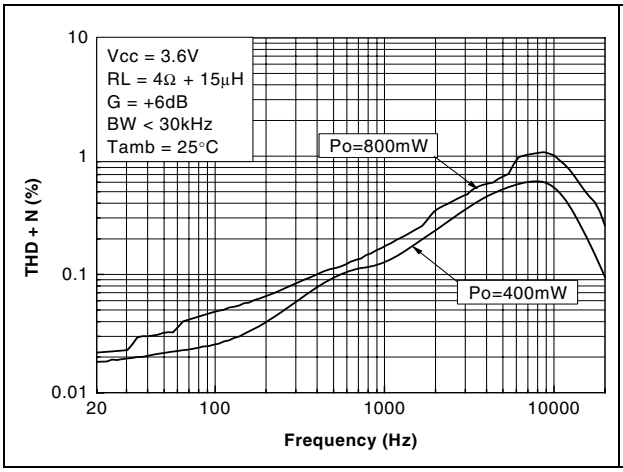


Figure 19. THD+N vs. frequency

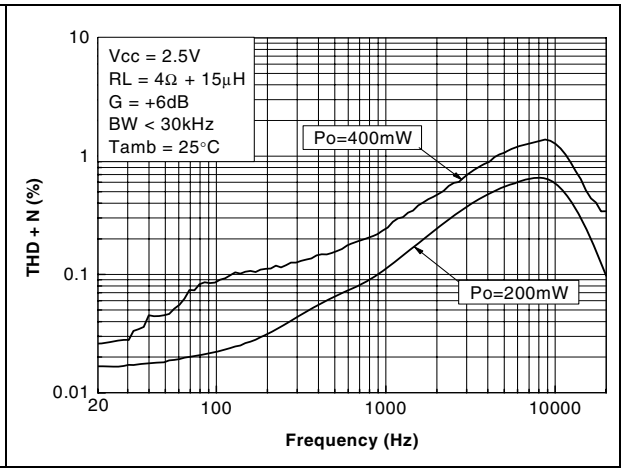


Figure 20. THD+N vs. frequency

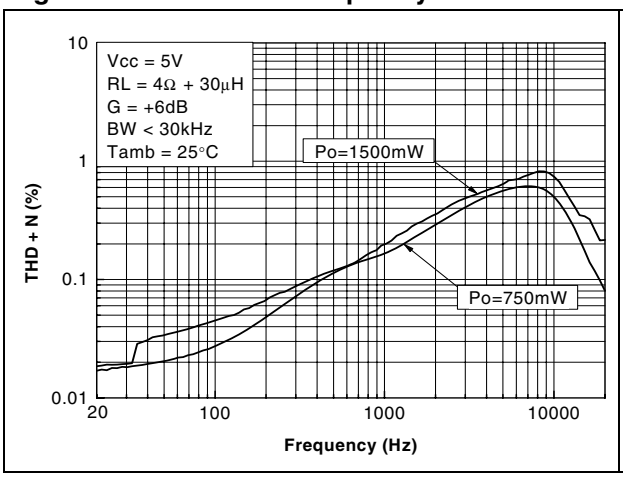


Figure 21. THD+N vs. frequency

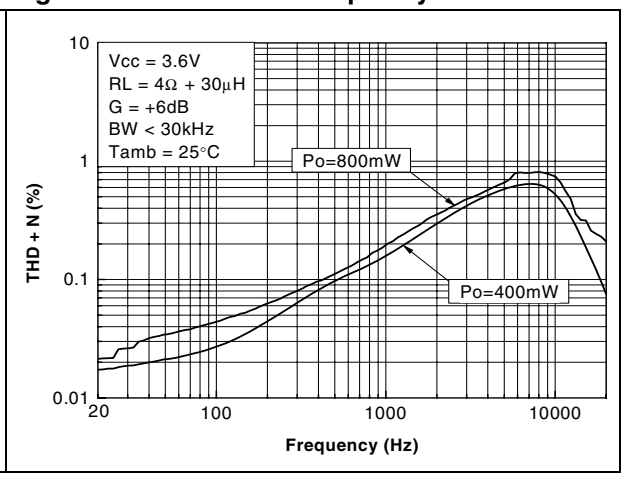


Figure 22. THD+N vs. frequency

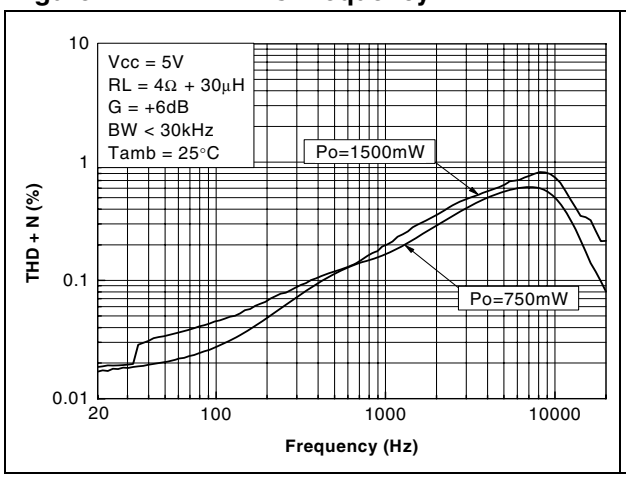


Figure 23. THD+N vs. frequency

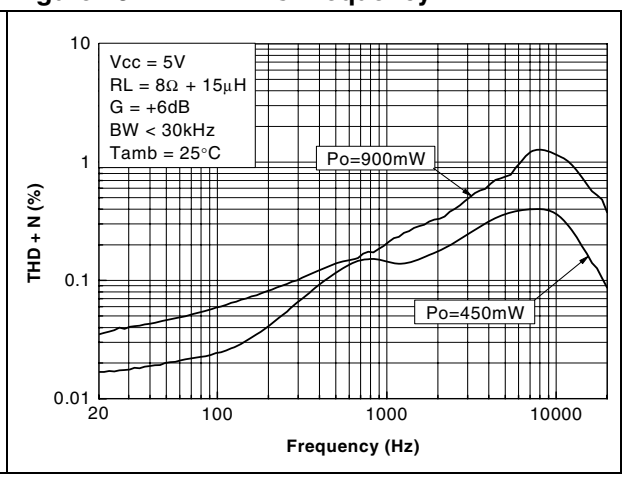


Figure 24. THD+N vs. frequency

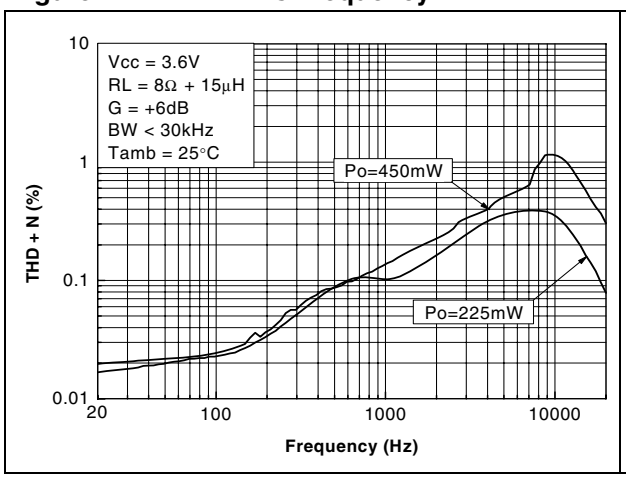


Figure 25. THD+N vs. frequency

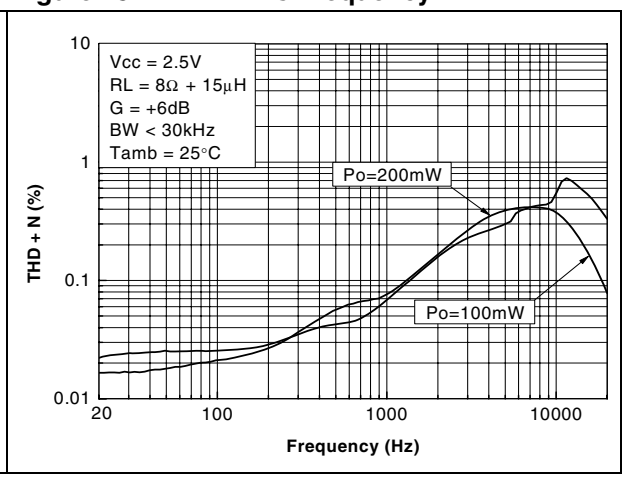


Figure 26. THD+N vs. frequency

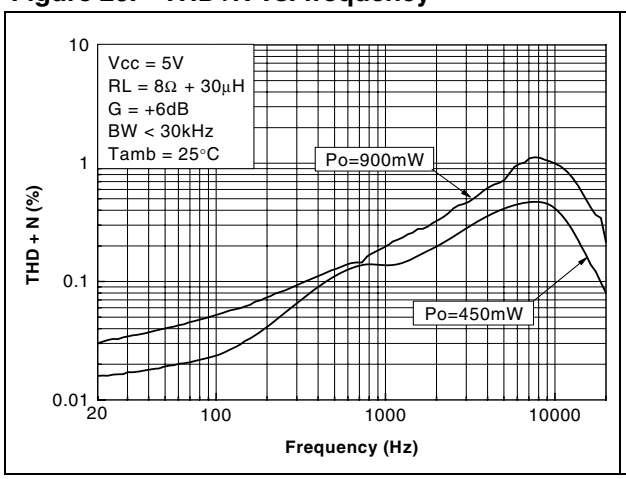


Figure 27. THD+N vs. frequency

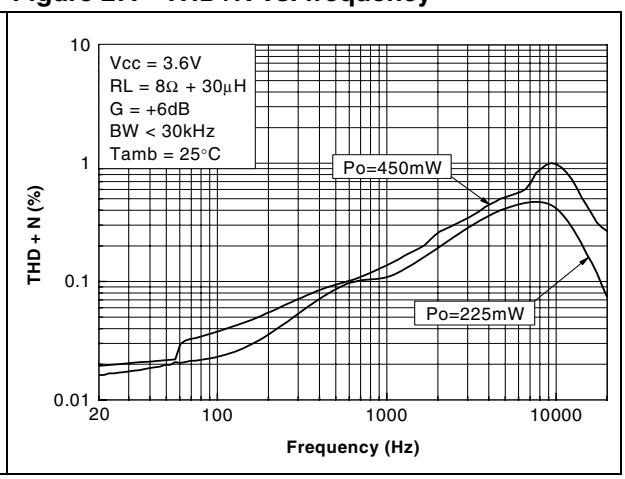


Figure 28. THD+N vs. frequency

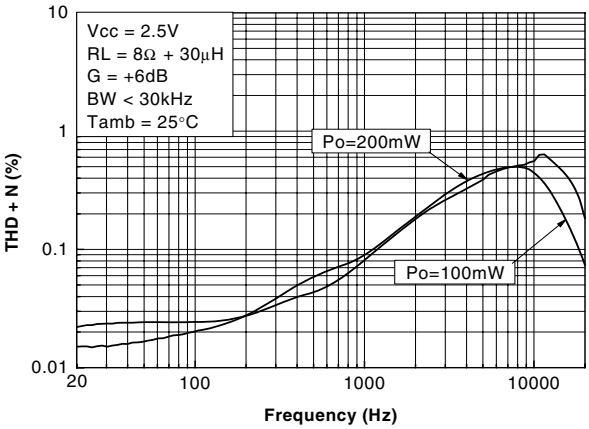


Figure 29. Output power vs. power supply voltage

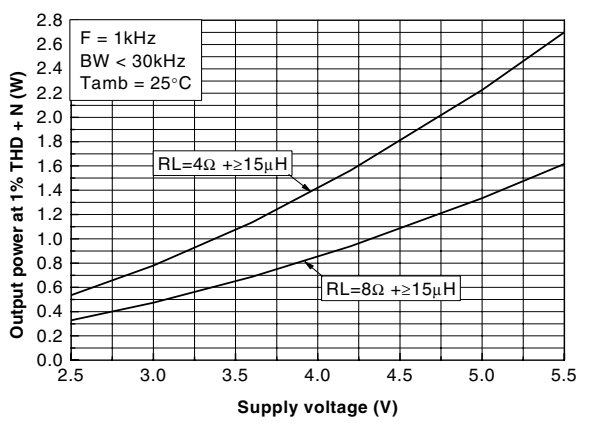


Figure 30. Output power vs. power supply voltage

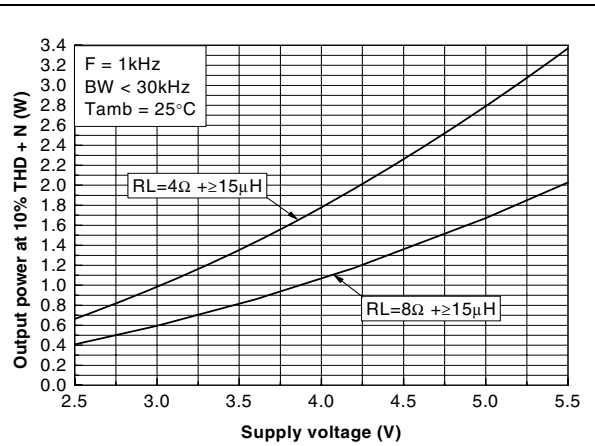


Figure 31. Crosstalk vs. frequency (3D effect off)

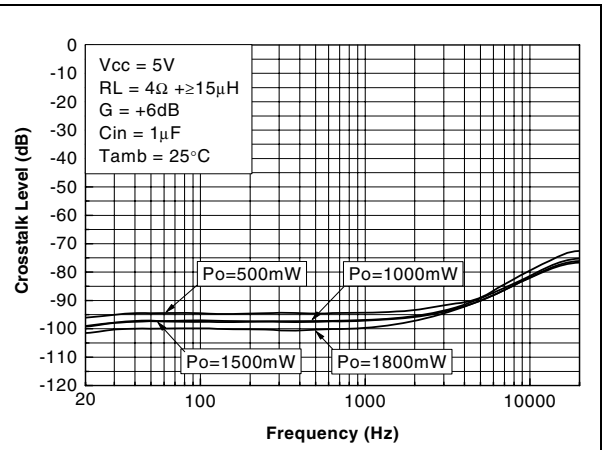


Figure 32. Crosstalk vs. frequency (3D effect off)

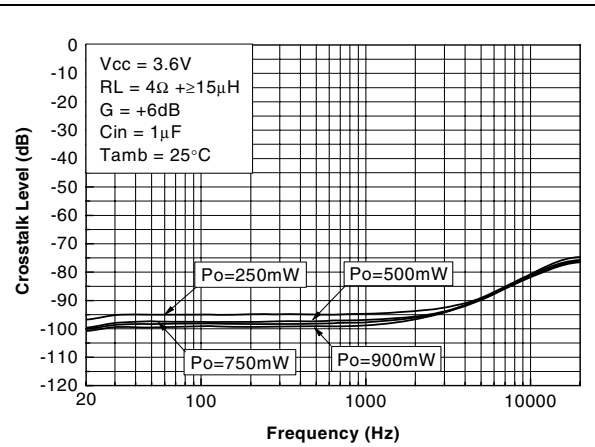


Figure 33. Crosstalk vs. frequency (3D effect off)

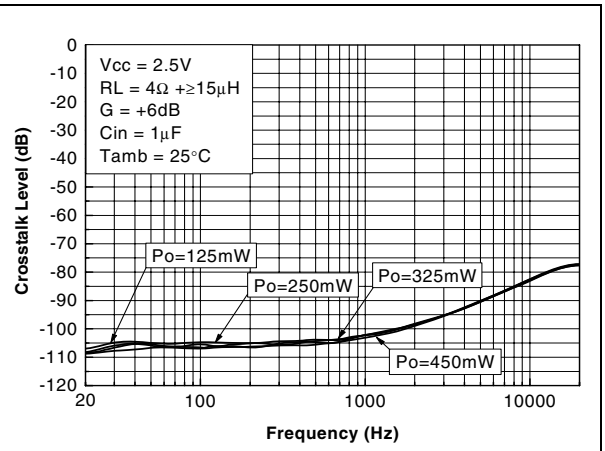


Figure 34. Crosstalk vs. frequency (3D effect off)

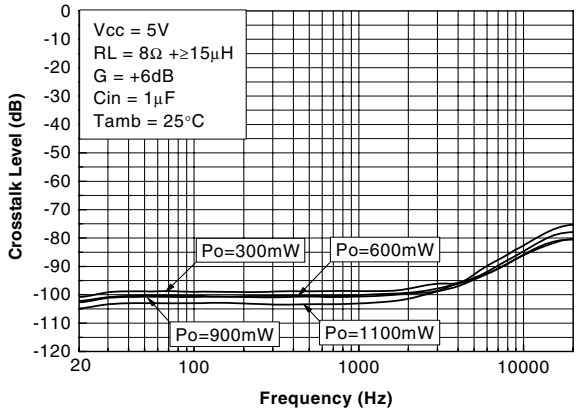


Figure 35. Crosstalk vs. frequency (3D effect off)

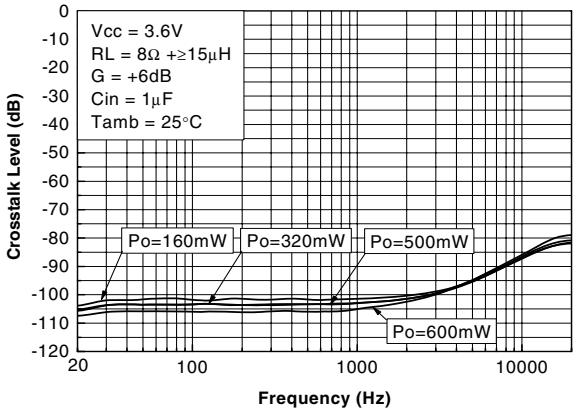


Figure 36. Crosstalk vs. frequency (3D effect off)

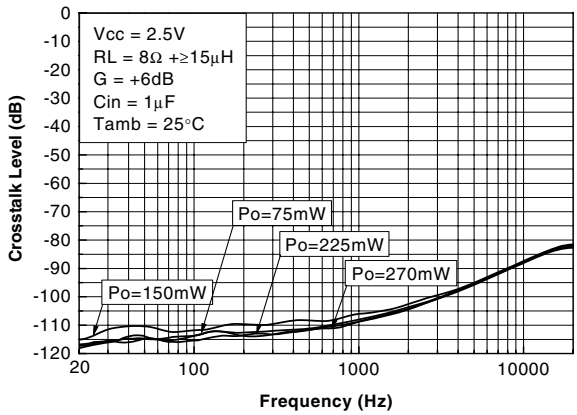


Figure 37. Gain vs. frequency (3D effect off)

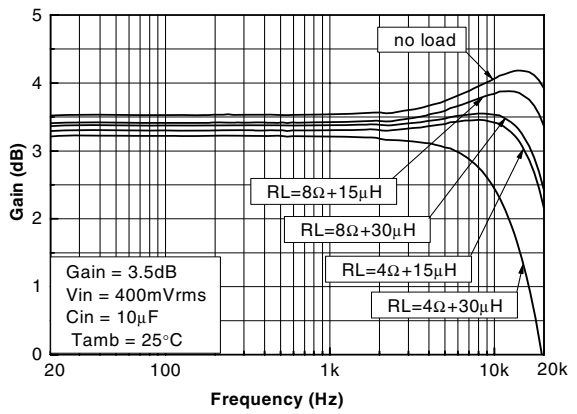


Figure 38. Gain vs. frequency (3D effect off)

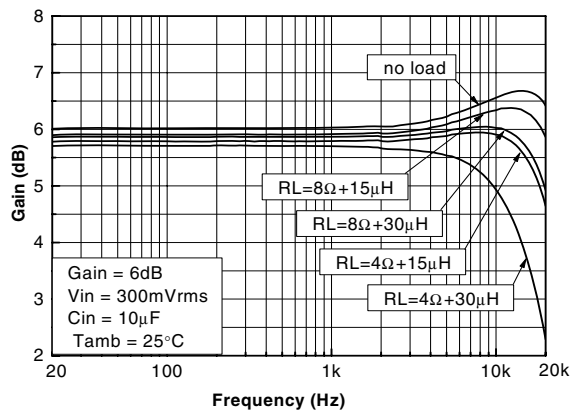


Figure 39. Gain vs. frequency (3D effect off)

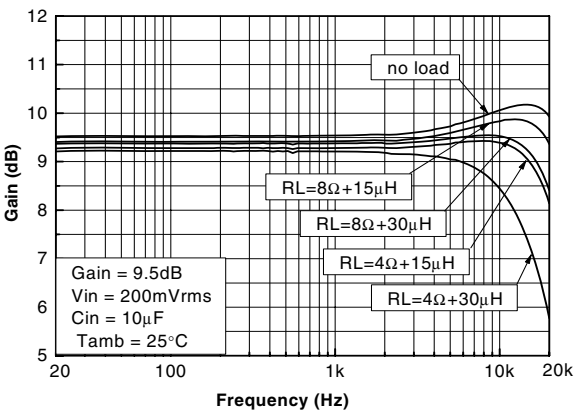


Figure 40. Gain vs. frequency (3D effect off)

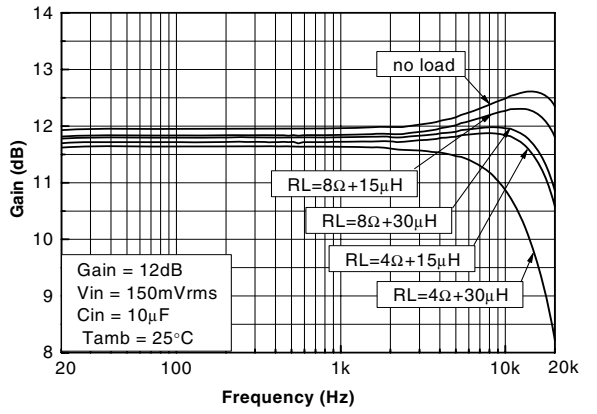


Figure 41. PSRR vs. frequency (3D effect off)

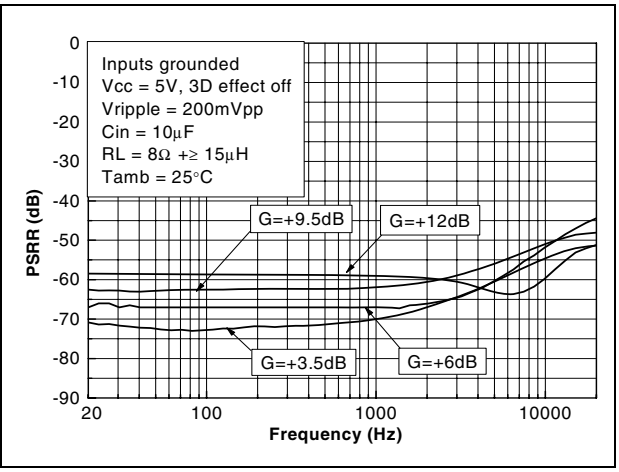


Figure 42. PSRR vs. frequency (3D effect off)

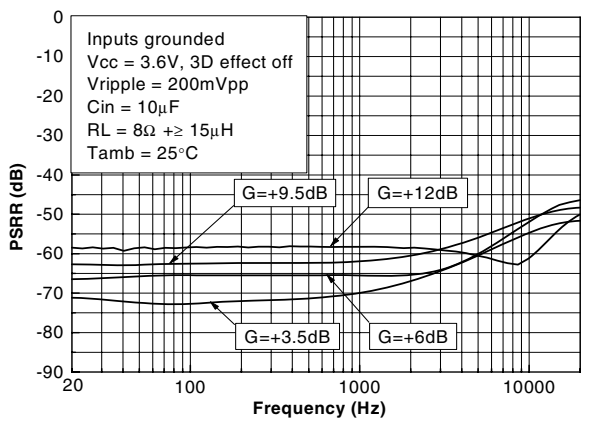


Figure 43. PSRR vs. frequency (3D effect off)

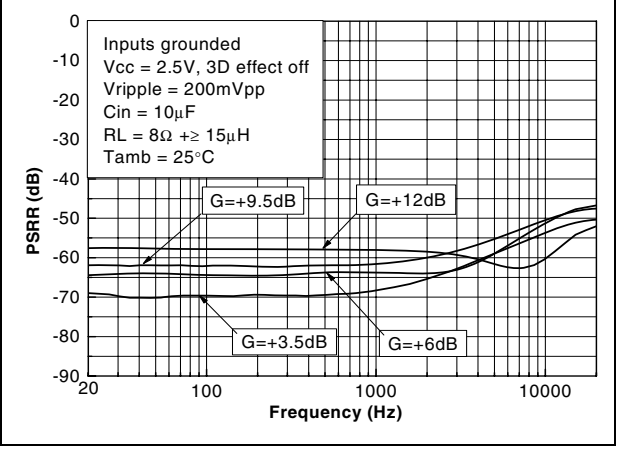


Figure 44. PSRR vs. frequency (3D effect on)

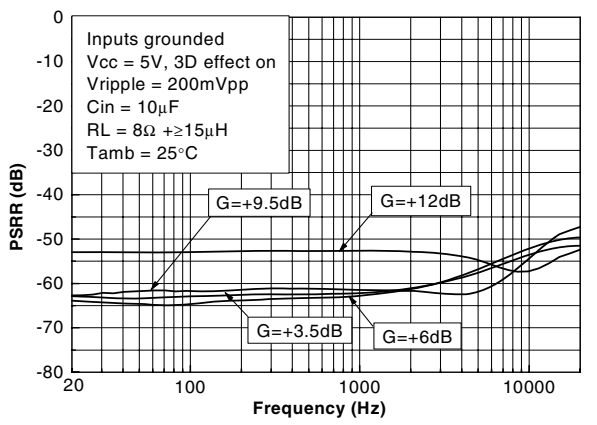


Figure 45. PSRR vs. frequency (3D effect on)

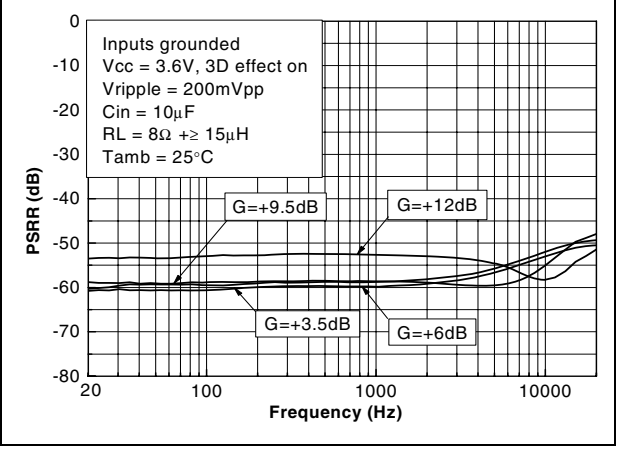


Figure 46. PSRR vs. frequency (3D effect on)

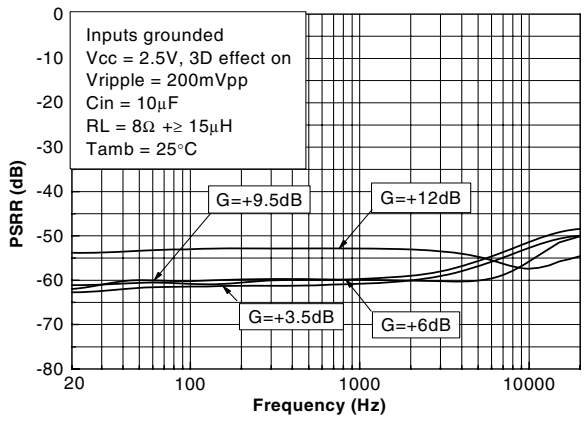


Figure 47. CMRR vs. frequency (3D effect off)

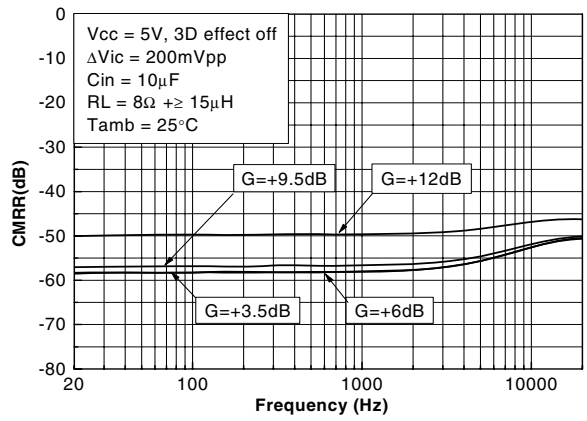


Figure 48. CMRR vs. frequency (3D effect off)

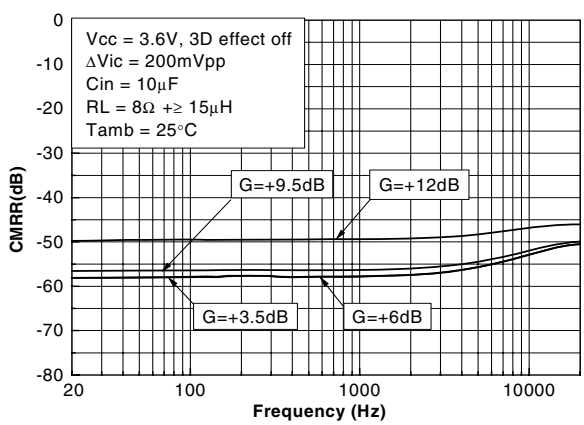


Figure 49. CMRR vs. frequency (3D effect off)

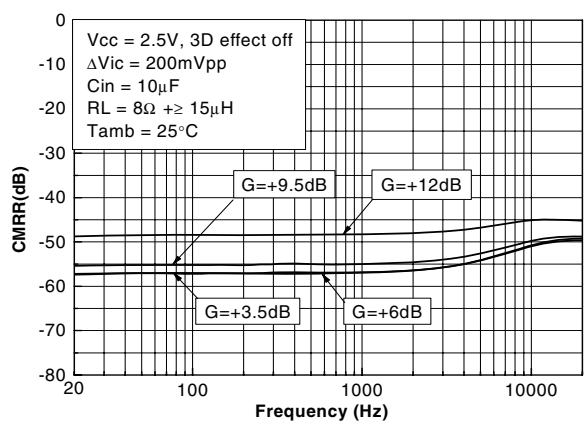


Figure 50. CMRR vs. frequency (3D effect on)

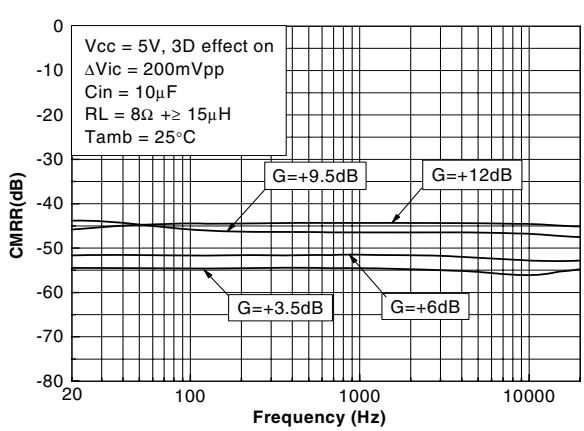


Figure 51. CMRR vs. frequency (3D effect on)

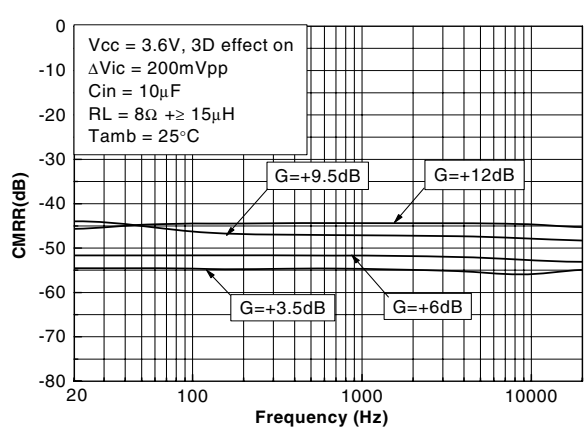


Figure 52. CMRR vs. frequency (3D effect on)

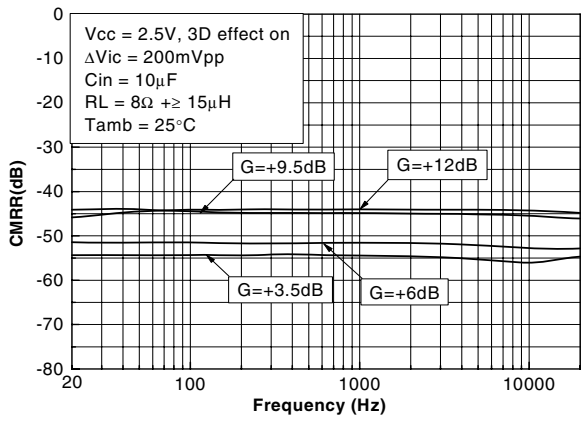


Figure 53. Power derating curves

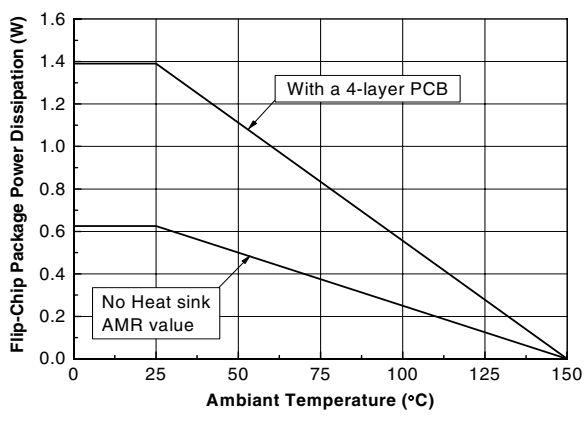


Figure 54. Startup and shutdown phase V_{CC}= 5 V, G= 6 dB, C_{in}= 1 µF, V_{in}= 2 V_{pp}, F= 500 Hz

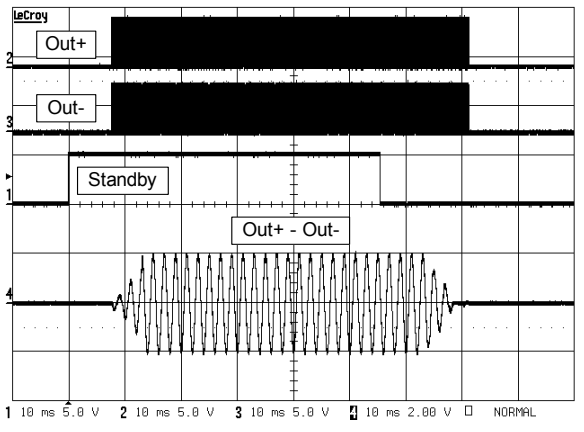
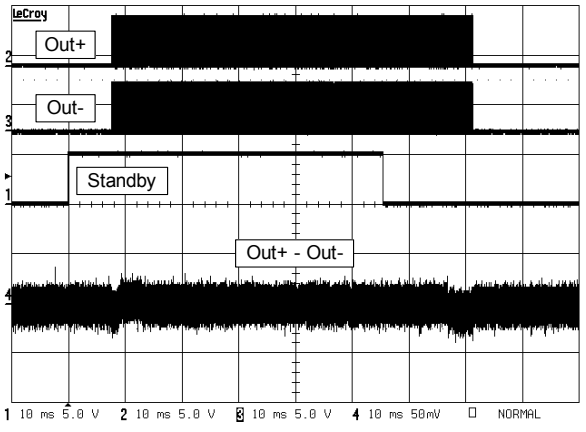


Figure 55. Startup and shutdown phase V_{CC}= 5 V, G= 6 dB, C_{in}= 1 µF, inputs grounded



4 Application information

4.1 Differential configuration principle

The TS4999 is a monolithic fully-differential input/output class D stereo power amplifier. The TS4999 also features 3D effect enhancement that can be switched on or off by one digital pin. Additionally, since the load is connected differentially compared to a single-ended topology, the output is four times higher for the same power supply voltage.

A fully-differential amplifier offers the following advantages.

- A high PSRR (power supply rejection ratio).
- A high common mode noise rejection.
- Virtually zero pop with no additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers.
- Easier interfacing with differential output audio DACs.

4.2 Gain settings

In the flat region of the frequency-response curve (no input coupling capacitor or internal feedback loop + load effect), the differential gain can be set to 3.5, 6, 9.5 or 12 dB, depending on the logic level of the G0 and G1 pins, as shown in *Table 11*.

Table 11. Gain settings with G0 and G1 pins

G1	G0	Gain (dB)	Gain (V/V)
0	0	3.5	1.5
0	1	6	2
1	0	9.5	3
1	1	12	4

Note: Between pins G0, G1 and GND there is an internal 300 kΩ (+/-20%) resistor. When the pins are floating, the gain is 6 dB. In full standby (left and right channels OFF), these resistors are disconnected (HiZ input).

4.3 3D effect enhancement

The TS4999 features 3D audio effects which can be switched off and switched on through input pin 3D when used as a digital interface. The relation between the logic level of this pin and the on/off 3D effect is shown in *Table 3 on page 4* and *Table 7 on page 6*.

The 3D audio effect evokes the perception of spatial hearing of stereo audio signals and improves this effect in cases where the stereo speakers are too close to each other, such as in small or portable devices.

The perceived amount of 3D effect also depends on many factors such as speaker position, distance between speakers, listener/frequency spectrum of the audio signal, as well as the difference of signal between the left and right channel.

In some cases, the speaker volume can increase when the 3D effect is switched on. This factor is dependent on the composition and frequency spectrum of listened stereo audio signal.

Note: 1 When the 3D effect is switched on, both channels must be in operation or shutdown mode at the same time.

2 Between pin 3D and GND there is an internal 300 kΩ (+/-20%) resistor. When the pin is floating, the 3D effect is off. In full standby (left and right channels OFF), this resistor is disconnected (HiZ input).

4.4 Low frequency response

If a low frequency bandwidth limitation is required, input coupling capacitors can be used. In the low frequency region, the input coupling capacitor C_{in} starts to have an effect. C_{in} forms, with the input impedance Z_{in}, a first order high-pass filter with a -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot C_{in}}$$

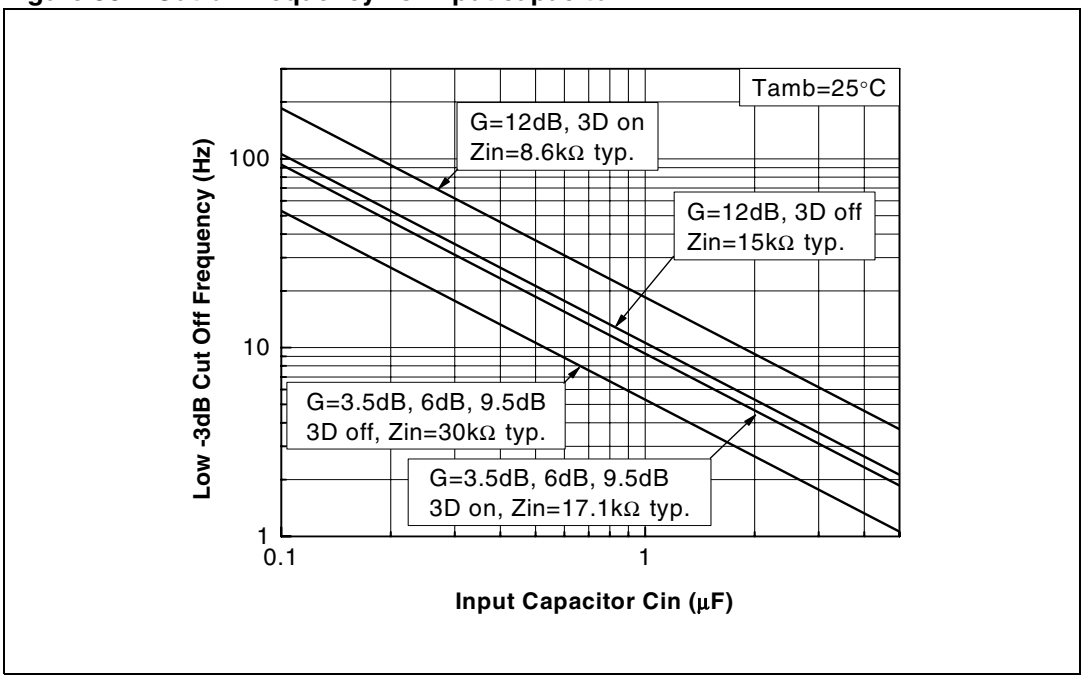
So, for a desired cut-off frequency F_{CL}, C_{in} is calculated as follows:

$$C_{in} = \frac{1}{2 \cdot \pi \cdot Z_{in} \cdot F_{CL}}$$

with F_{CL} in Hz, Z_{in} in Ω and C_{in} in F.

The input impedance Z_{in} is for the whole power supply voltage range and changes with the gain setting. There is also a tolerance around the typical values (see *Table 8*, *Table 9* and *Table 10*.

Figure 56. Cut-off frequency vs. input capacitor



4.5 Circuit decoupling

Power supply capacitors, referred to as C_S, C_{SL} and C_{SR}, are needed to correctly bypass the TS4999.

The TS4999 has a typical switching frequency of 280 kHz and an output fall and rise time of approximately 5 ns. Due to these very fast transients, careful decoupling is mandatory.

A 1 µF ceramic capacitor between each PVCC and PGND (C_{SL}, C_{SR}) and one additional ceramic capacitor between AVCC and AGND 0.1 µF (C_S) are sufficient, but they must be located as close as possible to the TS4999 in order to avoid any extra parasitic inductance or resistance created by a long track wire. Parasitic loop inductance, in relation to di/dt, introduces overvoltage that decreases the global efficiency of the device and may cause, if this parasitic inductance is too high, the device to break down.

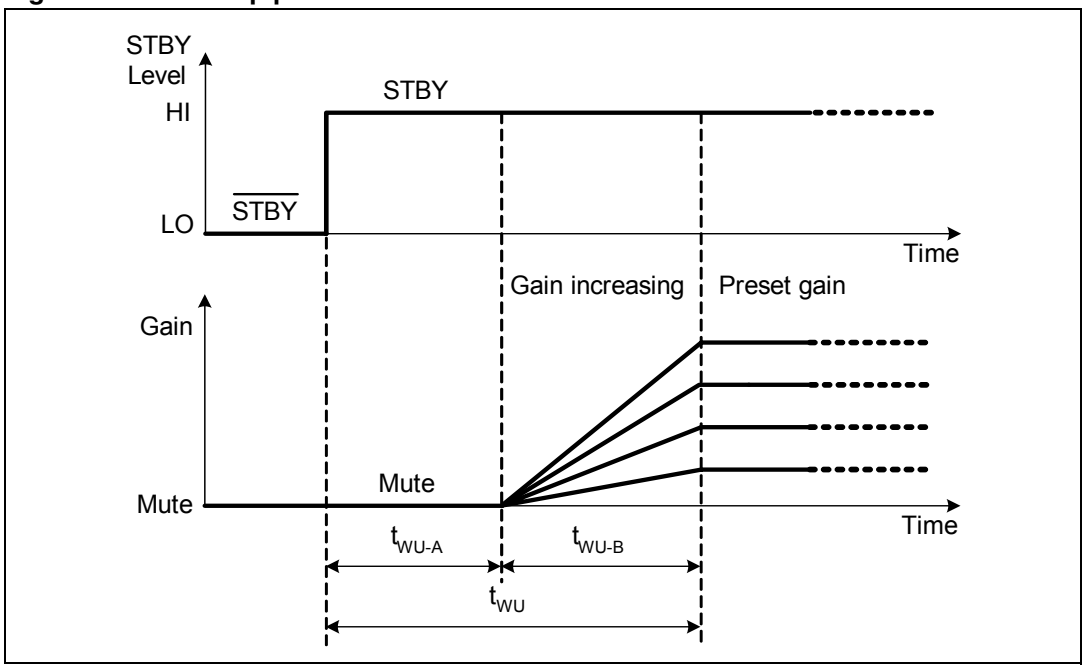
In addition, even if a ceramic capacitor has an adequate high frequency ESR (equivalent series resistance) value, its current capability is also important. A 0603 size is a good compromise, particularly when a 4 Ω load is used.

Another important parameter is the rated voltage of the capacitor. A 1 µF/6.3 V capacitor used at 5 V, loses about 50% of its value. With a power supply voltage of 5 V, the decoupling value, instead of 1 µF, could be reduced to 0.5 µF. As C_S has particular influence on the THD+N in the medium-to-high frequency region, this capacitor variation becomes decisive. In addition, less decoupling means higher overshoots which can be problematic if they reach the power supply AMR value (6 V).

4.6 Wakeup (t_{WU}) and shutdown (t_{STBY}) times

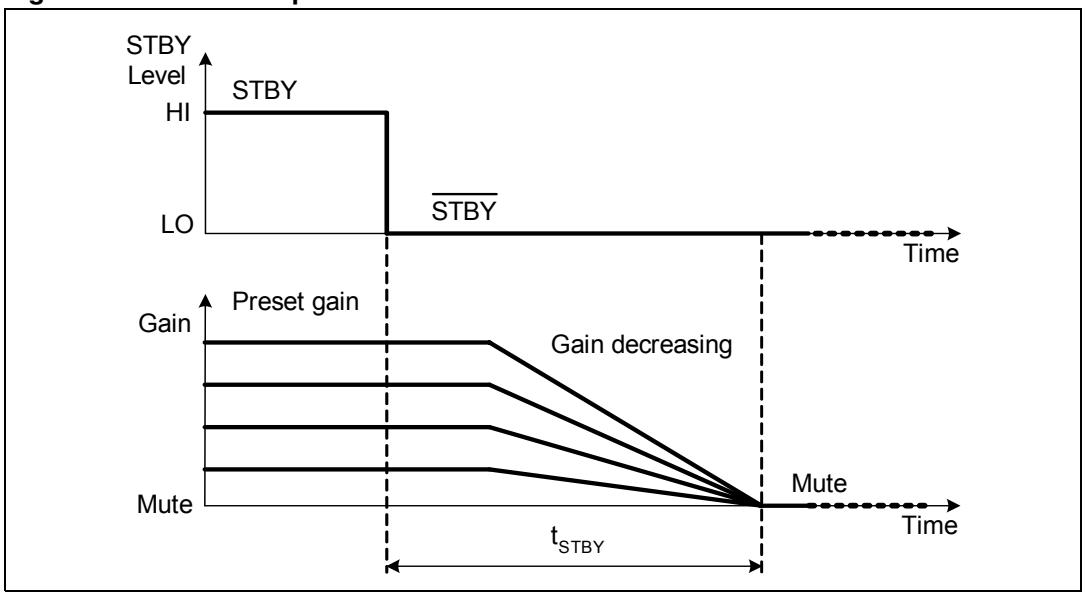
During the wake-up sequence, there is a delay when the standby is released to switch the device ON. The wake-up sequence of the TS4999 consists of two phases. During the first phase t_{WU-A}, a digitally-generated delay, mutes the outputs. Then, the gain increasing-phase t_{WU-A} begins. The gain increases smoothly from the mute state to the preset gain selected by the digital pins G0 and G1. This startup sequence avoid any pop noise during startup of the amplifier. See *Figure 57: Wake-up phase*

Figure 57. Wake-up phase



When the standby command is set, the time required to set the output stage to high impedance and to put the internal circuitry in shutdown mode is called the standby time. This time is used to decrease the gain from its nominal value set by the digital pins G0 and G1 to mute and avoid any pop noise during shutdown. The gain decreases smoothly until the outputs are muted. See *Figure 58: Shutdown phase*.

Figure 58. Shutdown phase



4.7 Consumption in shutdown mode

Between the shutdown pin and GND there is an internal 300 kΩ (+-/20%) resistor. This resistor forces the TS4999 to be in shutdown mode when the shutdown input is left floating.

However, this resistor also introduces additional shutdown power consumption if the shutdown pin voltage is not at 0 V.

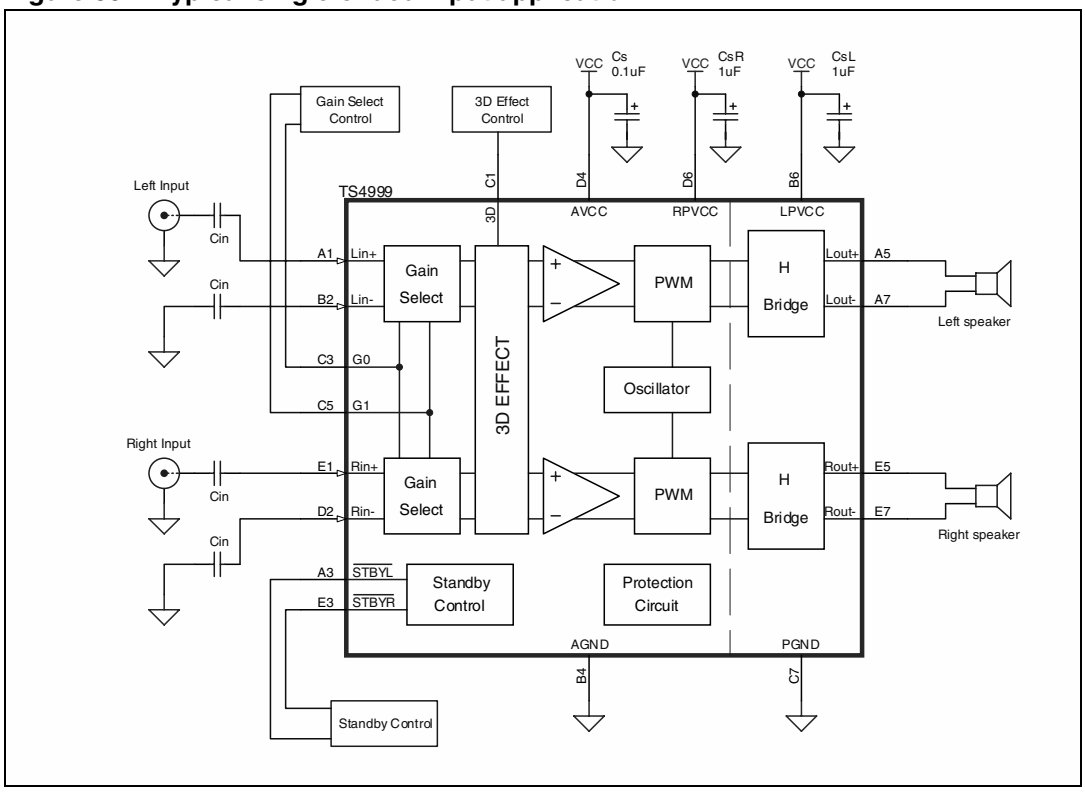
With a 0.4 V shutdown voltage pin for example, you must add 0.4 V/300 kΩ = 1.3 µA typical (0.4 V/240 kΩ = 1.66 µA in maximum) for each shutdown pin to the standby current specified in *Table 8*, *Table 9* and *Table 10*.

Of course, this current will be provided by the external control device for standby pins.

4.8 Single-ended input configuration

It is possible to use the TS4999 in a single-ended input configuration. Input coupling capacitors are also mandatory in this configuration. The schematic diagram in *Figure 59* shows a typical single-ended input application.

Figure 59. Typical single-ended input application



4.9 Output filter considerations

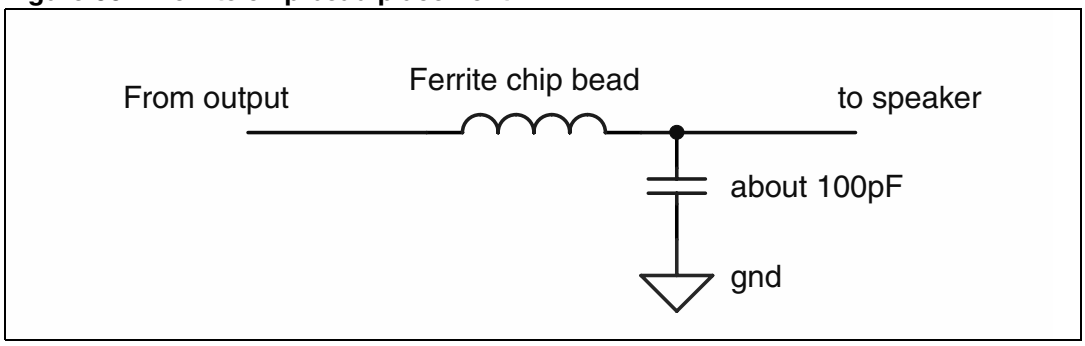
The TS4999 is designed to operate without an output filter. However, due to very sharp transients on the TS4999 output, EMI-radiated emissions may cause some standard compliance issues.

These EMI standard compliance issues can appear if the distance between the TS4999 outputs and loudspeaker terminal are long (typically more than 50 mm, or 100 mm in both directions, to the speaker terminals). Because the PCB layout and internal equipment device are different for each configuration, it is difficult to provide a one-size-fits-all solution.

However, to decrease the probability of EMI issues, there are several simple rules to follow.

- Reduce, as much as possible, the distance between the TS4999 output pins and the speaker terminals.
- Use a ground plane for "shielding" sensitive wires.
- Place, as close as possible to the TS4999 and in series with each output, a ferrite bead with a rated current of at least 2.5 A and impedance greater than 50-Ω at frequencies above 30 MHz. If, after testing, these ferrite beads are not necessary, replace them by a short-circuit.
- Allow extra footprint to place, if necessary, a capacitor to short perturbations to ground (see *Figure 60*).

Figure 60. Ferrite chip bead placement



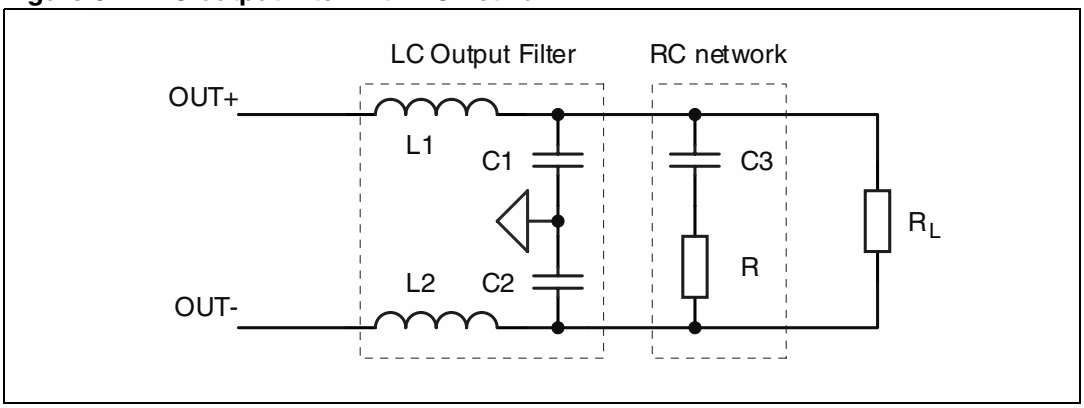
In the case where the distance between the TS4999 output and the speaker terminals is too long, it is possible to encounter low frequency EMI issues due to the fact that the typical operating PWM frequency is 280 kHz and that the fall and rise time of the output signal is less than or equal to 5 ns. In this configuration, it is necessary to use the output filter represented in *Figure 61 on page 30*, which consists of L1, C1, L2 and C2 being placed as close as possible to the TS4999 outputs.

In particular cases where the output filter is used and there is the possibility to disconnect a load, we recommended using an RC network that consists of C3 and R, as shown in *Figure 61*. In this case, when the output filter is connected without any load, the filter acts as a short-circuit for frequencies above 10 kHz in the output frequency spectrum of the amplifier. The RC network corrects the frequency response of the output filter and compensates this limitation.

Table 12. Example of component selection

Component	R_L = 4 Ω	R_L = 8 Ω
L1	15µH / 1.4A	30µH / 0.7A
L2	15µH / 1.4A	30µH / 0.7A
C1	2µF / 10V	1µF / 10V
C2	2µF / 10V	1µF / 10V
C3	1µF / 10V	1µF / 10V
R	22Ω / 0.25W	47Ω / 0.25W

Figure 61. LC output filter with RC network



4.10 Short-circuit protection

The TS4999 includes an output short-circuit protection. This protection prevents the device from being damaged when faults occur on the amplifier outputs.

When a channel is in operating mode and a short-circuit occurs between two outputs of the channel or between an output and ground, the short-circuit protection detects this situation and puts the appropriate channel into standby mode. To put the channel back into operating mode, it is necessary to put the channel's standby pin to logical LO and then back to logical HI and wake-up the channel.

4.11 Thermal shutdown

The TS4999 device has an internal thermal shutdown protection mechanism to protect the device from overheating in the event of extreme temperatures. The thermal shutdown mechanism is activated when the device reaches 150° C. When the temperature decreases to safe levels (around 135° C), the circuit switches back to normal operation.

5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 Flip chip package

Figure 62. Flip chip package

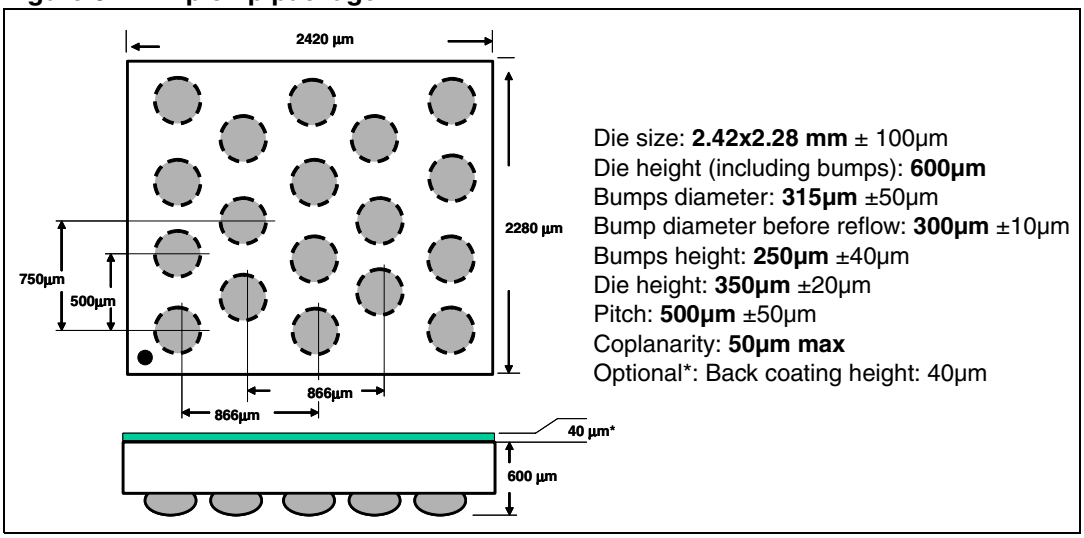


Figure 63. Pinout (top view)

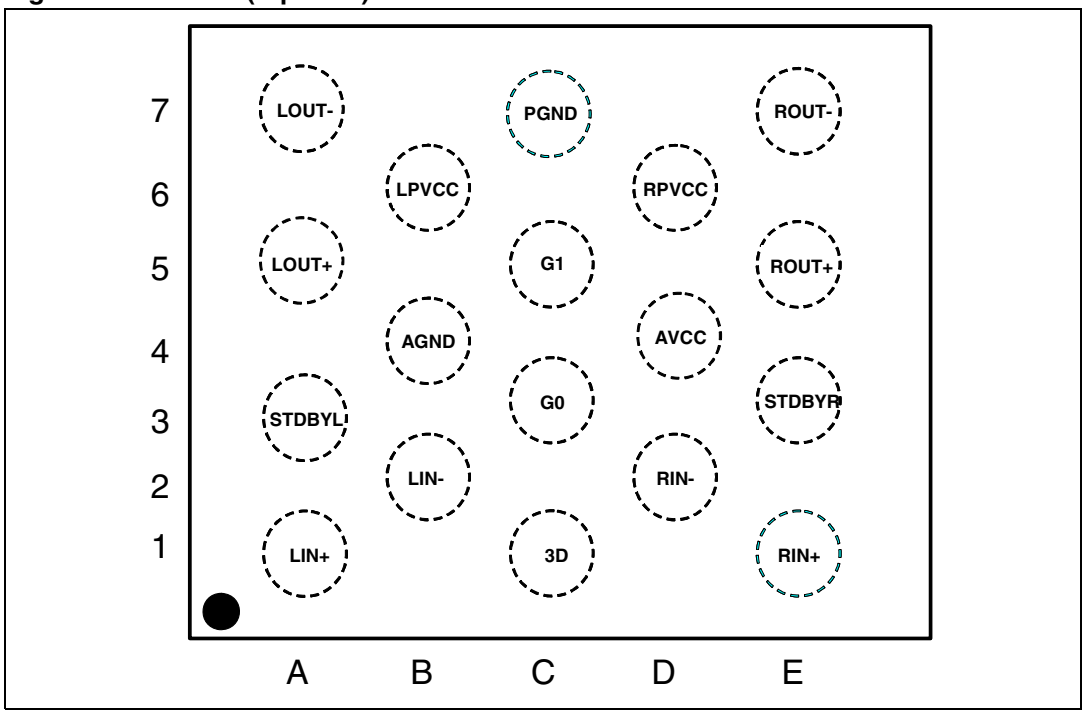
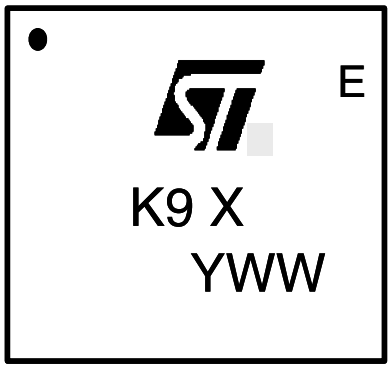


Figure 64. Marking (top view)



- ST Logo
- Symbol for lead-free: E
- Two first product code: **K9**
- third X: Assembly Line Plant code
- Three digits date code: Y for year - WW for week
- The dot is for marking pin **A1**

5.2 Tape and reel package

Figure 65. Schematic (top view)

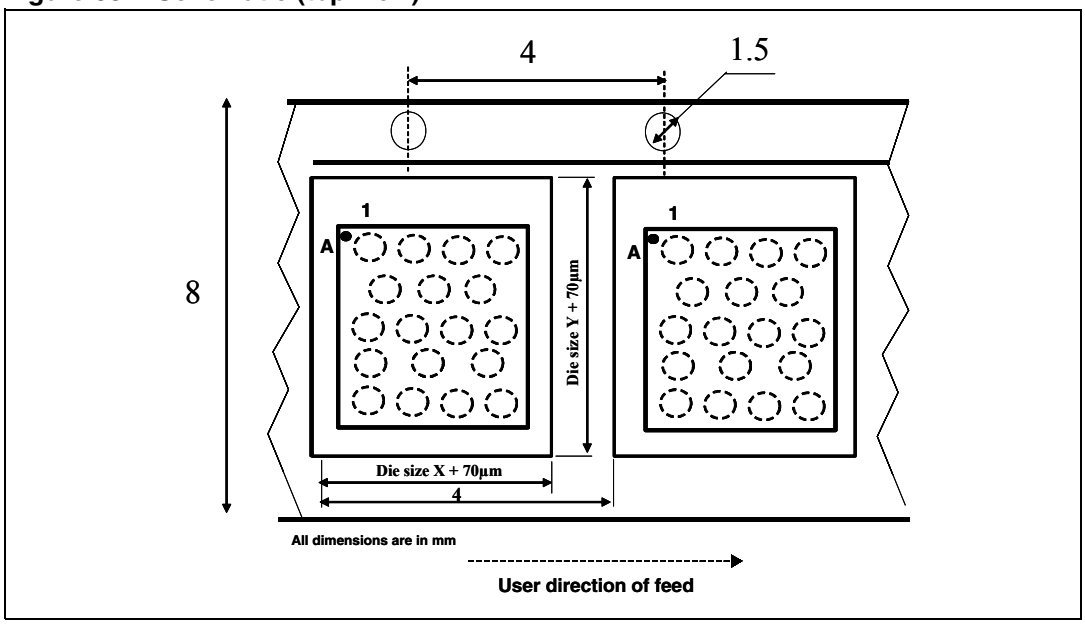
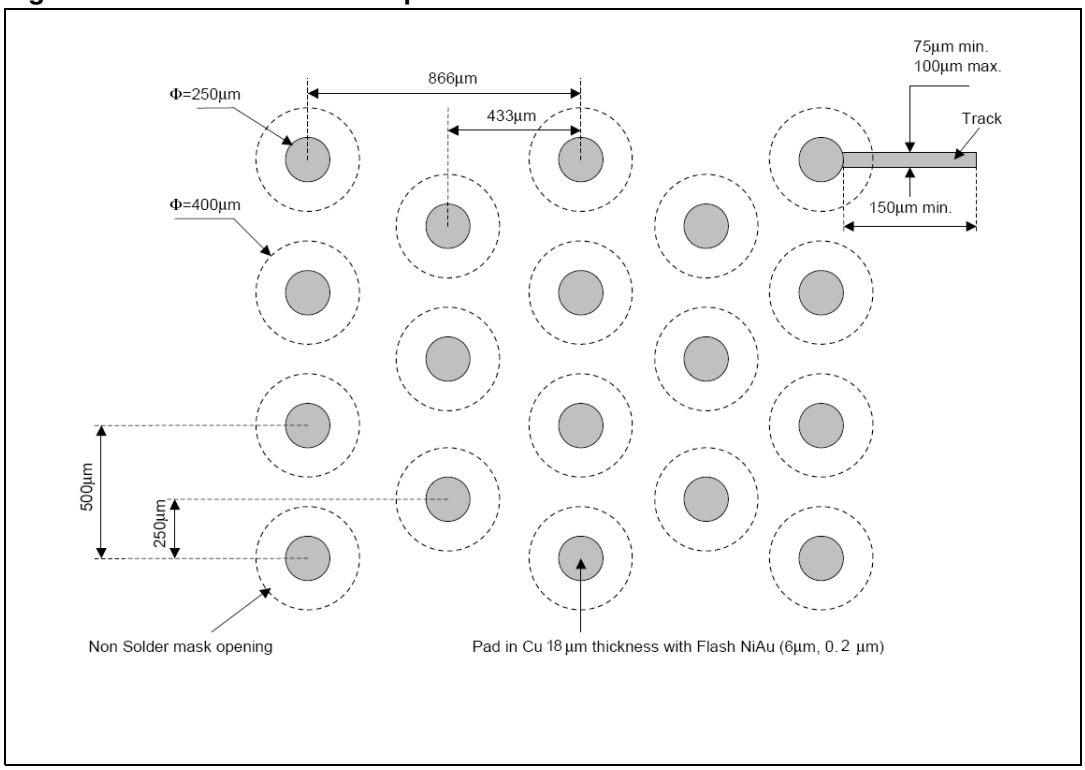


Figure 66. Recommended footprint data



6 Ordering information

Table 13. Order codes

Part number	Temperature range	Package	Packing	Marking
TS4999EIJT	-40°C to +85°C	Flip chip 18	Tape & reel	K9

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
18-Dec-2008	1	Initial release.