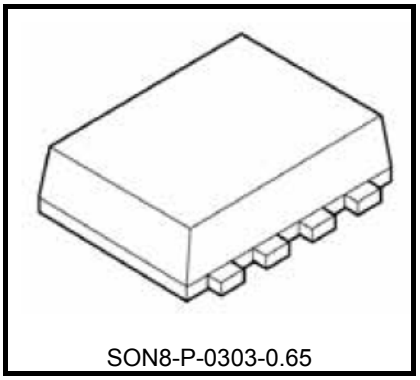
TOSHIBA Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD7102F

1 channel High-Side N channel Power MOSFET Gate Driver

TPD7102F is a 1channel high-side N channel power MOSFET gate driver. This IC contains a charge pump circuit, allowing easy configuration of a high-side switch for large-current applications.



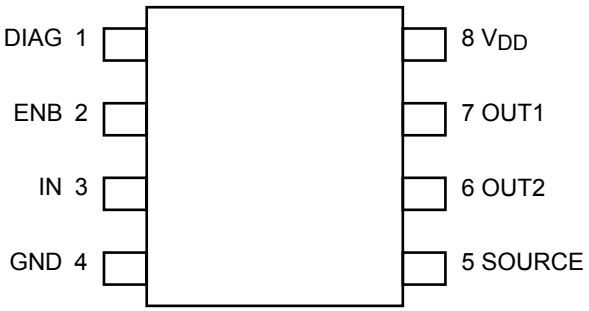
SON8-P-0303-0.65

Weight: 0.017g (typ.)

Features

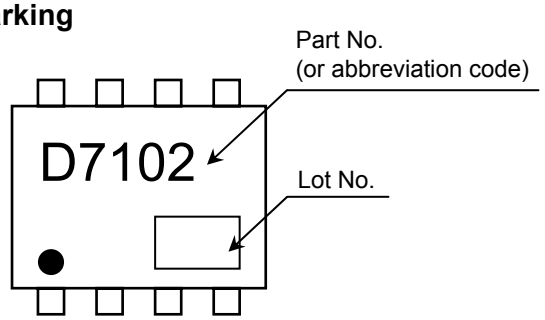
- Charge pump circuit is built in
- The diagnosis function of the voltage between OUT1 and SOURCE is built in
- Housed in the PS-8 package and supplied in embossed carrier tape.

Pin Assignment (top view)



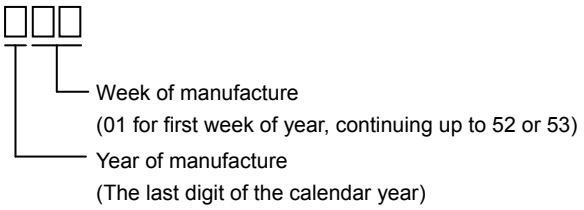
(TOP VIEW)

Marking



・Note:● on the lower left of the marking indicates Pin 1

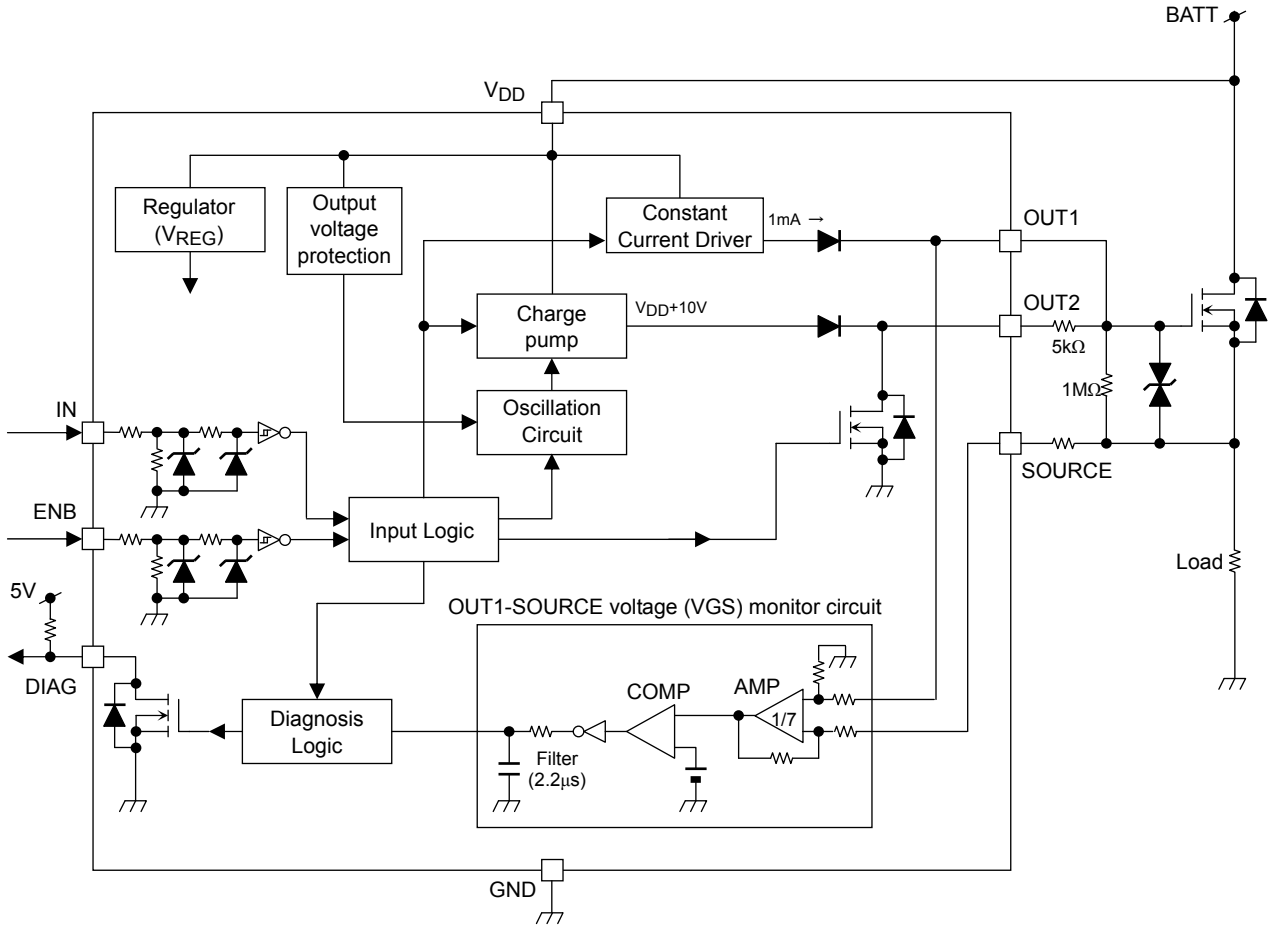
*Weekly code: (Three digits)



Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product.
The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain

Note:That because of its MOS structure, this product is sensitive to static electricity.

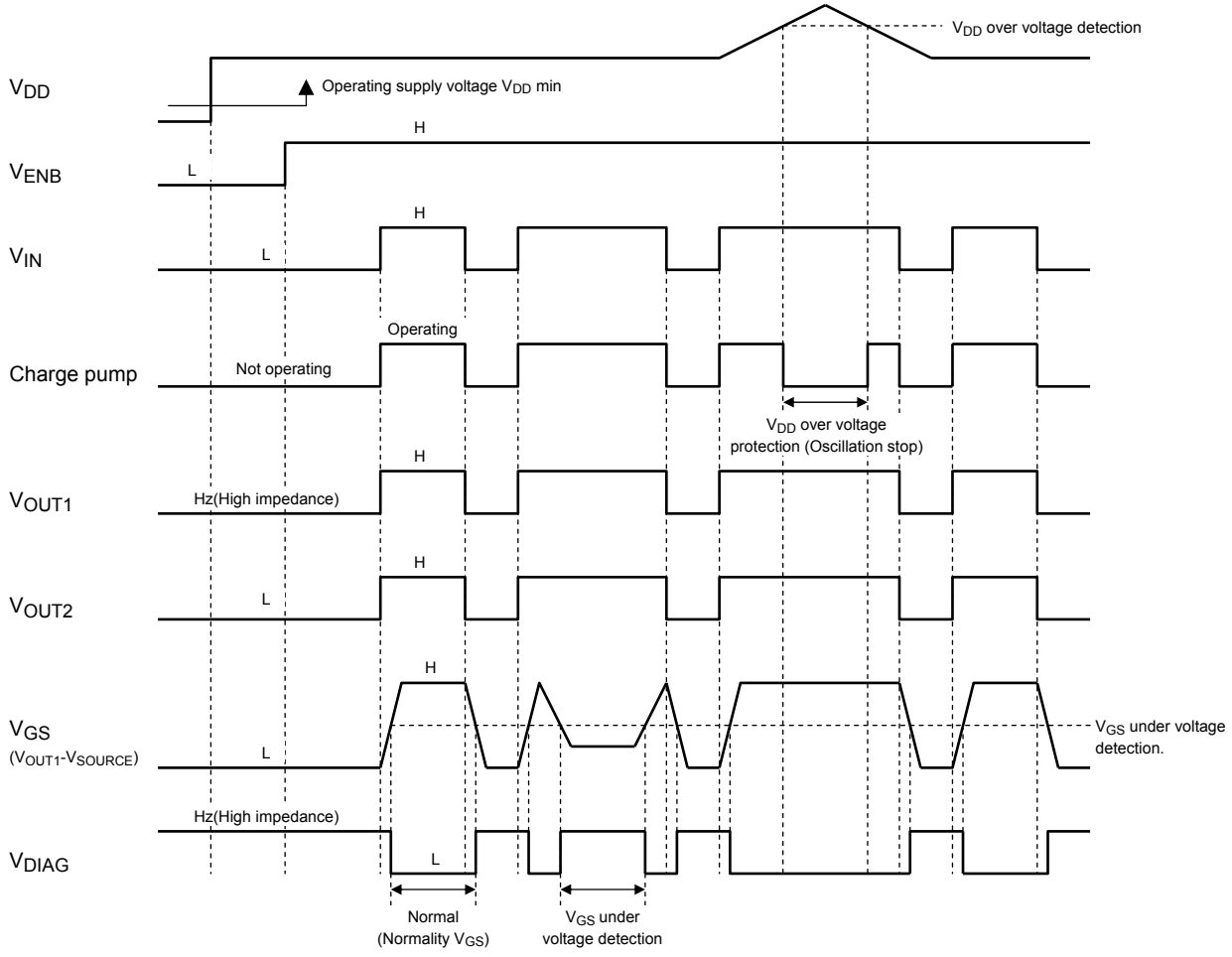
Block Diagram / Application circuit



Pin Description

Pin No.	Symbol	Function
1	DIAG	Diagnosis detection pin. N channel open drain.
2	ENB	Enable pin. The ENB pin has a pull-down resistor. When V_{ENB} is L, OUT1 is Hz and OUT2 is L.
3	IN	Input pin. The IN pin has a pull-down resistor. When V_{IN} and V_{ENB} are H, OUT1 and OUT2 are H.
4	GND	Ground pin.
5	SOURCE	Source voltage of the external power MOSFET monitor pin.
6	OUT2	Output pin 2.
7	OUT1	Output pin 1.
8	V_{DD}	Power supply pin.

Timing Chart



Note: IN and ENB apply H, after V_{DD} applied operating supply voltage.

Truth Table

IN signal	ENB signal	Charge pump circuit	V_{OUT1}	V_{OUT2}	V_{GS}	DIAG	Mode
L	L	Oscillation stop	Hz	L	V_{GS}=H	Hz	Normal (V_{DD}=7 to 18V)
H	L		Hz	L		Hz	
L	H		Hz	L		Hz	
H	H	Oscillation	H	H		L	
L	L	Oscillation stop	Hz	L	V_{GS}=L	Hz	
H	L		Hz	L		Hz	
L	H		Hz	L		Hz	
H	H	Oscillation	H	H		Hz	
L	L	Oscillation stop	Hz	L	V_{GS}=H	Hz	V_{DD} over volatage (V_{DD}>18V)
H	L		Hz	L		Hz	
L	H		Hz	L		Hz	
H	H		H	H		L	
L	L		Hz	L	V_{GS}=L	Hz	
H	L		Hz	L		Hz	
L	H		Hz	L		Hz	
H	H		H	H		Hz	

Note: V_{GS}=H(V_{GS}>V_{GSUV}) / V_{GS}=L(V_{GS}≤V_{GSUV}) *V_{GS}=V_{OUT1}-V_{SOURCE}

Note: Hz: High impedance

* DIAG is L only when V_{IN} and V_{ENB} and V_{GS} are H.

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Remarks
Power supply voltage	DC	$V_{DD(1)}$	-0.3 to 25	V	
	Pulse	$V_{DD(2)}$	35	V	t=400ms single pulse
Input voltage		V_{IN}	-0.3 to 6	V	
Diagnosis output voltage		V_{DIAG}	-0.3 to 25	V	
Diagnosis output current		I_{DIAG}	2	mA	
Output sink current(DC)		$I_{OUT2}(+)$	5	mA	Sink current
SOURCE pin negative voltage		$-V_{SOURCE}$	-7	V	t≤0.1μs, SOURCE pin 10kΩ connect
Power dissipation (Note 1-a)		$P_{D(1)}$	0.7	W	
Power dissipation (Note 1-b)		$P_{D(2)}$	0.35	W	
Operating temperature		T_{opr}	-40 to 125	°C	
Junction temperature		T_j	150	°C	
Strage temperature		T_{stg}	-55 to 150	°C	

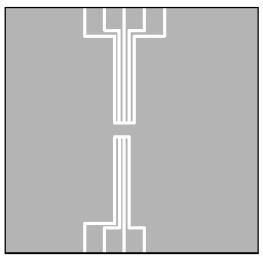
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Resistance

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to ambient	$R_{th\ (j-a)}$	178.6(Note 1-a)	°C / W
		357.2(Note 1-b)	

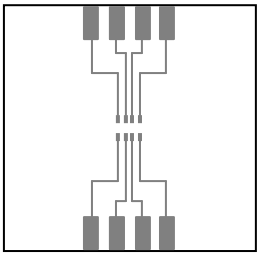
Note 1:

(a)Glass epoxy board



Glass epoxy board
Material: FR-4
25.4mm×25.4mm×0.8mm

(b)Glass epoxy board



Glass epoxy board
Material: FR-4
25.4mm×25.4mm×0.8mm

Electrical Characteristics (Unless otherwise specified, T_j = -40 to 125°C, V_{DD} = 7 to 18V)

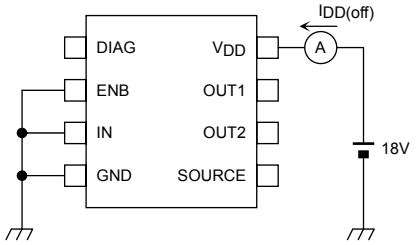
Characteristics	Symbol	Pin	Test Condition	Min	Typ.	Max	Unit
Operating supply voltage (Charge pump circuit, Input logic, Diagnosis logic operate)	$V_{DD(OPR)}$	V_{DD}	-	7	12	18	V
Supply current	$I_{DD(off)}$	V_{DD}	V_{DD} = 18V, V_{IN} =V_{ENB}= 0V	-	0.35	2	mA
	$I_{DD(on)}$	V_{DD}	V_{DD} = 18V, V_{IN} =V_{ENB}= 5V	-	3	8	mA
Input voltage	V_{INH}	IN, ENB	-	3.5	-	-	V
	V_{INL}		-	-	-	1.5	
Input current	I_{INH}, I_{ENBH}	IN, ENB	V_{IN}=V_{ENB}= 5V *Each pin current	-	50	200	μA
	I_{INIL}, I_{ENBL}		V_{IN}=V_{ENB}= 0V *Each pin current	-1	-	1	
Output voltage	V_{OUT1H}	OUT1	V_{DD} = 9 to 18V, V_{IN}=V_{ENB}=5V, V_{SOURCE}=V_{DD}, OUT1-SOURCE 1MΩ	V_{DD}-2.7	V_{DD}-1	V_{DD}	V
	V_{OUT2H}	OUT2	V_{DD} = 9 to 18V, V_{IN}=V_{ENB}=5V, V_{SOURCE}=V_{DD}, OUT2-SOURCE 1MΩ	V_{DD} + 6.0	V_{DD} +10	V_{DD} +12.5	V
OUT2 sink DMOS ON-Resistance	$R_{ONOUT2L}$	OUT2	V_{DD} = 7 to 18V, V_{IN}=V_{ENB}= 0V, I_{OUT2}=1mA	-	70	180	Ω
OUT1 high level output current	IOH1	OUT1	V_{DD}=9 to 18V, V_{IN}=V_{ENB}=5V	-	-1.0	-0.15	mA
OUT1 output leakage current	IOL1	OUT1	V_{DD}=9 to 18V, V_{IN}=V_{ENB}=0V	-1	-	-	μA
OUT1 sink current	I_{OUT1+}	OUT1	V_{OUT1}=12V,V_{IN}=V_{ENB}=0V	-	5	20	μA
OUT2 output current	IOH2	OUT2	V_{DD}=9 to 18V, V_{IN}=V_{ENB}=5V, V_{OUT2}=V_{DD}+6V	-	-100	-30	μA
Diagnosis output leakage current	I_{DIAGH}	DIAG	V_{DD} = 7 to 18V, V_{IN}=V_{ENB}=0V V_{DIAG} = 5V	-	-	10	μA
Diagnosis output voltage	V_{DIAGL}	DIAG	V_{DD} = 7 to 18V, V_{IN}=V_{ENB}=5V I_{DIAG} = 1mA	-	-	0.4	V
V_{GS} under voltage detection (OUT1-SOURCE voltage)	V_{GSUV}	OUT1, SOURCE	V_{DD} = 9 to 18V, V_{IN}=V_{ENB}=5V	3.3	4.1	4.8	V
V_{DD} over voltage detection	V_{DDOV}	V_{DD}	-	18	22	25	V
Switching time	t_{on}	IN→OUT1	Refer to Test circuit 7	-	16	100	μs
	t_{off}			-	2	10	

Note: Typical condition is V_{DD}=12V, T_j=25°C.

Note: Sink current to this IC is expressed by "+", source current from this IC is expressed by "-".

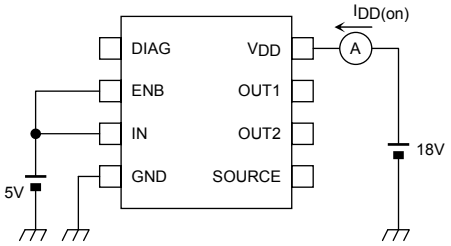
Test circuit 1

Supply current $I_{DD(off)}$



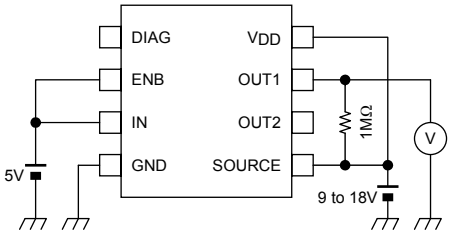
Test circuit 2

Supply current $I_{DD(on)}$



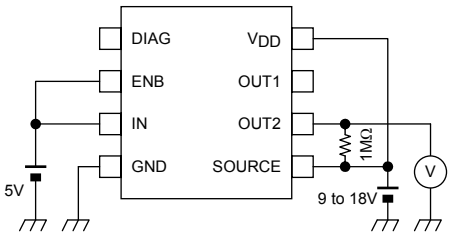
Test circuit 3

Output voltage V_{OUT1H}



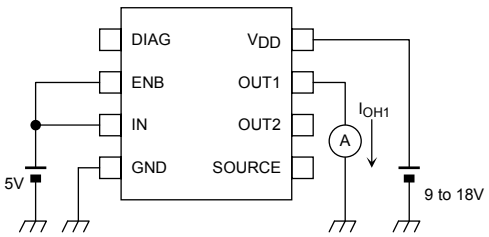
Test circuit 4

Output voltage V_{OUT2H}



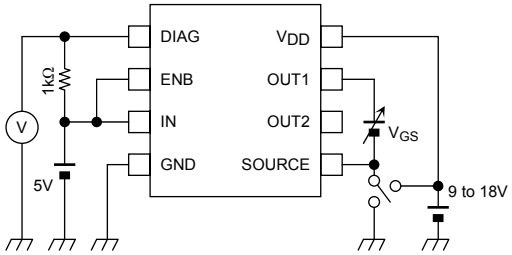
Test circuit 5

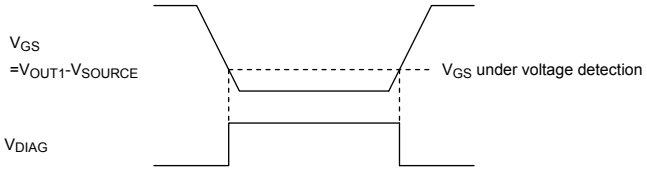
OUT1 high level output current IOH1



Test circuit 6

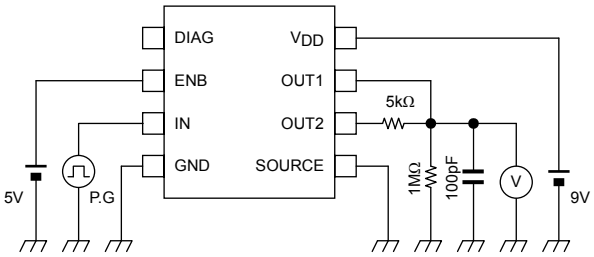
V_{GS} under voltage detection

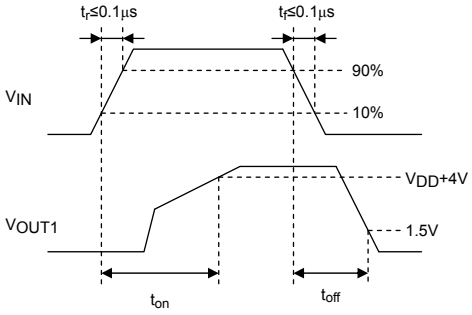




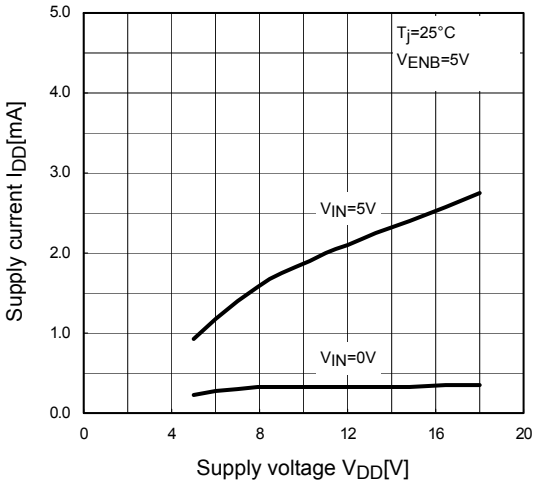
Test circuit 7

Switching time t_{on}, t_{off}

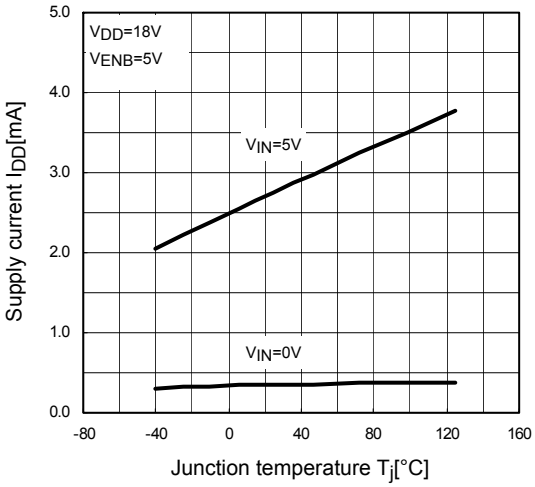




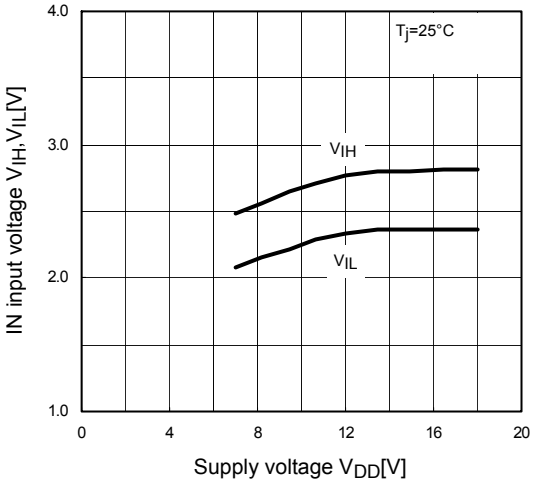
I_{DD} - V_{DD}



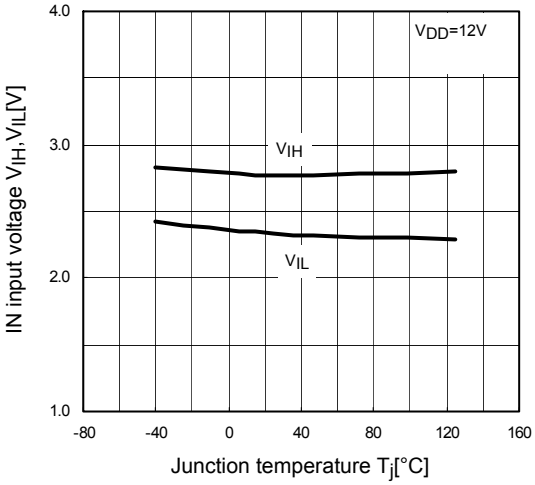
I_{DD} - T_j



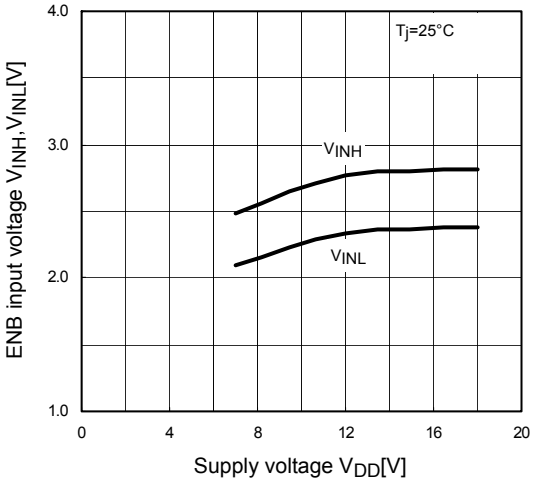
V_{IH},V_{IL} - V_{DD}



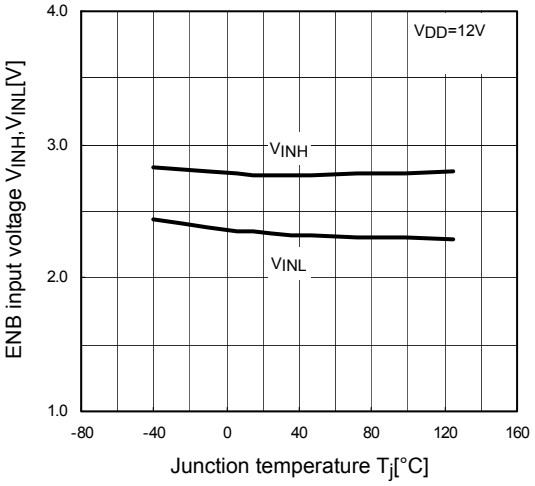
V_{IH},V_{IL} - T_j



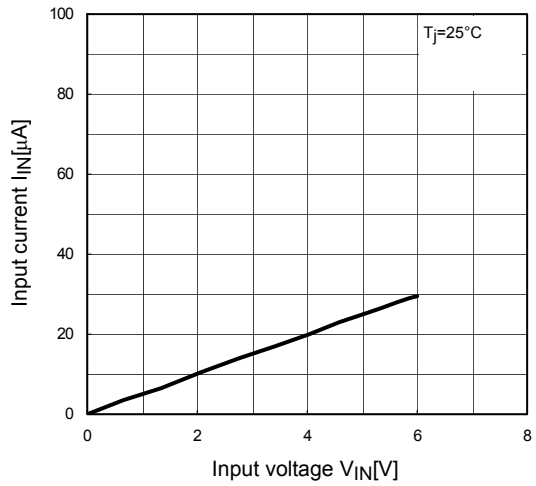
V_{INH},V_{INL} - V_{DD}



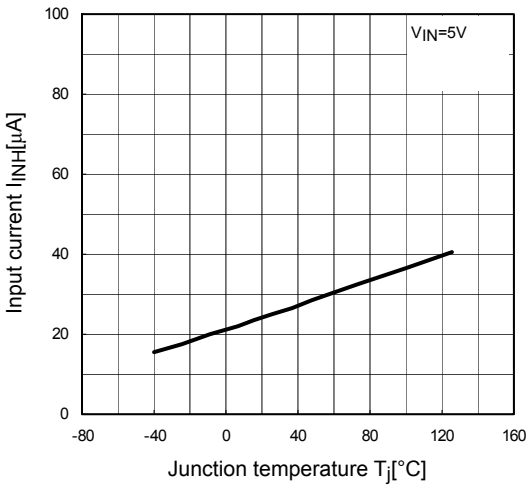
V_{INH},V_{INL} - T_j



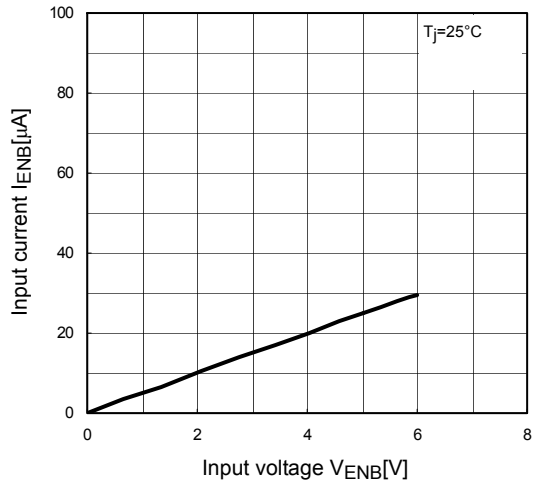
I_{IN} - V_{IN}



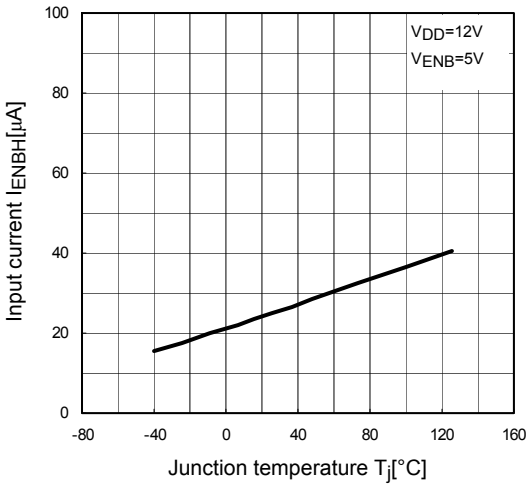
I_{INH} - T_j



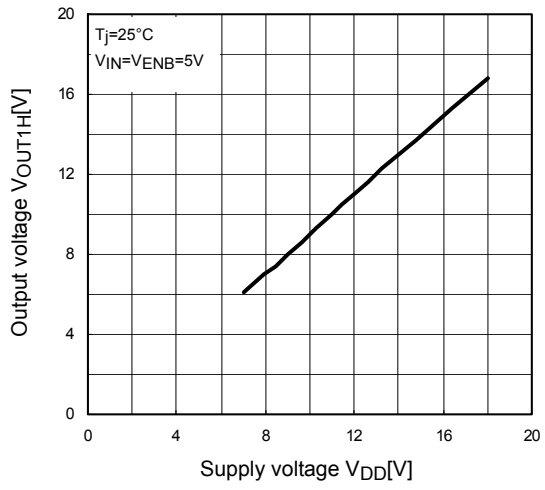
I_{ENB} - V_{ENB}



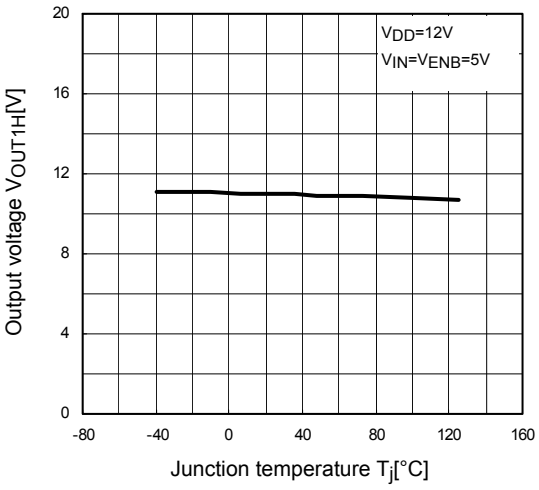
I_{ENBH} - T_j



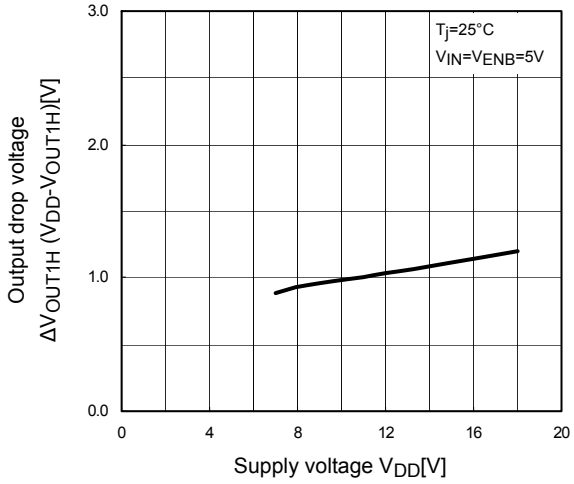
V_{OUT1H} - V_{DD}



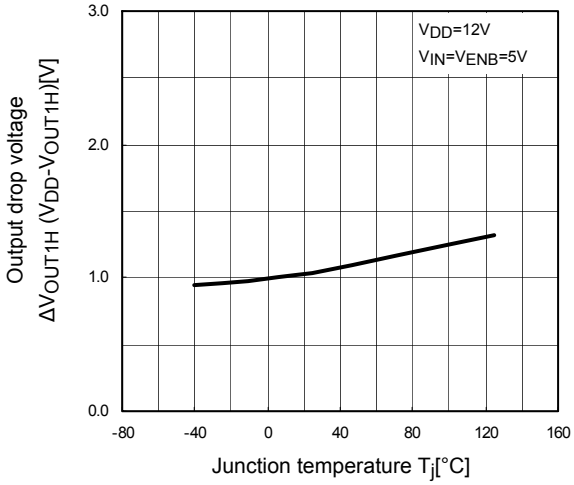
V_{OUT1H} - T_j



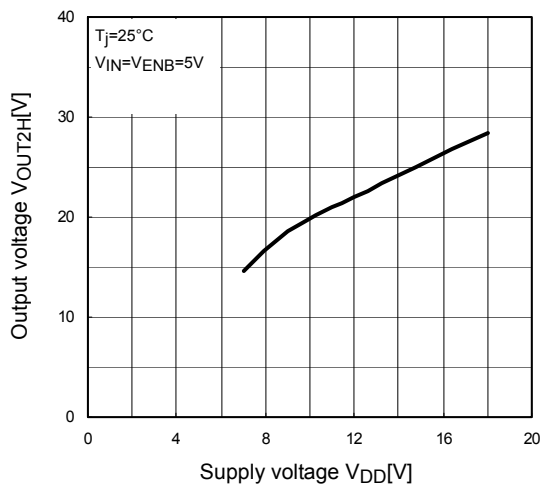
ΔV_{OUT1H} - V_{DD}



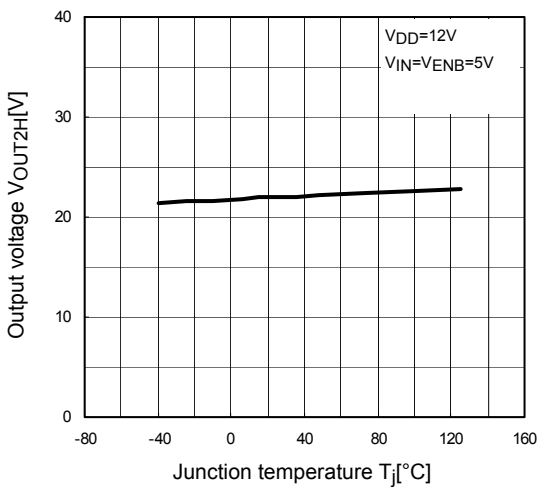
ΔV_{OUT1H} - T_j



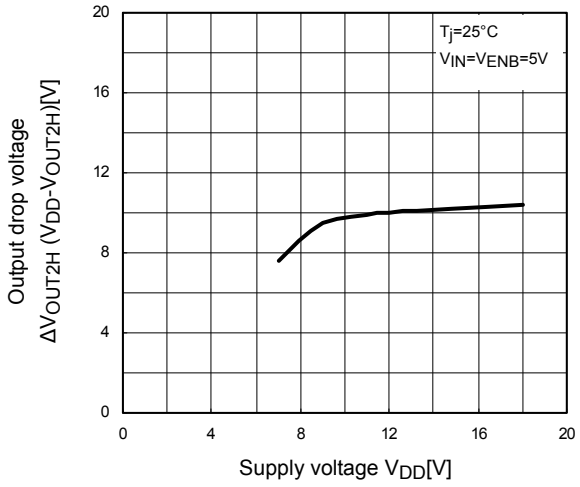
V_{OUT2H} - V_{DD}



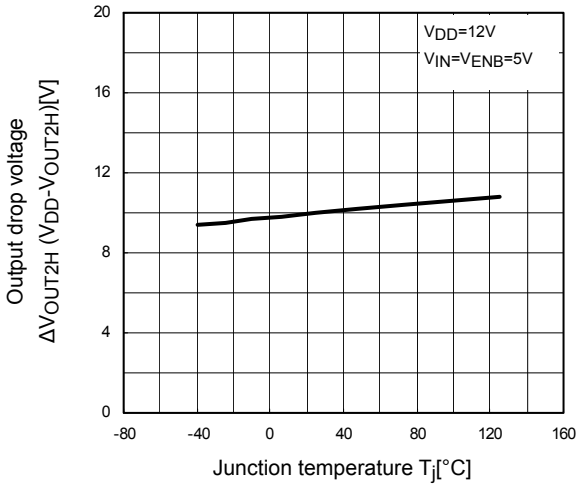
V_{OUT2H} - T_j



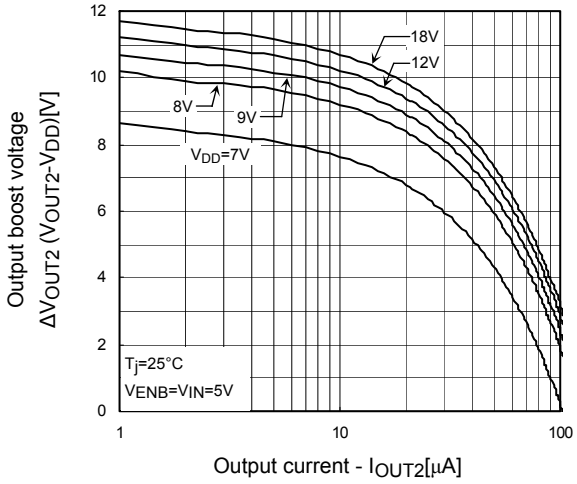
ΔV_{OUT2H} - V_{DD}



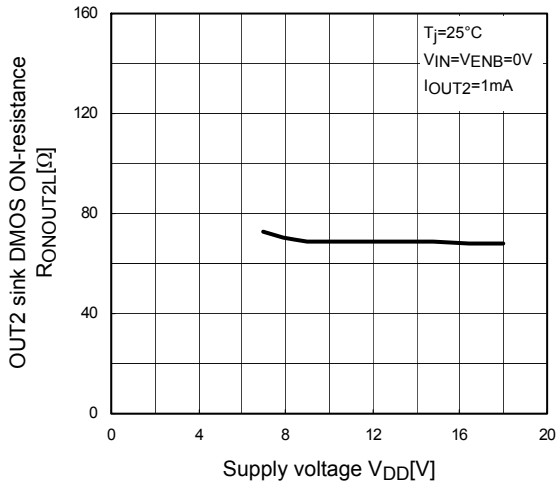
ΔV_{OUT2H} - T_j



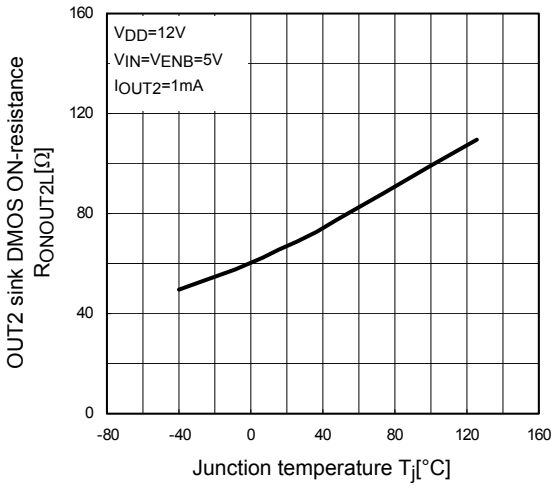
ΔV_{OUT2} – - I_{OUT2}



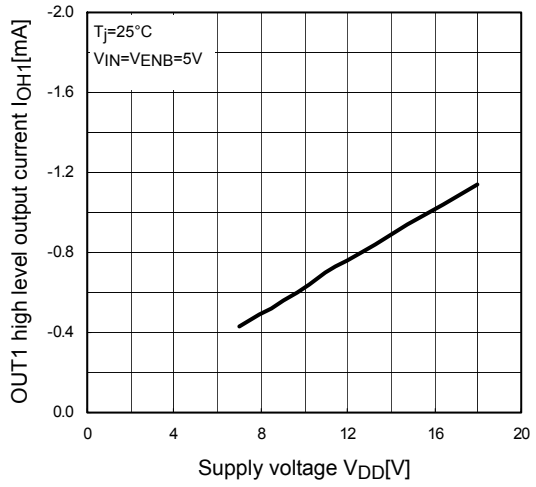
$R_{ONOUT2L}$ - V_{DD}



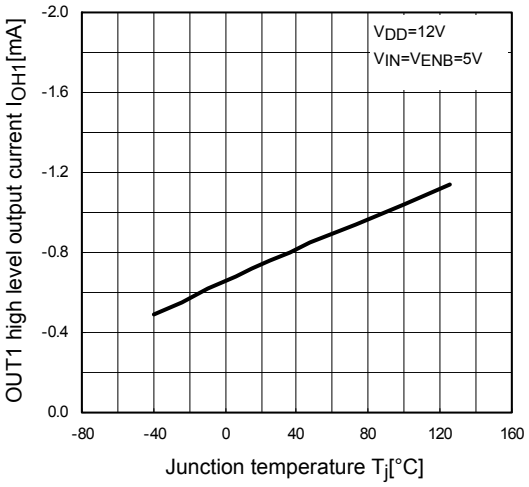
$R_{ONOUT2L}$ - T_j



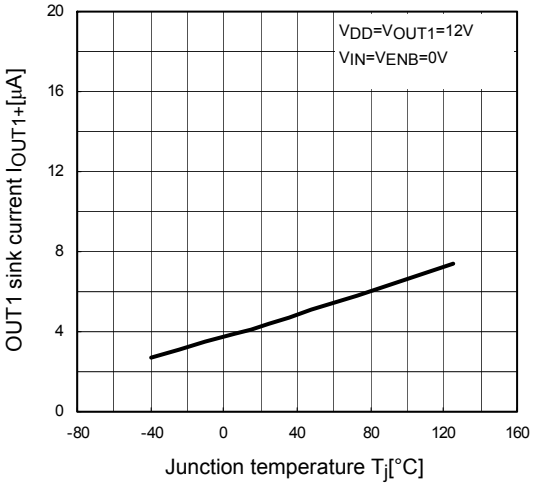
I_{OH1} - V_{DD}



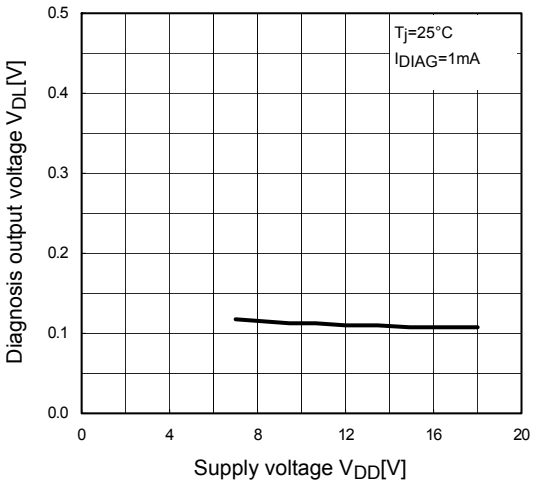
I_{OH1} - T_j



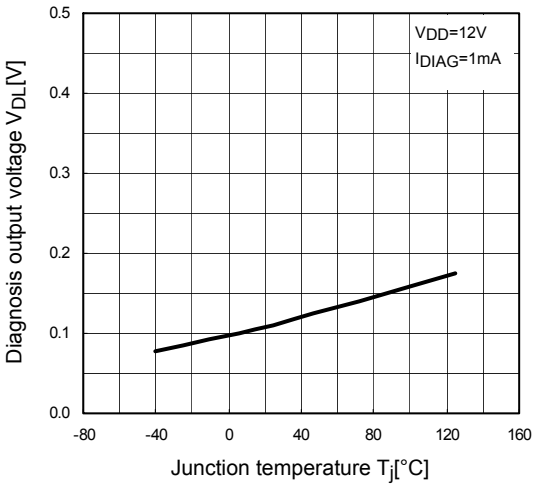
I_{OUT1+} - T_j



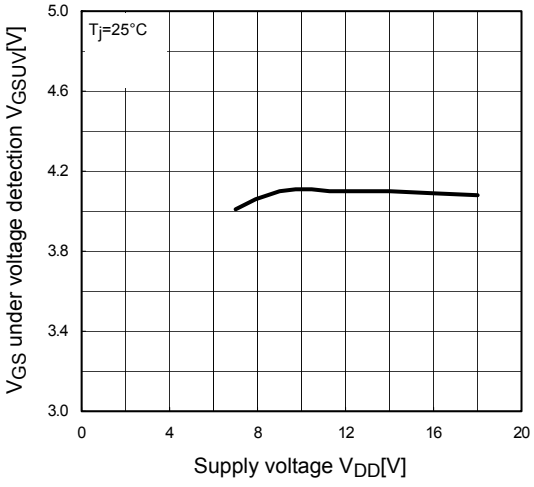
V_{DL} - V_{DD}



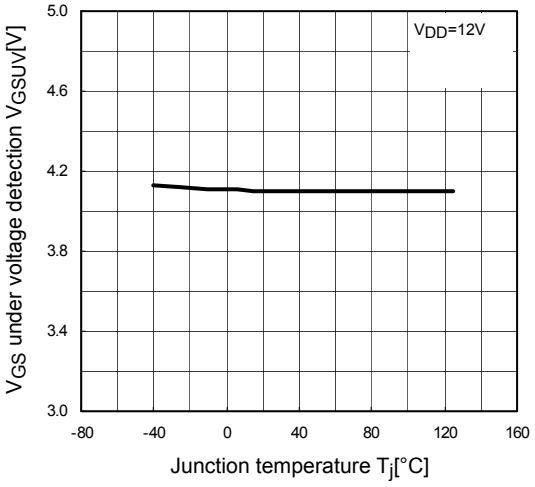
V_{DL} - T_j



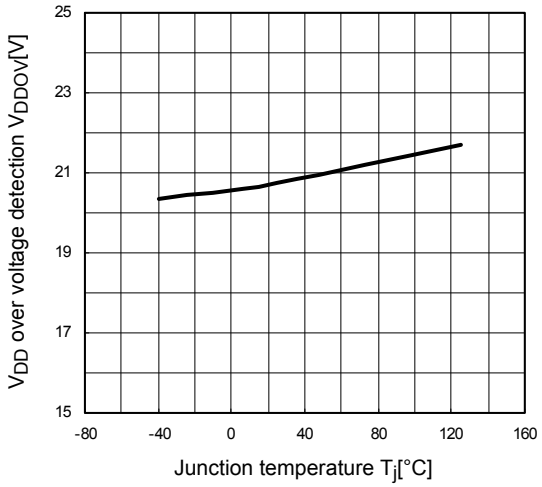
V_{GSUV} - V_{DD}



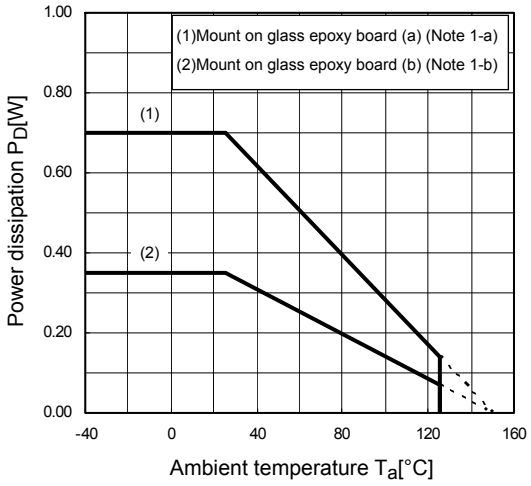
V_{GSUV} - T_j



V_{DDOV} - T_j



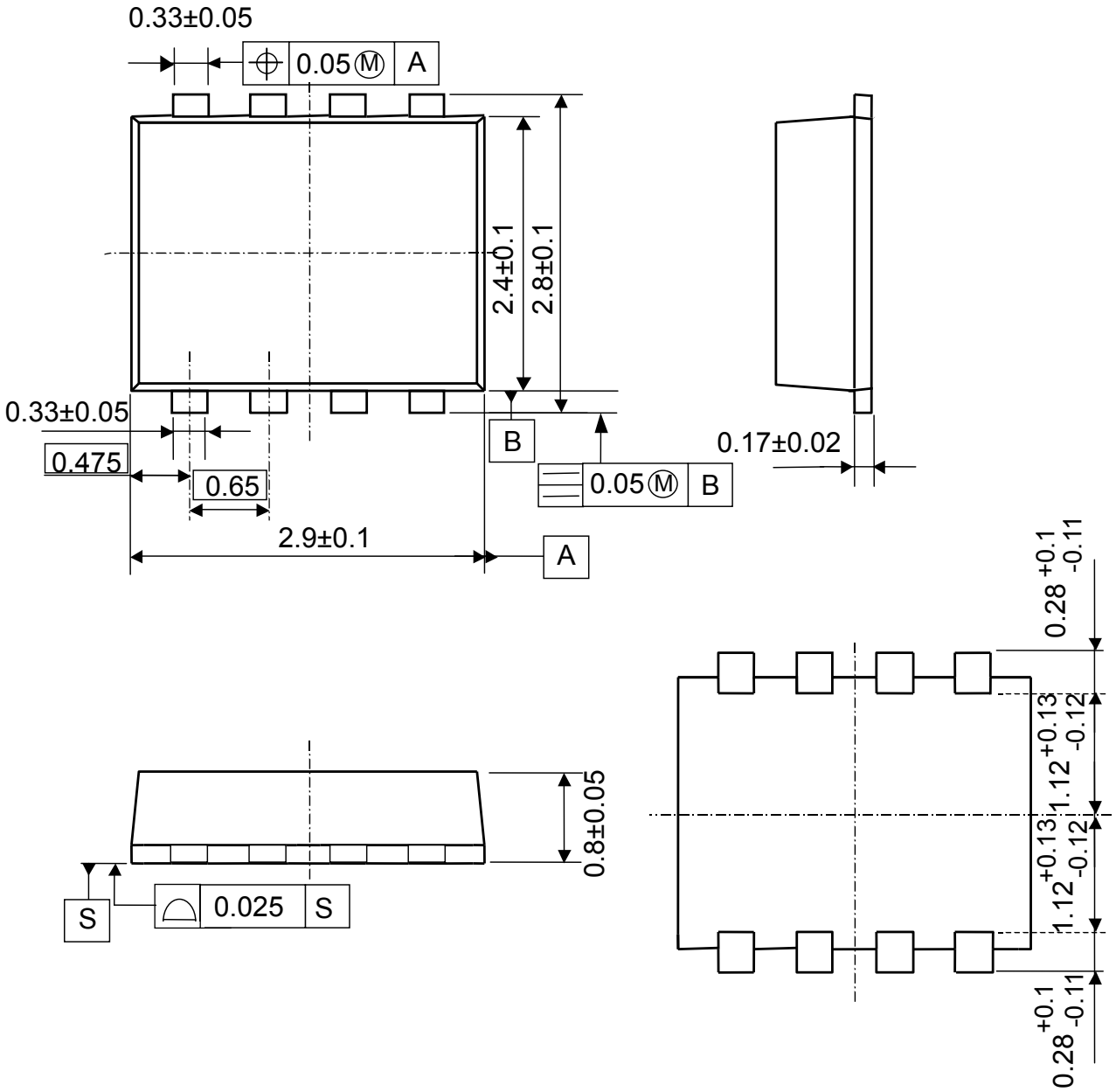
P_D - T_a



Package Dimensions

SON8-P-0303-0.65

Unit : mm



Weight : 0.017g(Typ.)

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