

**General Description**

AKD4424-SA is an evaluation board for AK4424 (192kHz sampling 24Bit Stereo DAC with 2Vrms Output). AKD4424-SA has a digital audio interface (AK4115) of Optical input and can easily achieve the interface with digital audio system. Therefore, it is easy to evaluate the sound quality of AK4424.

**Ordering Guide**

AKD4424-SA ---- AK4424 Evaluation Board

**Function**

On-board digital audio interface. (AK4115)

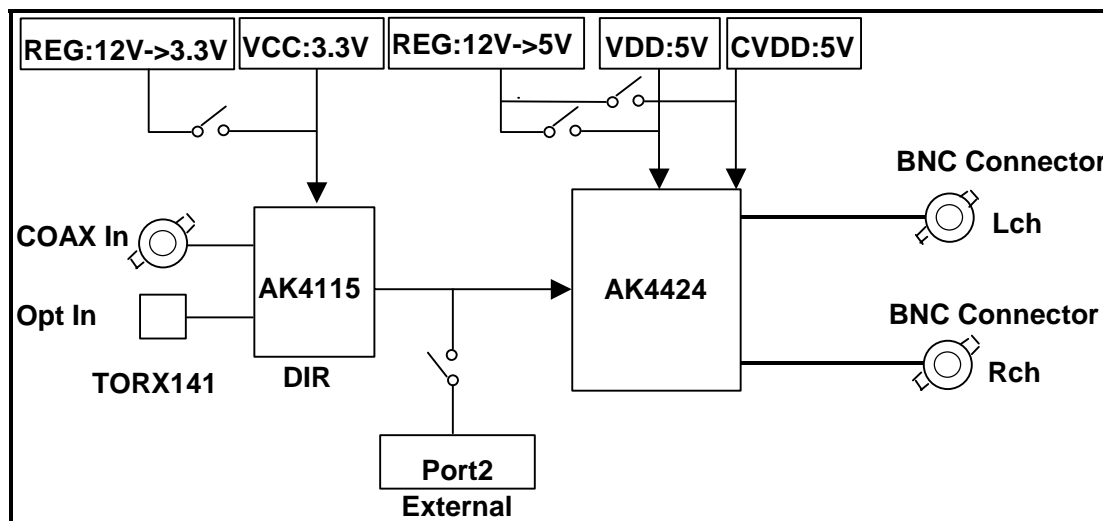


Figure 1. AKD4424-SA Block diagram  
 (\* Circuit diagram are attached at the end of this manual.)

## Board Outline Chart

### ■ Outline Chart

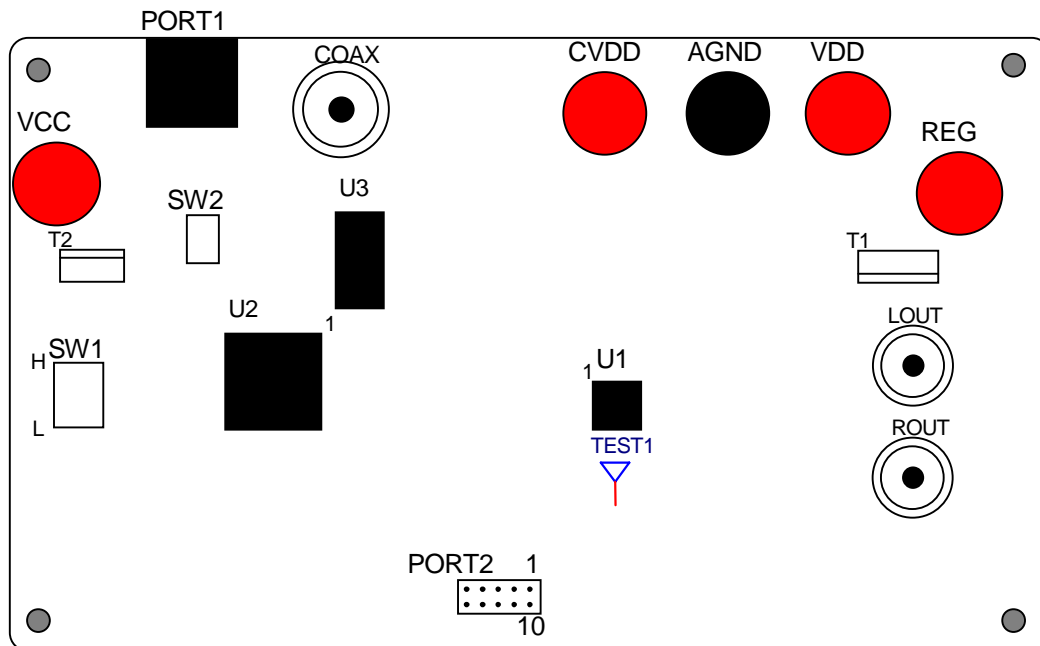


Figure 2. AKD4424-SA Outline Chart

### ■ Comment

- (1) LOUT, ROUT (BNC-JACK)  
It is analog signal output Jack. The signal is output from LOUT/ROUT pins.
- (2) COAX, PORT1, PORT2 (Digital signal connector)  
COAX (BNC-JACK): Digital signal (SPDIF, Fs: 24 ~ 48kHz) is input to the AK4115. (Default)  
PORT1 (Optical Connector): Optical digital signal (SPDIF, Fs: 32 ~ 48kHz) is input to the AK4115.  
PORT2 (10 pin header): The clock and data can be input and output with this connector.
- (3) REG, VDD, AGND, CVDD, VCC  
These are the power supply connectors. Connect power supply with these pins.  
As for the detail comments, refer to the setup of power supply in P3.
- (4) SW1, SW2 (Switch)  
SW1: Setting of frequency of MCKO that is output from AK4115.  
SW2: Reset of AK4115. Keep "H" during normal operation.

## ■ Operation sequence

### 1) Set up the power supply lines.

Each supply line should be distributed from the power supply unit.

Name of jack	Color of jack	Typ Voltage	Voltage Range	Using	Default Setting
VDD1	Red	+5V	+4.5~+5.5V	VDD of AK4424	Connected to +5V
CVDD1	Red	+5V	+4.5~+5.5V	CVDD of AK4424	Connected to +5V
VCC1	Red	+3.3V	+3.0~+3.6V	AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit	Connected to +3.3V
		+12V (Note 1)	+5.8V~+20V	Regulator: T2: +12V→+3.3V (AVDD, DVDD, TVDD, OVDD of AK4115 and VCC of Logic circuit)	
AGND2	Black	0V	0V	Ground	Connected to GND (Should be connected)
REG	Red	+12V (Note 2)	+7V~+25V	Regulator: T1: +12V→+5V (VDD, CVDD of AK4424)	Open (Not connected)

Table 1. Set up of power supply lines

Note 1) Use regulator: T2 can supply AK4115 with clear voltage :

R36: Short (0 )→ Open; R34,R35:Open→ Short (0 ); Connect to VCC with 12V power supply.

Note 2) Use regulator: T1 can supply AK4424 with clear voltage :

R25,R44: Short (0 )→ Open; R37,R43:Open→ Short (0 ); VDD, CVDD should be open. Connect to REG with 12V power supply.

### 2) DIP Switch setting:

Refer to Table 2 and Table 3

### 3) Power Down:

The AK4115 should be reset once by bringing SW2 (AK4115 PDN) “L” upon power-up.

## ■ Evaluation mode

### 1. Using DIR (Optical Link)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through optical connector (PORT1: TORX141). It is possible to evaluate the AK4424 by using CD disk.

Setting: R19: Open →470Ω; R33: short (0Ω)→Open

### 2. Using DIR (COAX) (Default)

The DIR generates MCLK, BICK, LRCK and SDATA from the received data through BNC connector (J3). It is possible to evaluate the AK4424 by using CD disk.

Setting: R19: Open; R33: short (0Ω); (Default)

\* COAX is recommended for an evaluation of the Sound quality.

### 3. Supply all interface signals that include master clock via PORT2 from external equipments..

Setting: R11: 5.1Ω→Open

R12, R13, R14: 51Ω→Open

R15, R16, R17, R18: Open→51Ω or short (0Ω)

Note) The above work of removing (open) or shorting resistors need to modify the connection by soldering.

### ■ Setting of DIP switch

[SW1]: AK4115 setting

No.	Pin	OFF	ON	Default の状態
1	OCKS1	AK4115's Master Clock setting Look Table 3		ON
2	OCKS0			OFF

Table 2. SW1 setting

OCKS1	OCKS0	MCLK Frequency
0	0/1	256fs @ fs=96kHz
1	0	512fs @ fs=48kHz
1	1	128fs @ fs=192kHz

Default

Table 3. MCLK clock setting

### ■ Setting of SW2 switch

[SW2](PDN): Reset of AK4115. Keep "H" during normal operation.

<b>Measurement Results</b>
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## [Measurement condition]

- Measurement unit : Audio Precision System two Cascade (AP2)
- MCLK : 512fs (fs=44.1KHz) / 256fs (fs=96KHz) / 128fs (fs=192KHz)
- BICK : 64fs
- fs : 44.1kHz / 96KHz / 192KHz
- Bit : 24bit
- Power Supply : VDD=CVDD=5V
- Interface : DIR
- Temperature : Room

**Table Data**

fs=44.1KHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	20kLPF	91.4	92.1
DR	1kHz, -60dB	20kLPF, A-weighted	104.9	104.8
S/N	"0" data	20kLPF, A-weighted	105.3	105.3

fs=96KHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	90.8	91.3
DR	1kHz, -60dB	40kLPF, A-weighted	104.9	104.9
S/N	"0" data	40kLPF, A-weighted	105.3	105.3

fs=192KHz

Parameter	Input signal	Filter condition	Lch	Rch
S/(N+D)	1kHz, 0dB	40kLPF	91.2	91.8
DR	1kHz, -60dB	40kLPF, A-weighted	104.6	104.6
S/N	"0" data	40kLPF, A-weighted	104.7	104.7

Plot Data

fs=44.1KHz

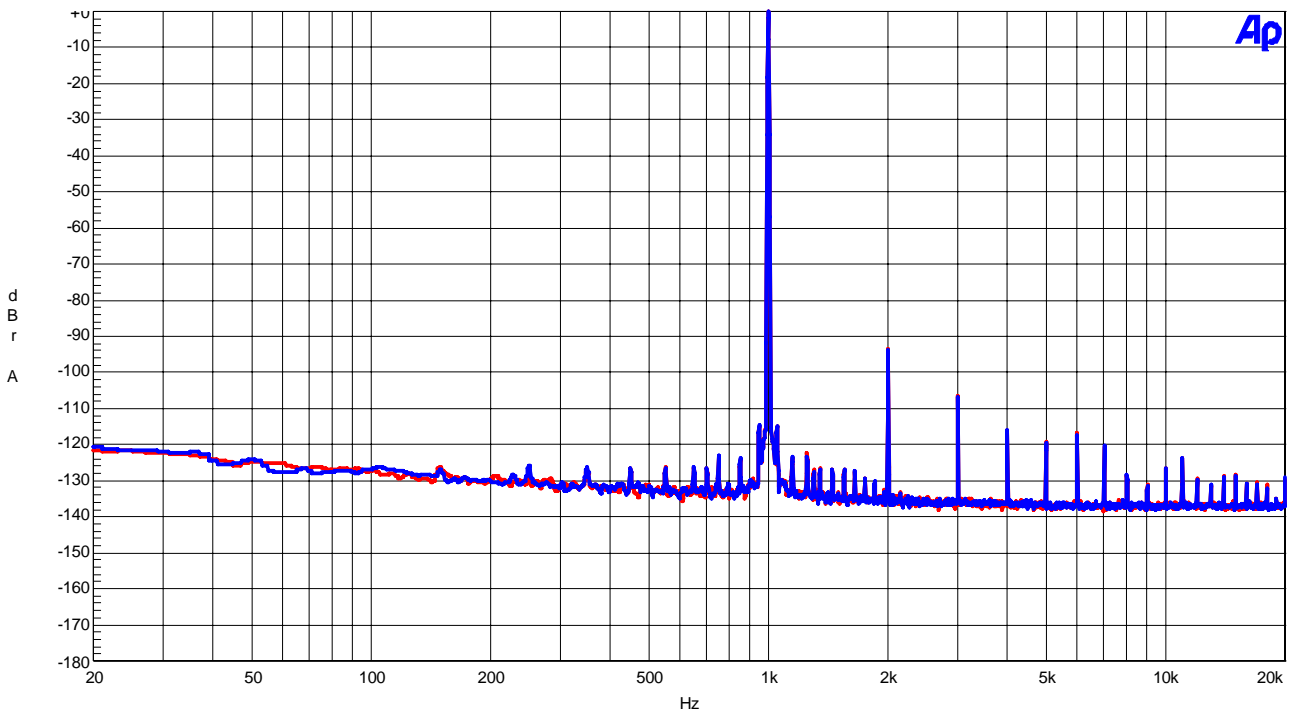


Figure 3. FFT (0dB)

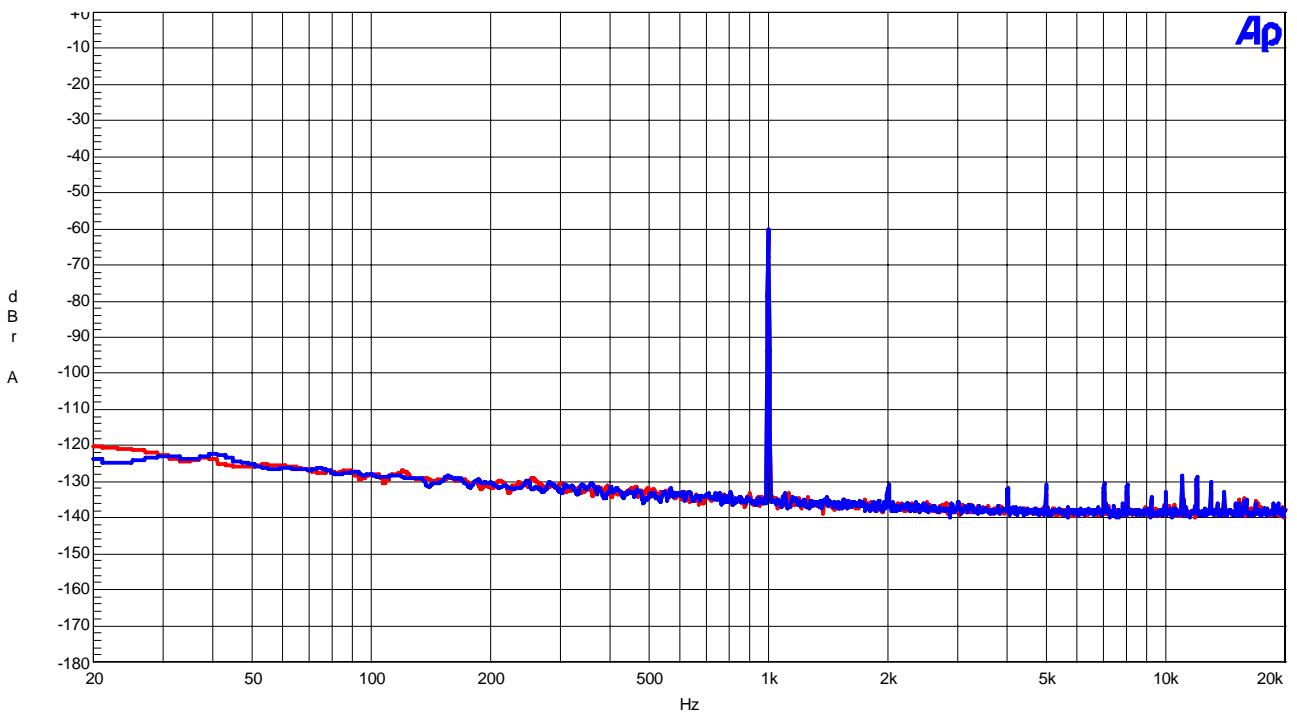


Figure 4. FFT (-60dB)

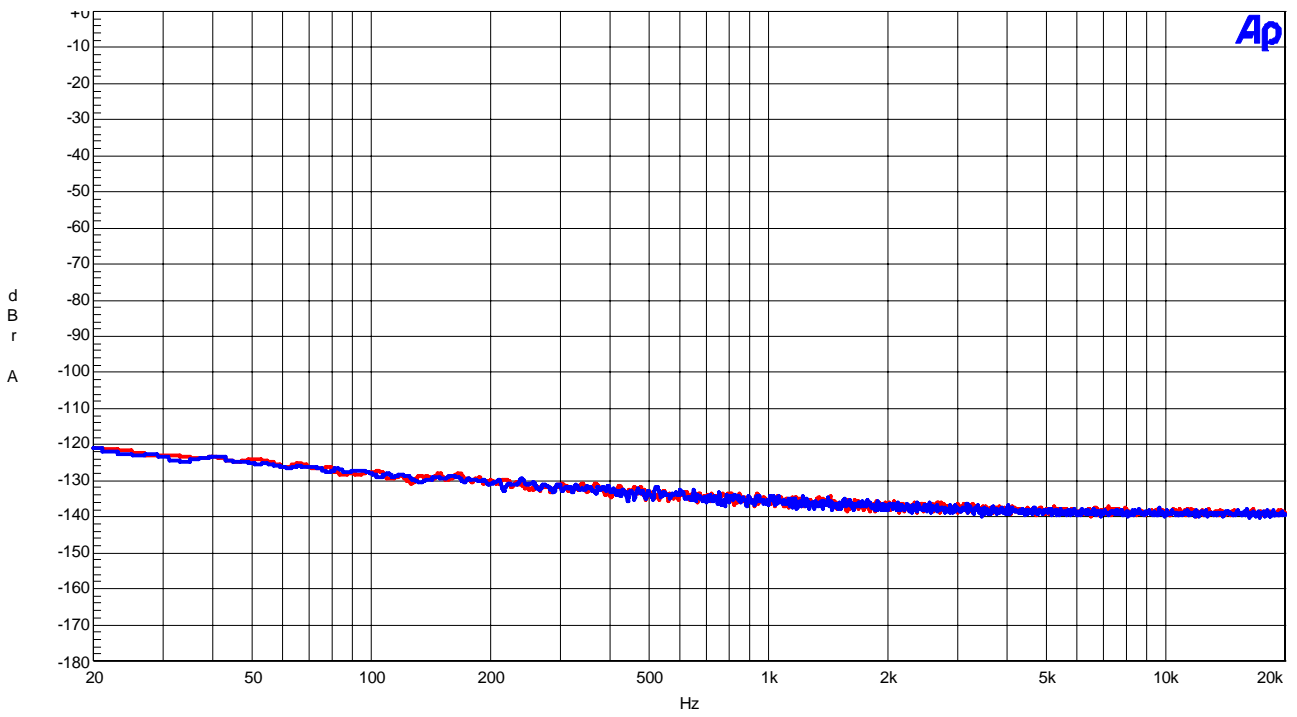


Figure 5. FFT (No Signal)

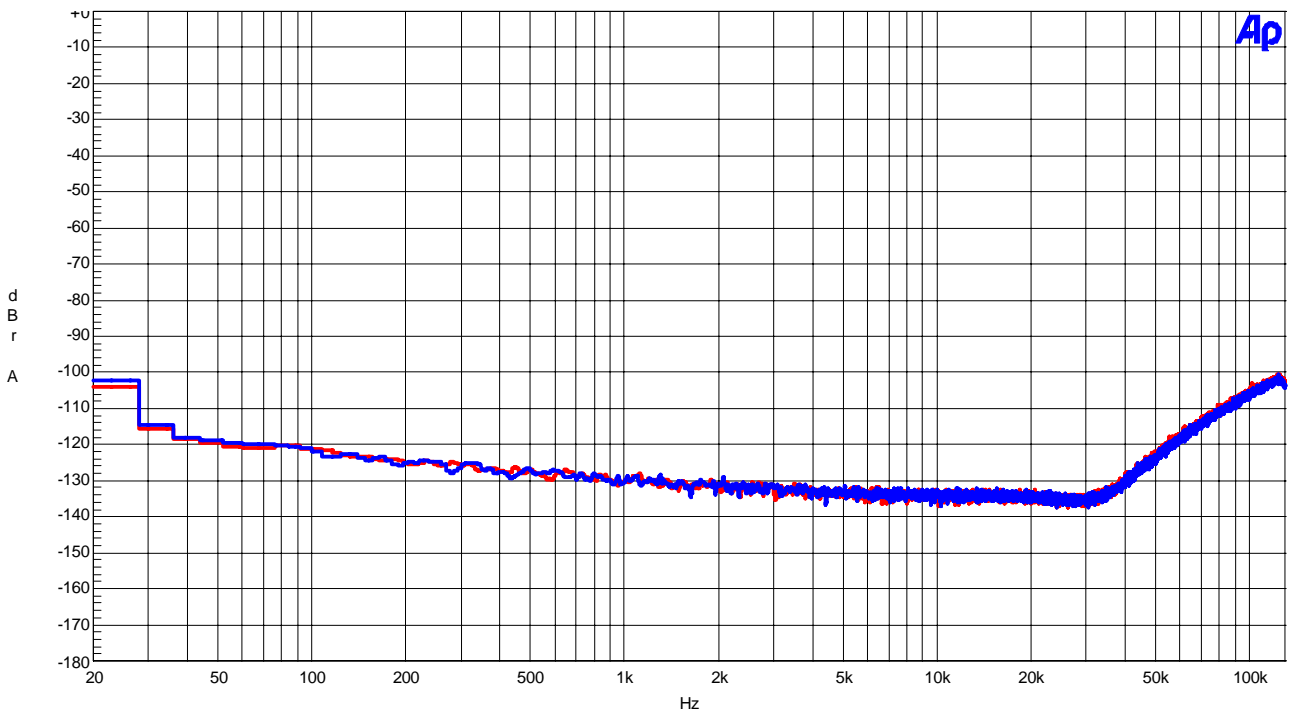


Figure 6. FFT (Out of Band Noise)

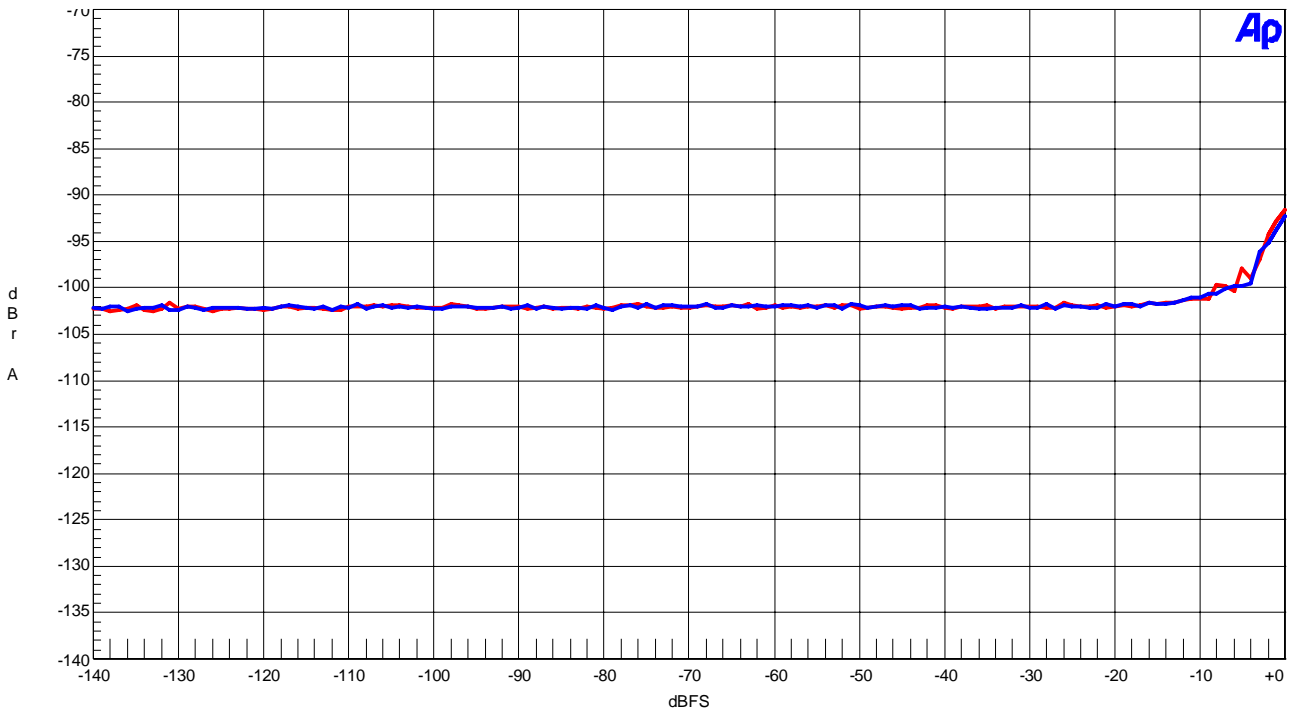


Figure 7. THD + N vs Input Level

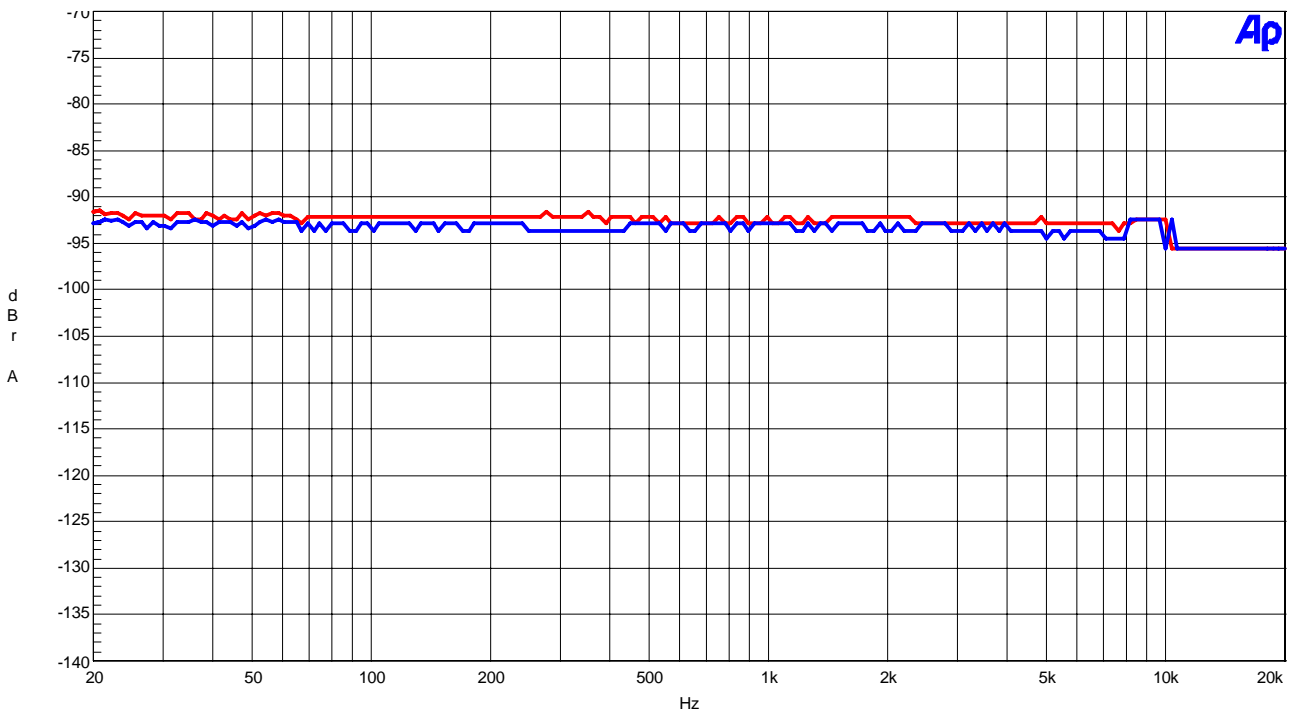


Figure 8. THD + N vs Input Frequency



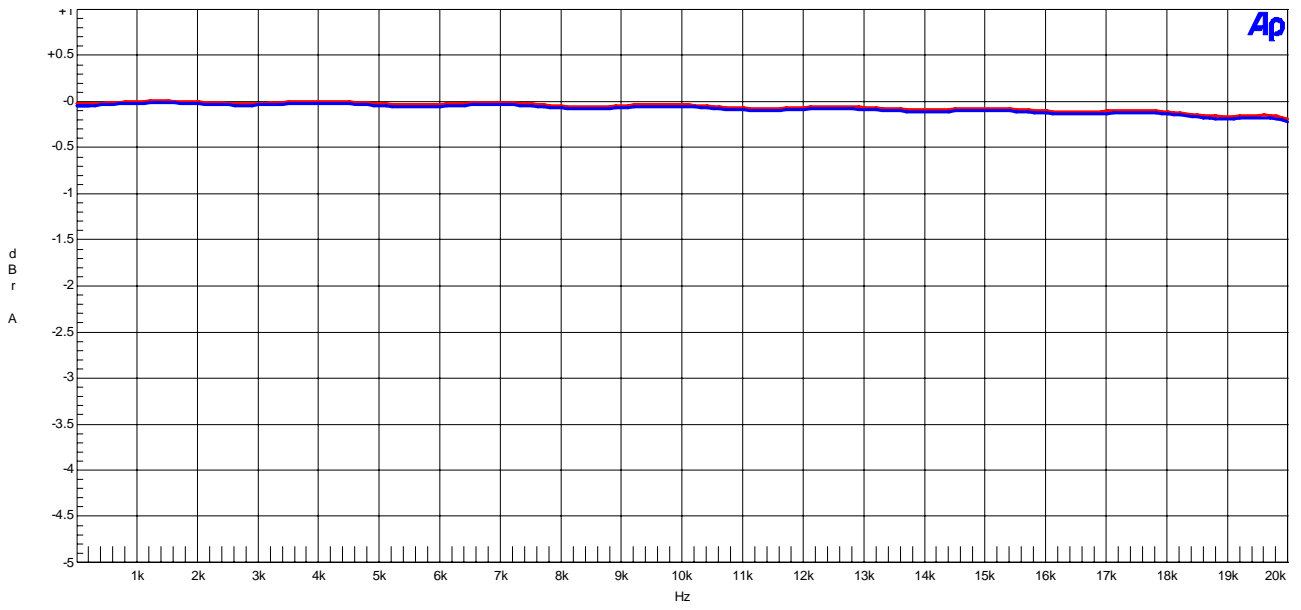


Figure 9. Frequency Response

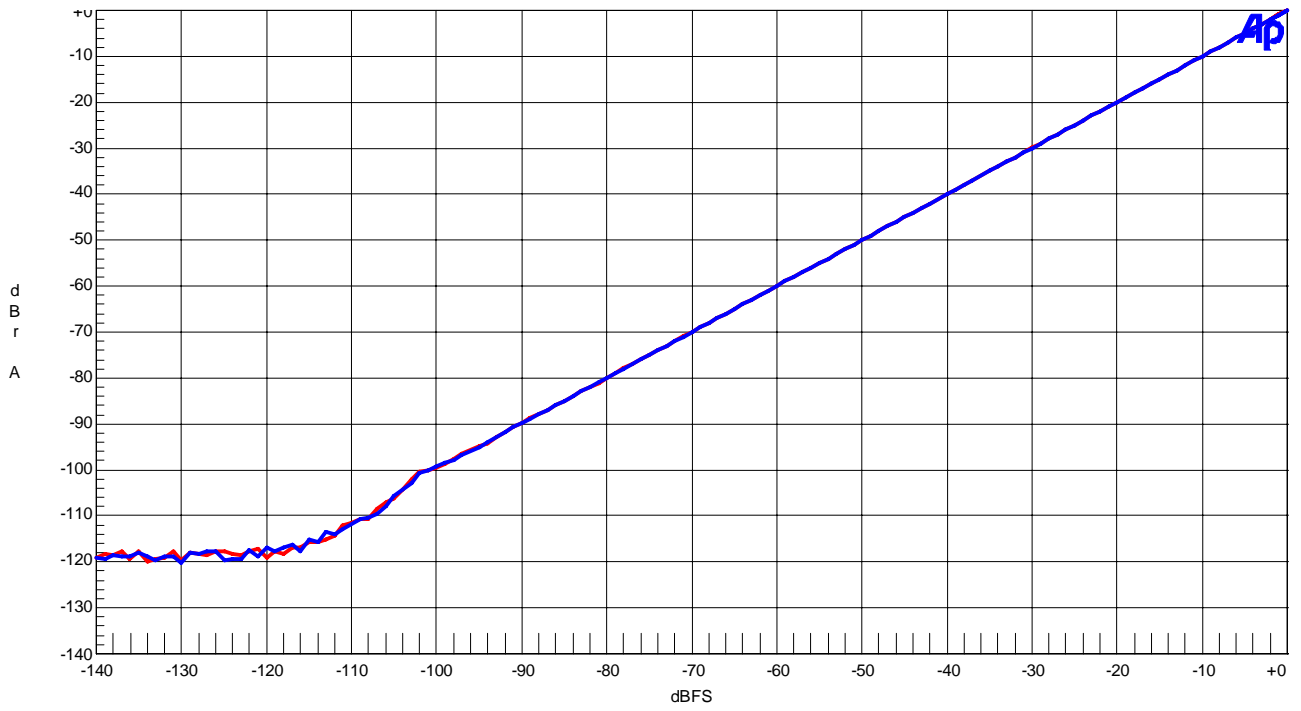


Figure 10. Linearity

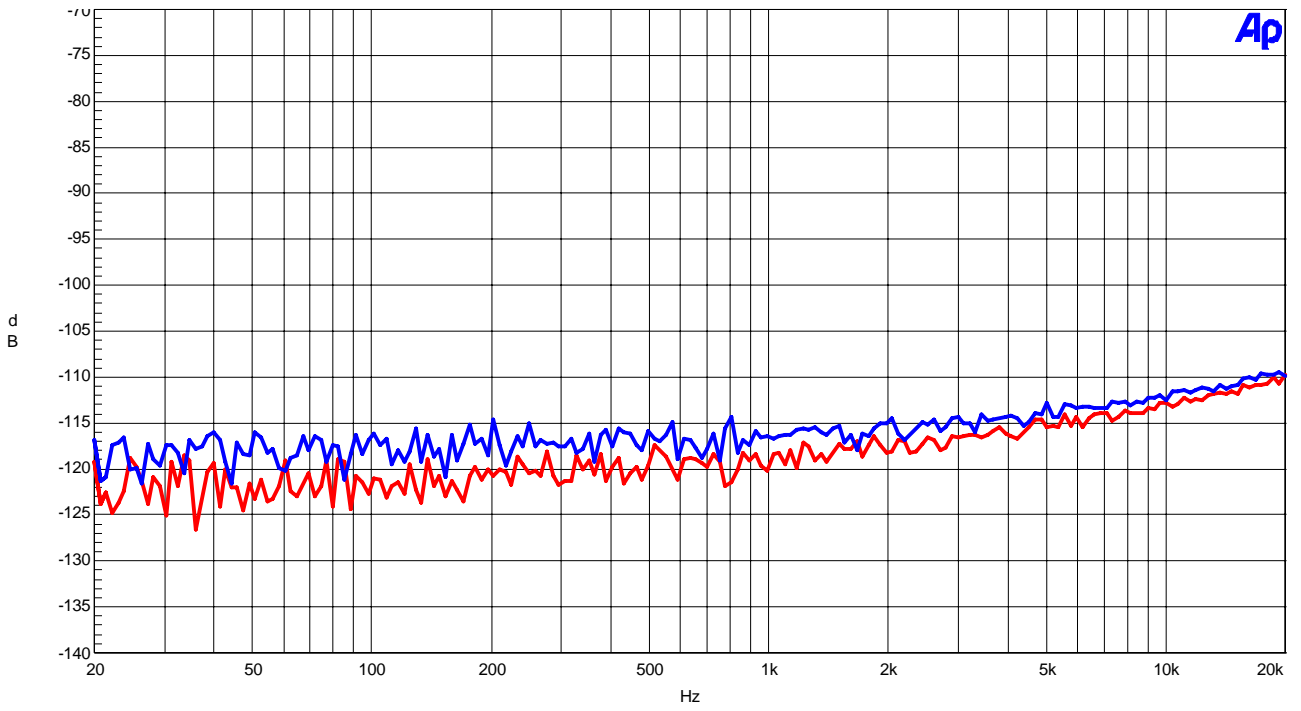


Figure 11. Crosstalk

fs=96KHz

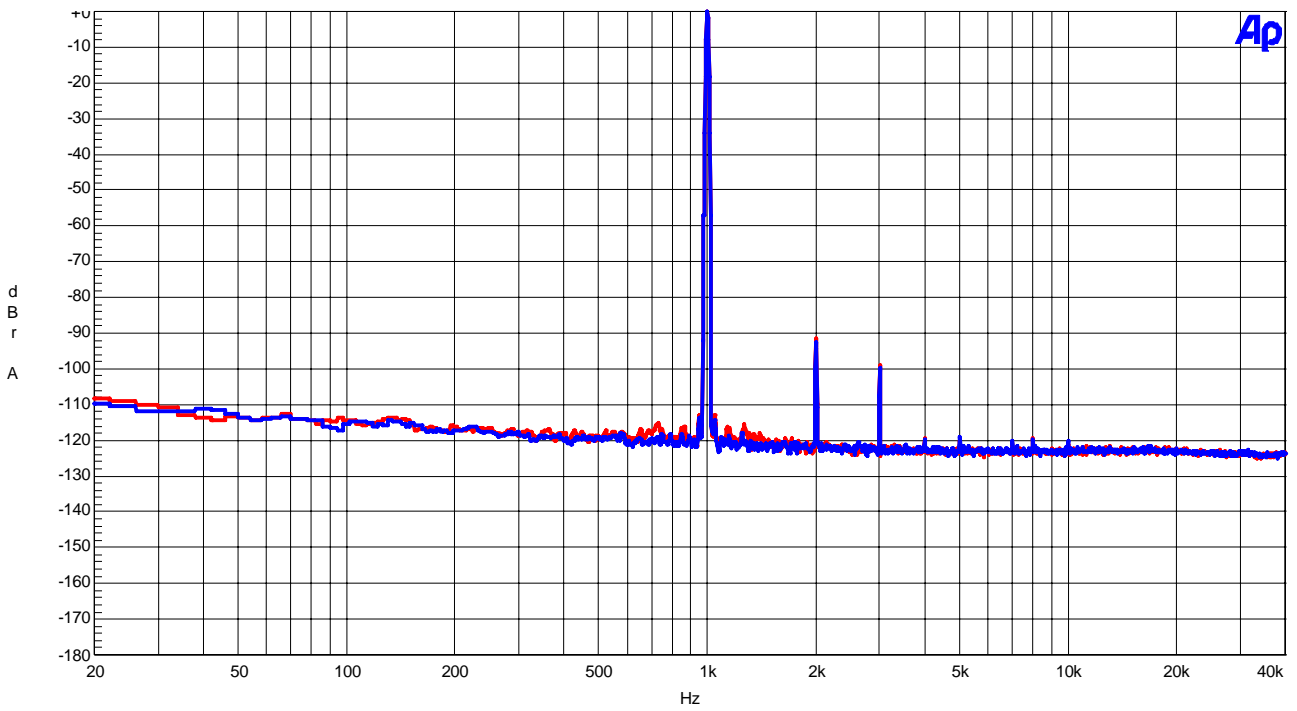


Figure 12. FFT (0dB)

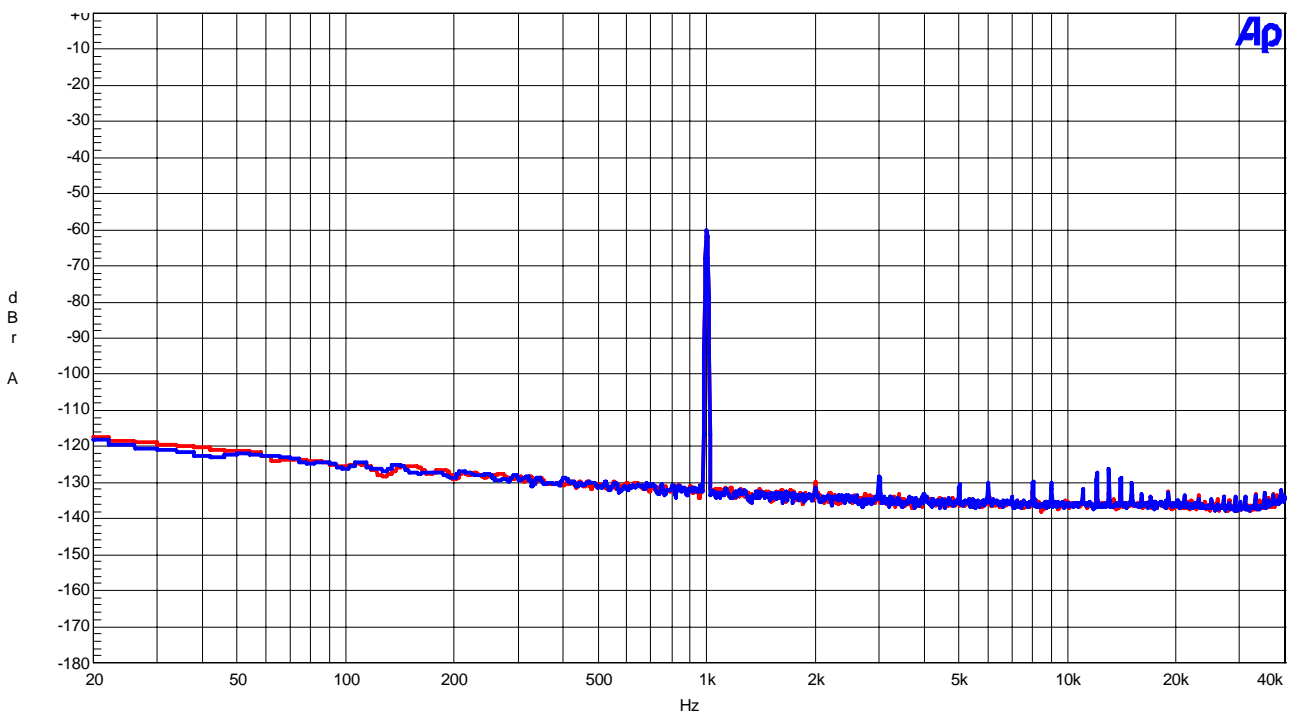


Figure 13. FFT (-60dB)

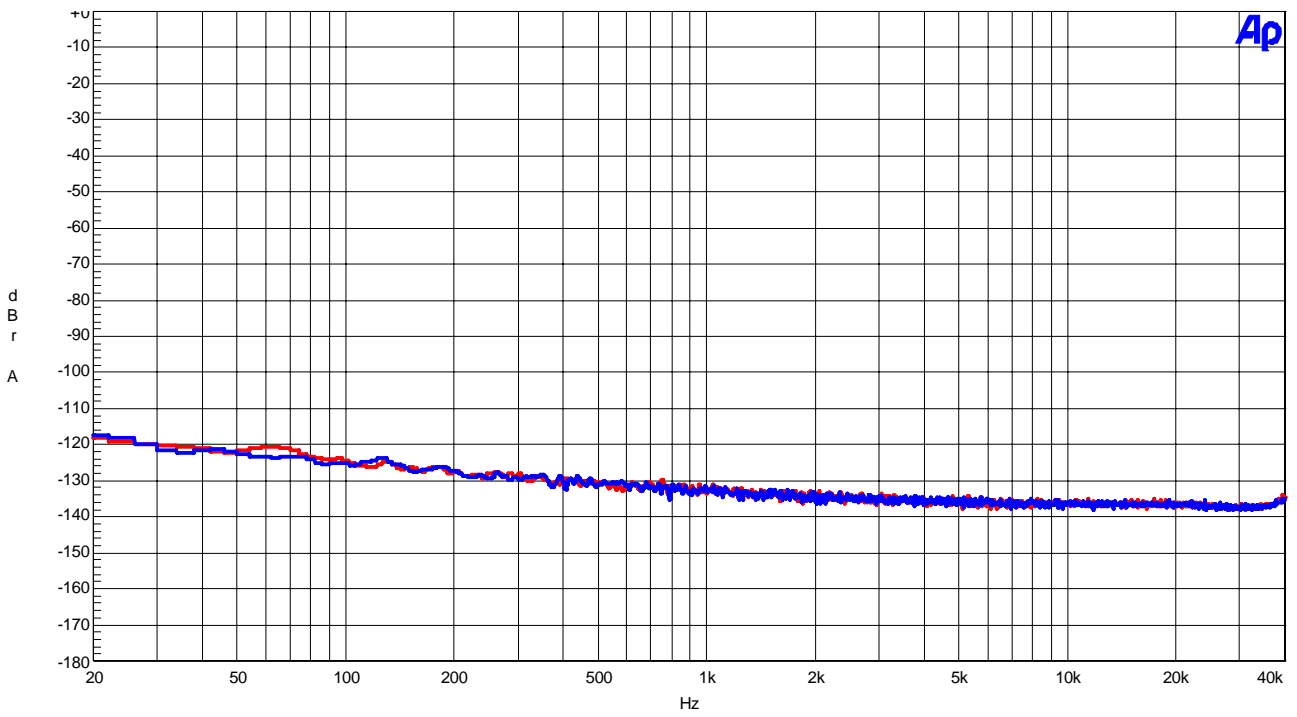


Figure 14. FFT (No Signal)

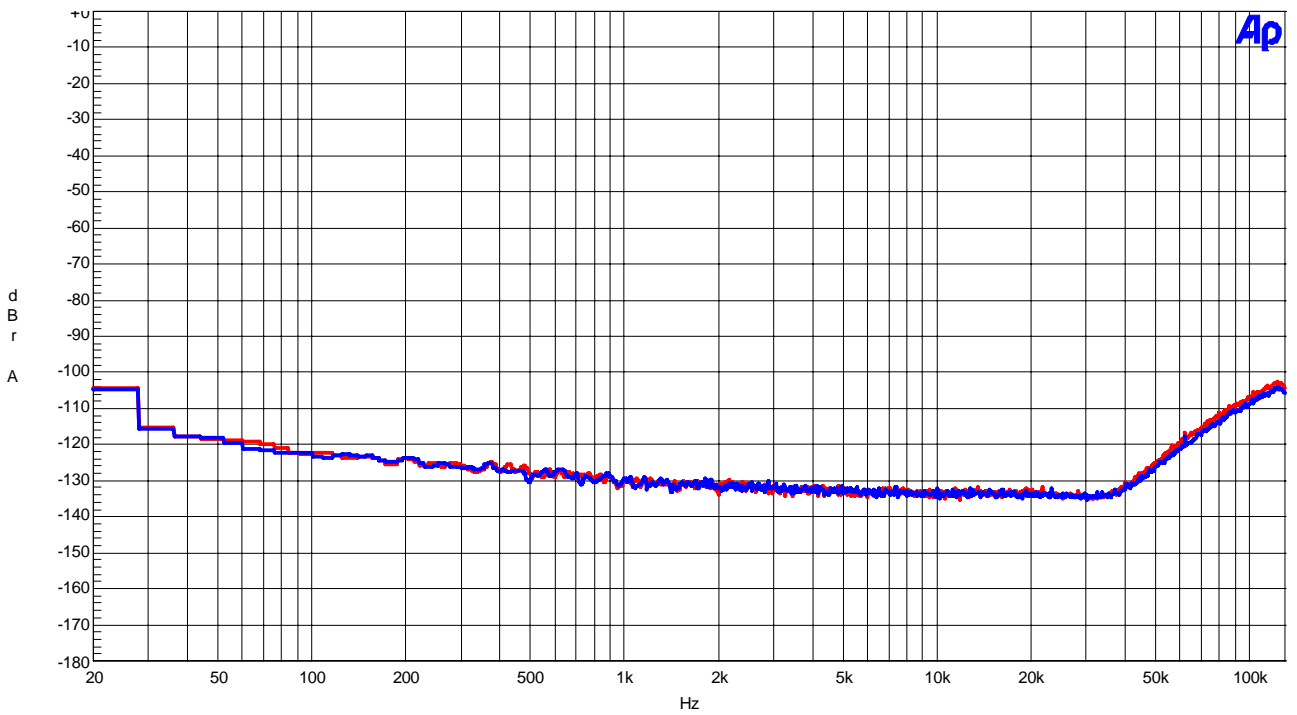


Figure 15. FFT (Out of Band Noise)

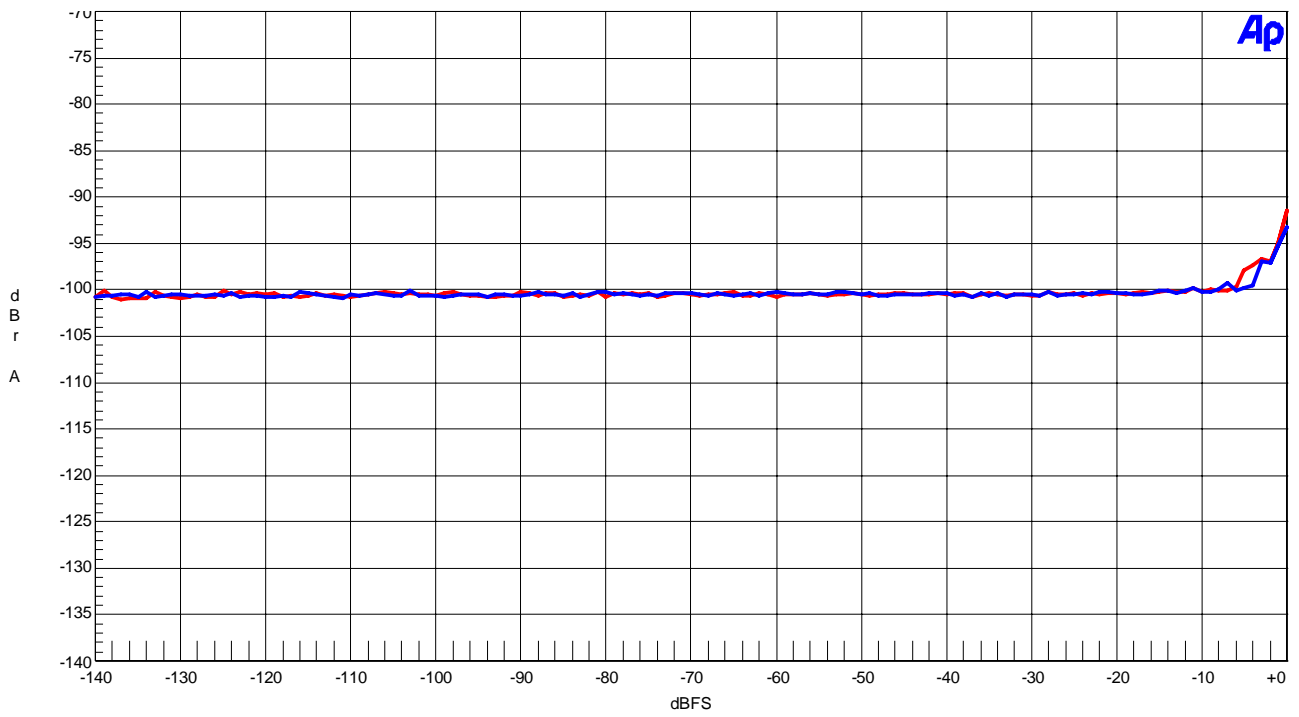


Figure 16. THD + N vs Input Level

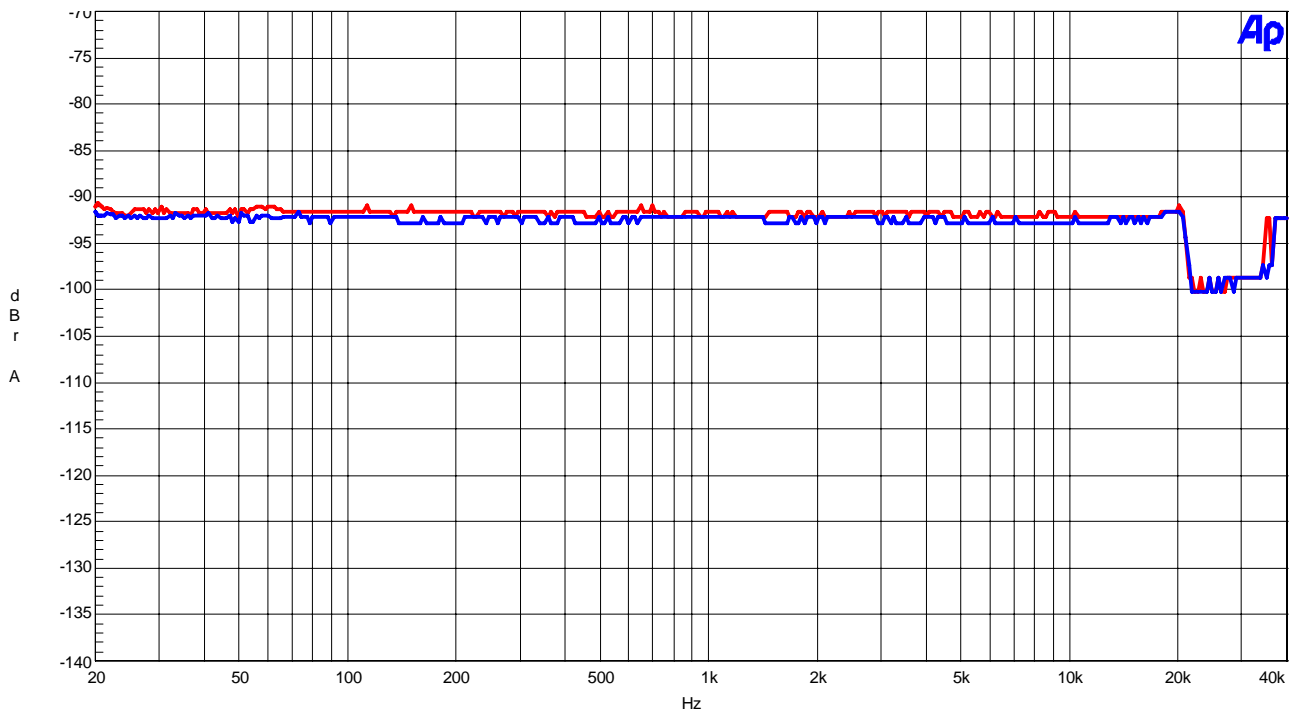


Figure 17. THD + N vs Input Frequency

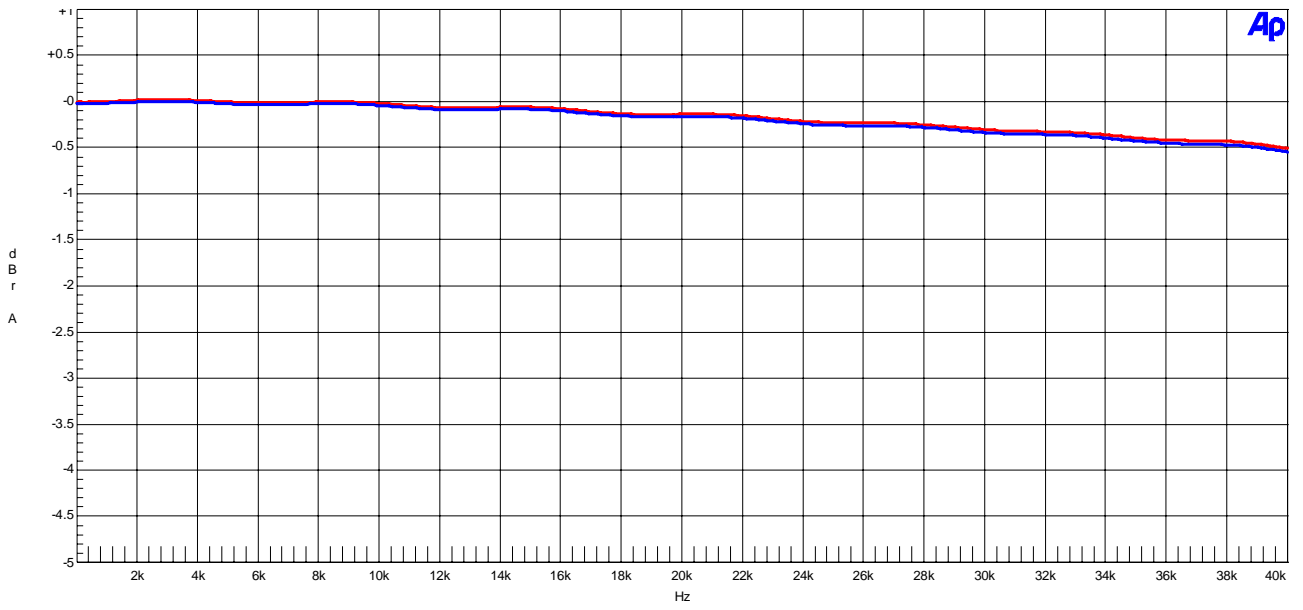


Figure 18. Frequency Response

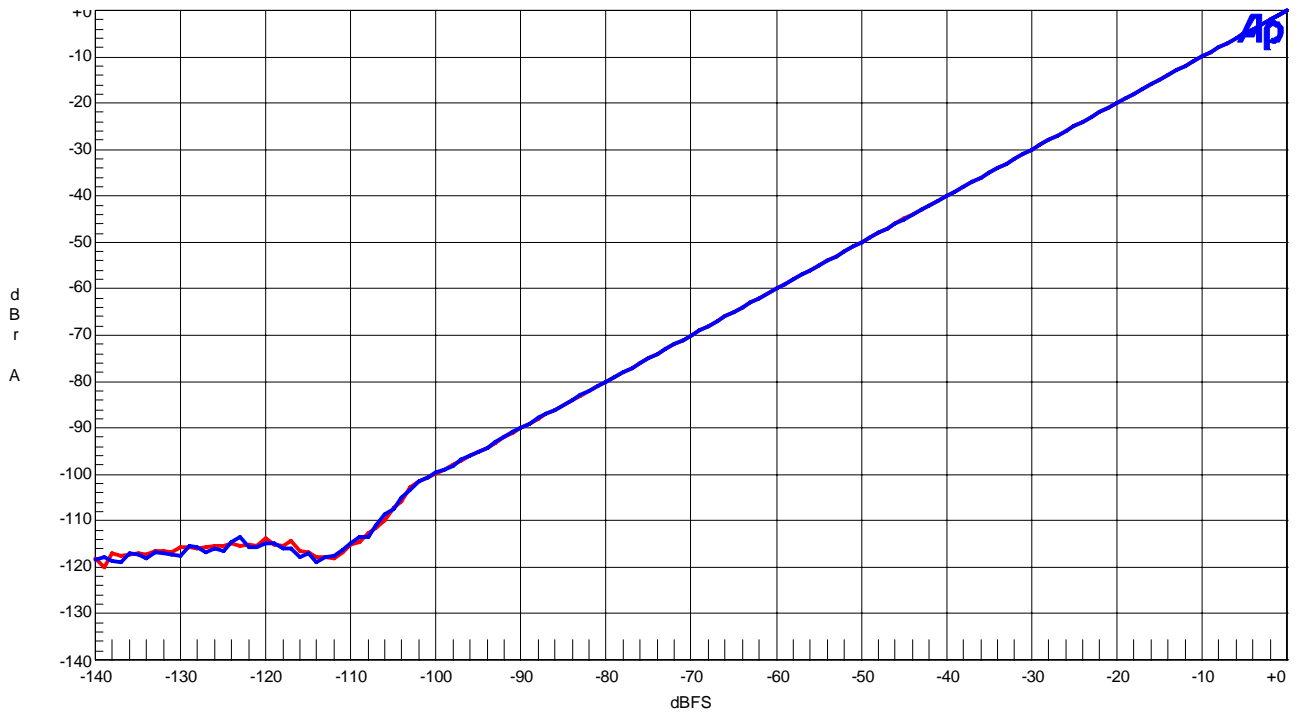


Figure 19. Linearity

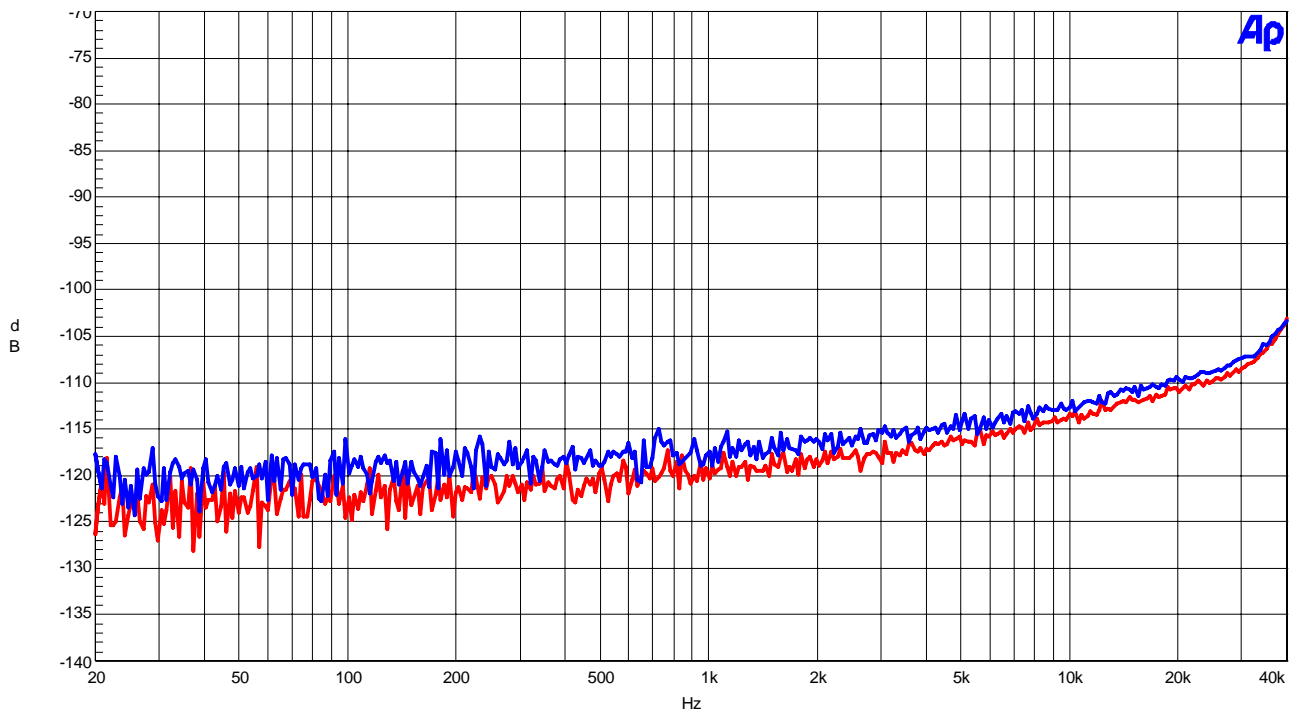


Figure 20. Crosstalk

fs=192KHz

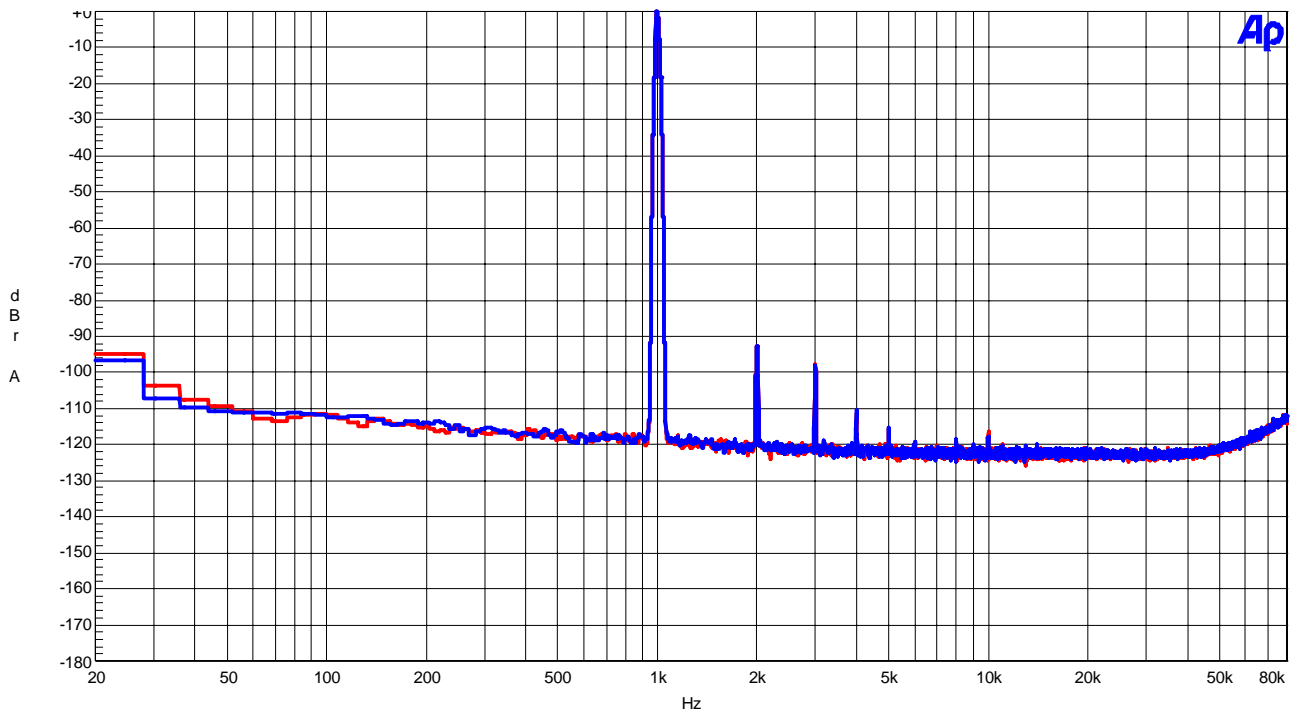


Figure 21. FFT (0dB)

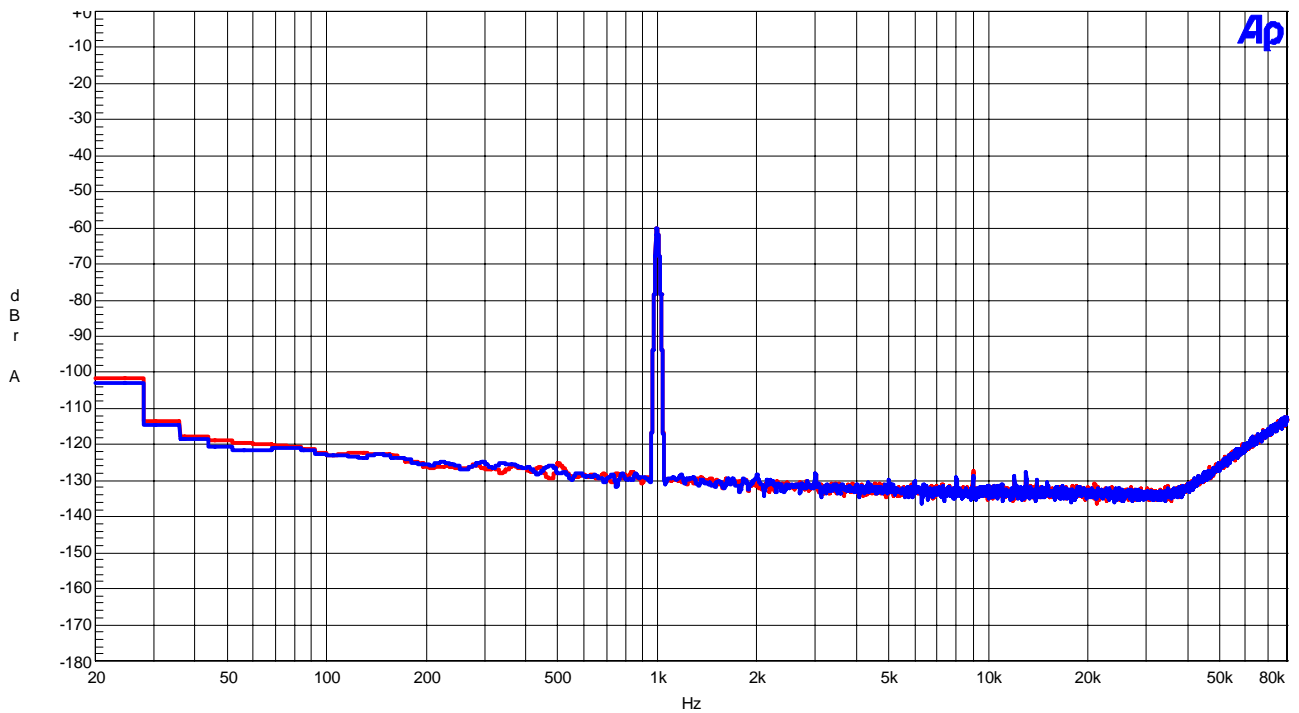


Figure 22. FFT (-60dB)



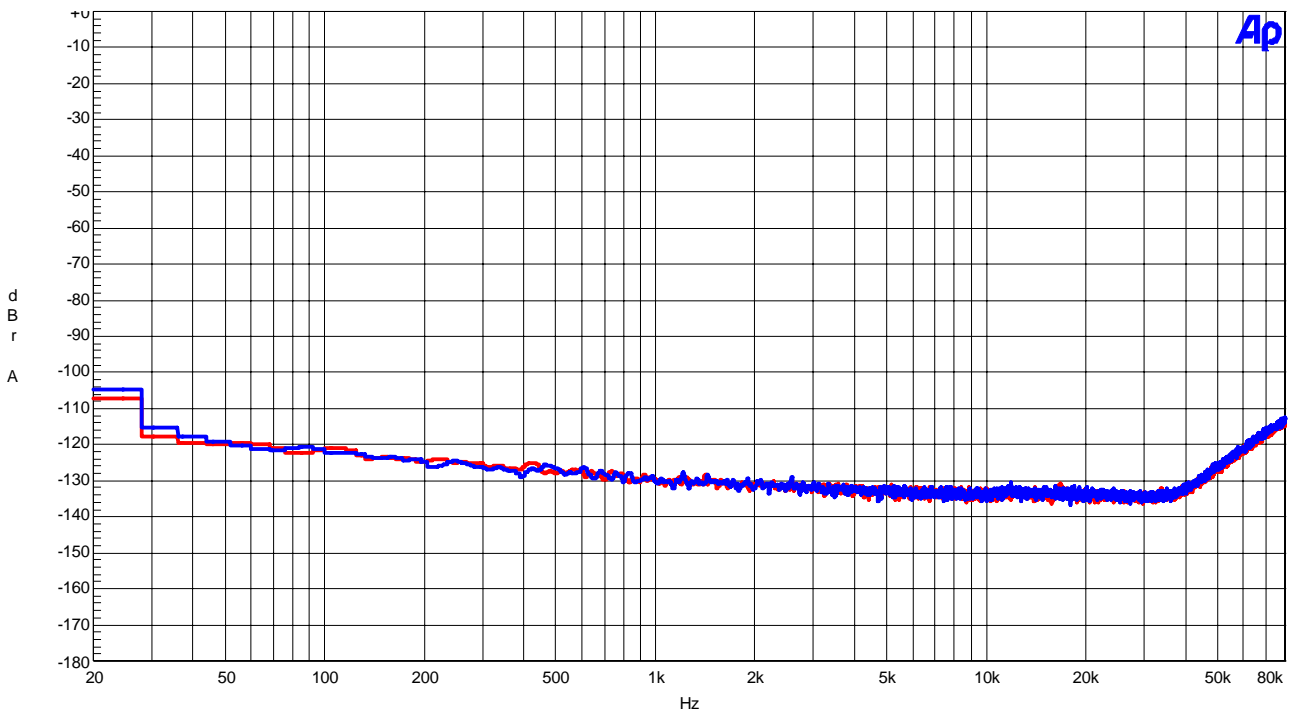


Figure 23. FFT (No Signal)

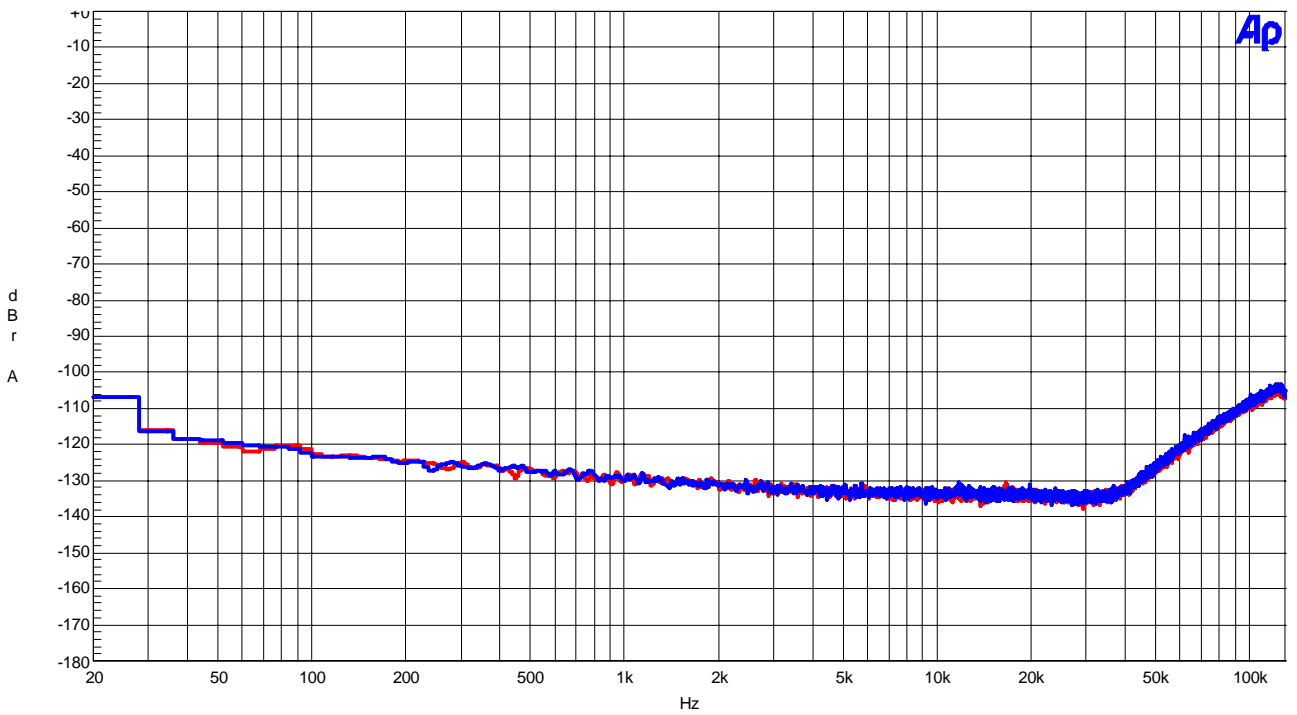


Figure 24. FFT (Out of Band Noise)

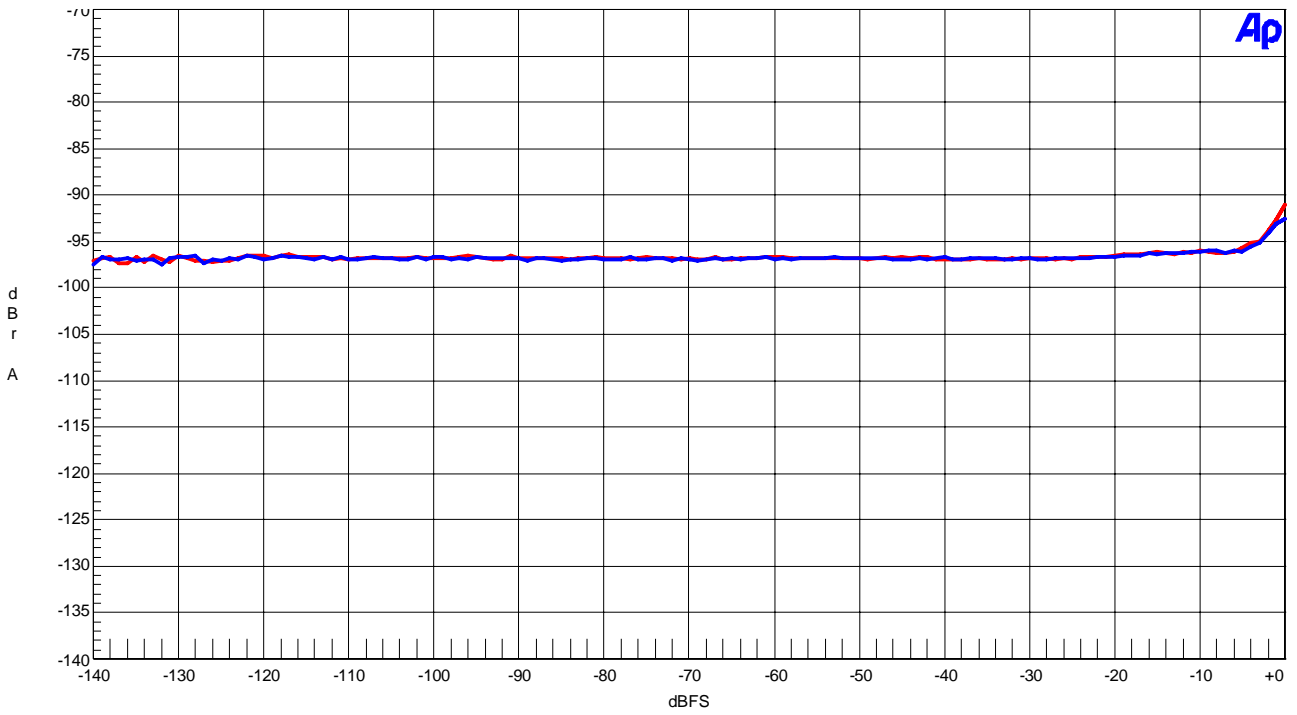


Figure 25. THD + N vs Input Level

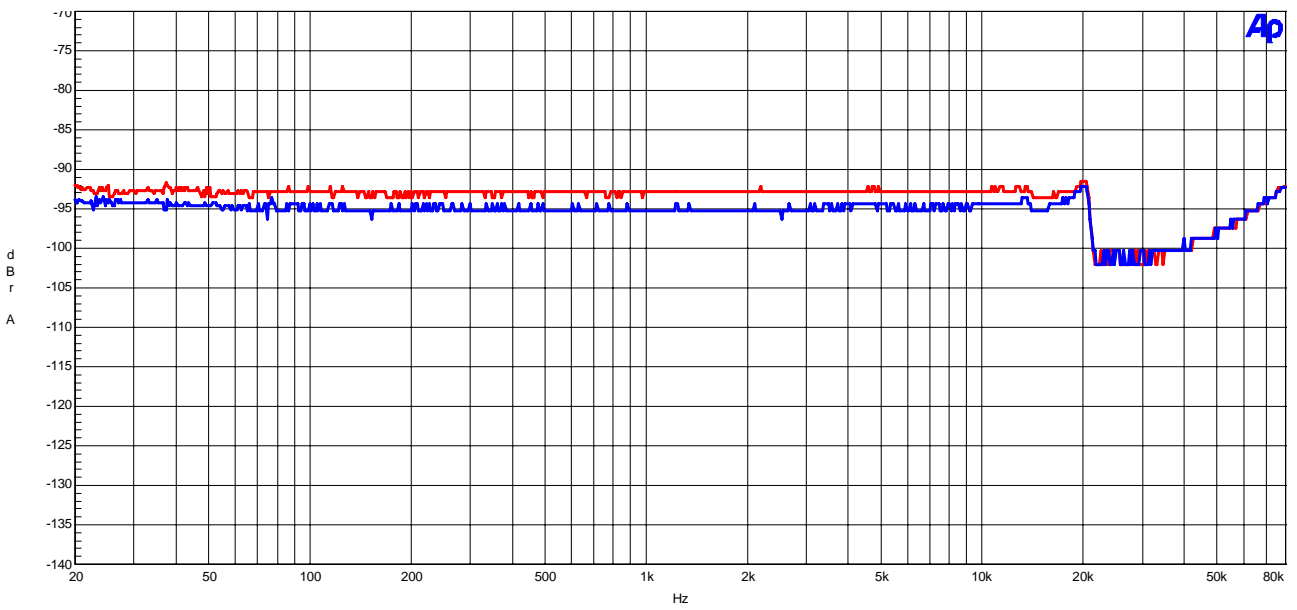


Figure 26. THD + N vs Input Frequency

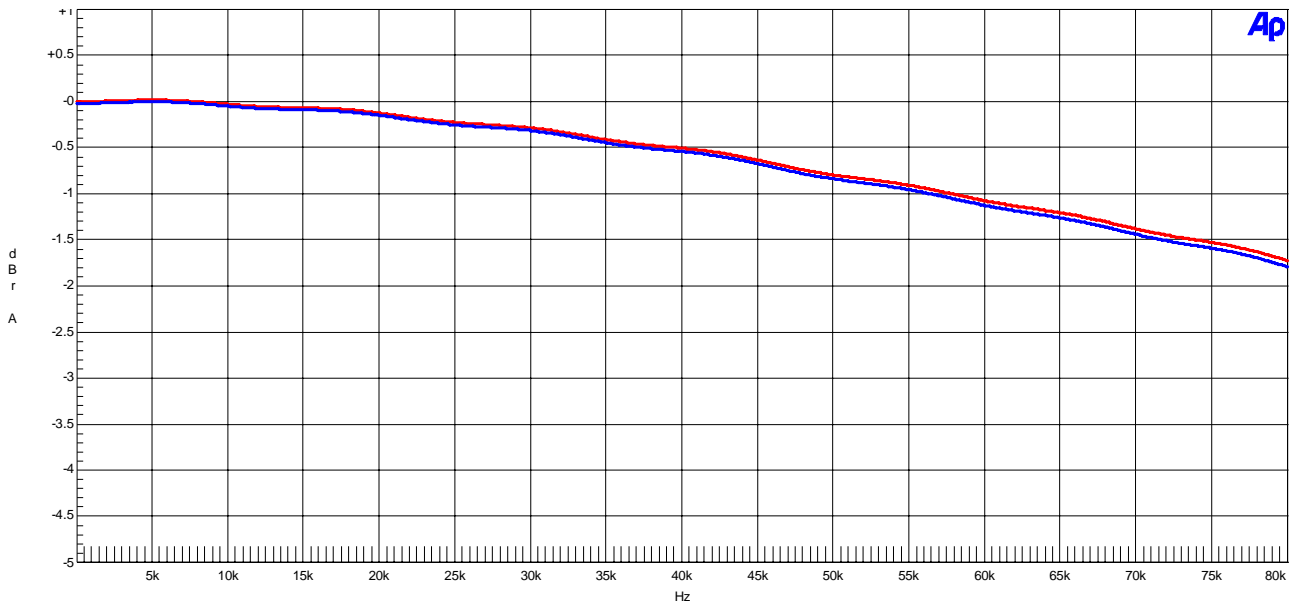


Figure 27. Frequency Response

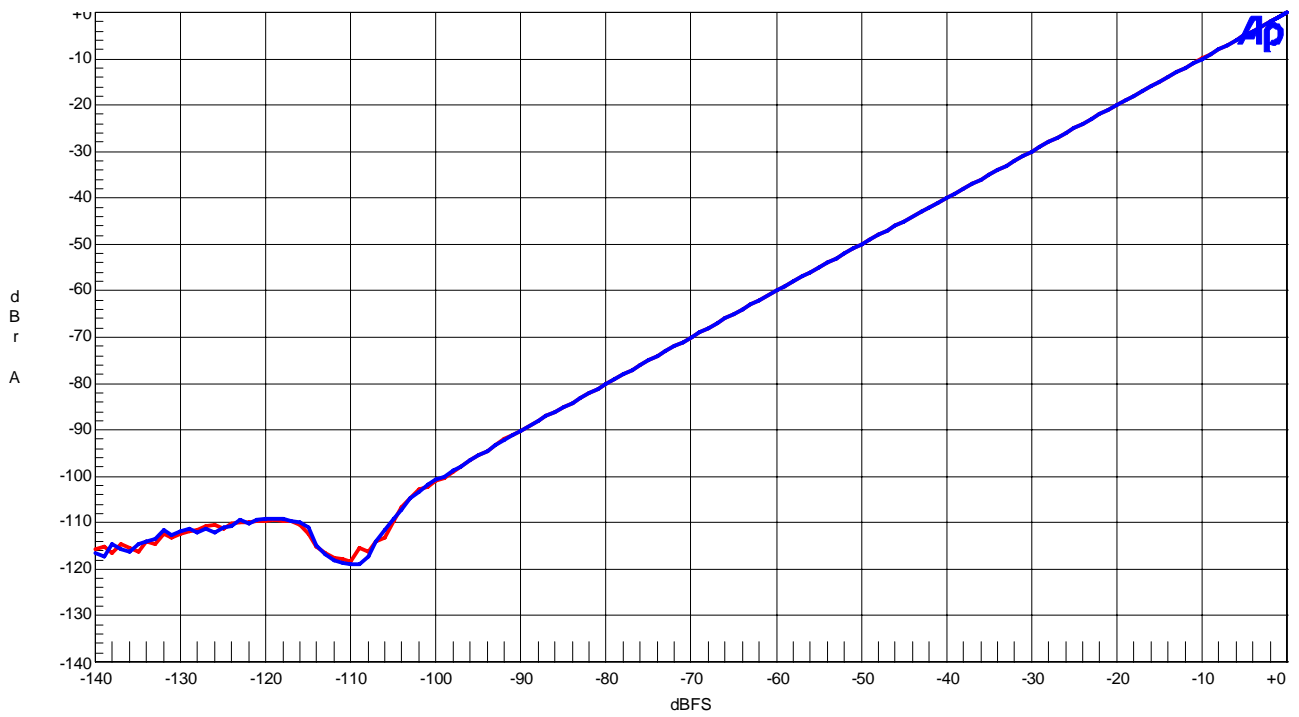


Figure 28. Linearity

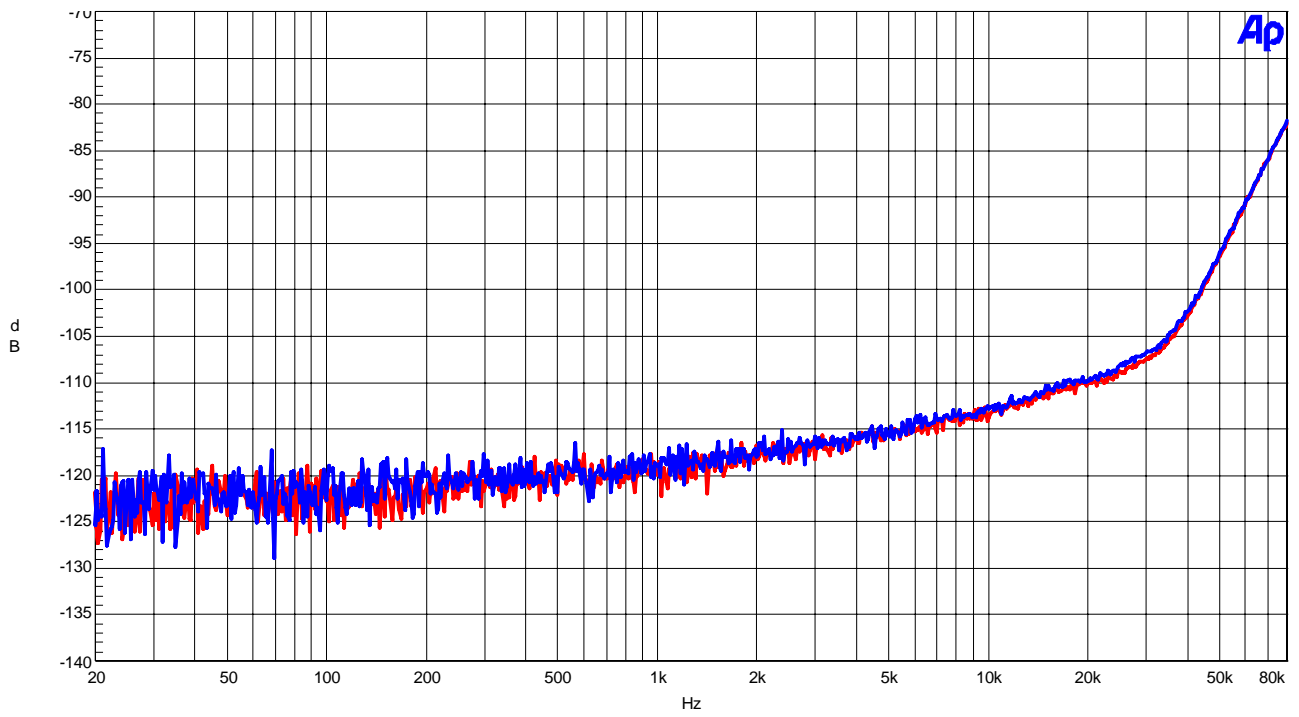


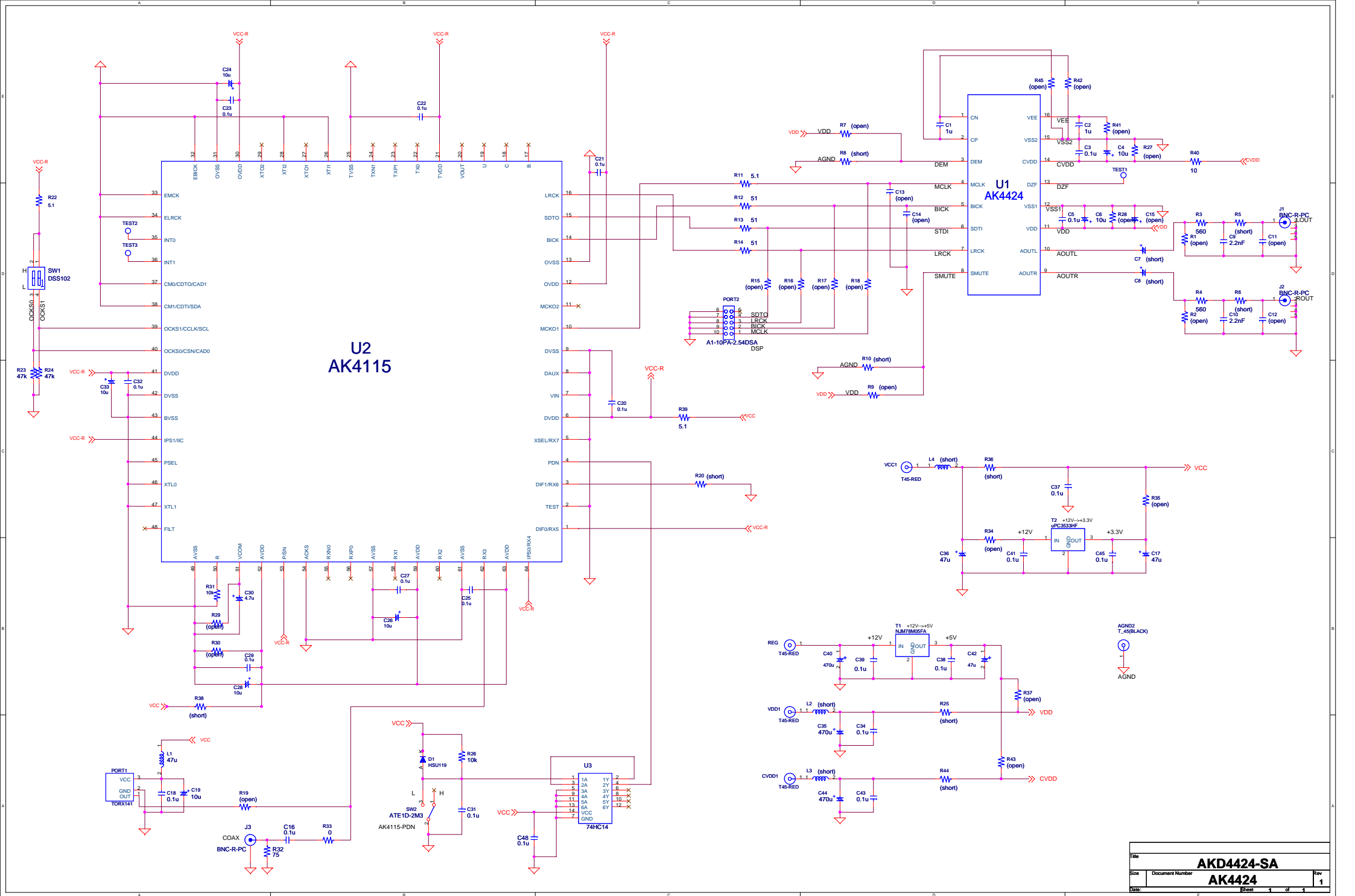
Figure 29. Crosstalk

<b>REVISION HISTORY</b>
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Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
08/01/24	KM092500	0	First Edition		
08/03/17	KM092501	1	Change	22	Circuit diagram was changed: Regulator: T2: TA48033F→uPC3533HF
			Change	1	Figure 1. Block diagram was changed.
			Change	3	Table 1. Set up of power supply lines was changed.

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