REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Make changes to table I, figure 1, and editorial changes throughout.	1990 JUNE 29	

REV																									
SHEET																									
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REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
15 AUGUST 1989

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, LINEAR, CMOS, 16-BIT, A/D CONVERTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-89676

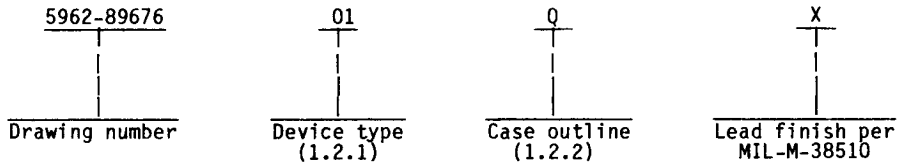
SHEET 1 OF 14

DESC FORM 193
SEP 87

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	INL test
01	CS5016-S	16-bit CMOS A/D converter, 16.25 µs	±5.0 LSB
02	CS5016-T	16-bit CMOS A/D converter, 16.25 µs	±1.0 LSB

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings 1/

Positive digital supply ($+V_D$) voltage range	-0.3 V dc to +6.0 V dc 2/
Negative digital supply ($-V_D$) voltage range	+0.3 V dc to -6.0 V dc
Positive analog supply ($+V_A$) voltage range	-0.3 V dc to +6.0 V dc
Negative analog supply ($-V_A$) voltage range	+0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND)	±0.5 V dc
Input current, any pin except supplies	±10 mA 3/
Analog input voltage (AIN and V_{REF} pins)	$-V_A$ - 0.3 V dc to $+V_A$ + 0.3 V dc
Digital input voltage	-0.3 V dc to $+V_D$ + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+195°C
Power dissipation (P_D):	
Case Q	1500 mW
Case X	1100 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case Q	45°C/W
Case X	60°C/W

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A$ +0.3 V dc.
3/ Transient currents of up to 100 mA will not cause latch-up.

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55°C to +125°C
Positive digital supply voltage ($+V_D$)	+4.5 V dc to $+V_A$ 2/
Negative digital supply voltage ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (V_{REF}) range	+4.5 V dc
Analog input voltage range:	
Unipolar mode	AGND to $+V_{REF}$
Bipolar mode	$-V_{REF}$ to $+V_{REF}$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

1/ All voltages reference to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A$ +0.3 V dc.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Resolution for which no missing codes is guaranteed	RES	1/	All	1,2,3	16		Bits
Integral linearity error	INL	1/ 2/	01	1,2,3		±5.0	LSB
			02			±1.0	
Full-scale error	FSE	1/ 2/	01	1,2,3		±4.0	LSB
			02			±3.0	
Full-scale error drift	$dFSE/d_t$	1/ 2/ 3/ 4/	All	2,3		±4.0	LSB
Unipolar offset error	VOFF	1/ 2/	01	1,2,3		±4.0	LSB
			02			±3.0	
Unipolar offset error drift	$dVOFF/d_t$	1/ 2/ 3/ 4/	All	2,3		±2.0	LSB
Bipolar offset error	BOFF	1/ 2/	01	1,2,3		±4.0	LSB
			02			±2.0	
Bipolar offset error drift	$dBOFF/d_t$	1/ 2/ 3/ 4/	All	2,3		±3.0	LSB
Bipolar negative full-scale error	BNFSE	1/ 2/	01	1,2,3		±5.0	LSB
			02			±3.0	
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/ 2/ 3/ 4/	All	2,3		±3.0	LSB
Peak harmonic or spurious noise	S/PN	1 kHz input, full scale amplitude, bipolar mode 1/ 2/	01	4,5,6	92		dB
			02		100		
		12 kHz input, full scale amplitude, bipolar mode 1/ 2/	01		82		dB
			02		85		
Signal to noise ratio	S/(N+D)	1 kHz input, full scale amplitude, bipolar mode 1/ 2/	01	4,5,6	84		dB
			02		90		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Analog input capacitance in fine mode	C_{IN}	Unipolar mode $T_A = +25°C$ 1/ 3/	All	4		375	pF
		Bipolar mode $T_A = +25°C$ 1/ 3/				220	
Digital input voltage ($\overline{HOLD}$, CLKIN, CAL, $\overline{INTRLV}$, BW, RST, BP/$\overline{UP}$, $\overline{AU}$, RD, $\overline{CS}$)	V_{IH}	5/ 6/	All	1,2,3	2.0		V
	V_{IL}					0.8	
Digital input current	I_{IN}	5/ 6/	All	1,2,3		±10	µA
Digital output voltage (D_0-D_{15}, SDATA, SCLK, $\overline{EOC}$, $\overline{EOT}$)	V_{OL}	Logic "0", 5/ 6/ $I_{SINK} = 1.6$ mA	All	1,2,3		0.4	V
	V_{OH}	Logic "1", 5/ 6/ $I_{SOURCE} = 100$ µA			+VD -1.0		
High impedance state output current	I_{OZ}	Pins D_0 to D_{15} only, 5/ 6/	All	1,2,3		±10	µA
Conversion time	t_C	1/ 6/ 7/	All	9,10,11		16.25	µs
Acquisition time	t_{ACQ}	$T_A = +25°C$ 1/ 2/ 3/ 8/	All	9		3.75	µs
Throughput	t_{PUT}	1/ 2/ 6/	All	9,10,11	50		kHz
Positive analog supply current	I_{A^+}	$+V_A$, $+V_D = 5.5$ V 6/ $-V_A$, $-V_D = -5.5$ V 9/	All	1,2,3		19.0	mA
Negative analog supply current	I_{A^-}	$+V_A$, $+V_D = 5.5$ V 6/ $-V_A$, $-V_D = -5.5$ V 9/	All	1,2,3		19.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Positive digital supply current	I_{D^+}	$+V_A$, $+V_D$ = 5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1,2,3		6.0	mA
Negative digital supply current	I_{D^-}	$+V_A$, $+V_D$ = 5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1,2,3		6.0	mA
Master clock frequency 10/	f_{CLK}	Internally generated, CLKIN = 0 V dc, T_A = -55°C $+V_D$, $+V_A$ = 4.5 V, $-V_D$, $-V_A$ = -4.5 V	All	11	1.75		MHz
$\overline{HOLD}$ pulse width	t_{HPW}	5/ 6/ 11/ (see figure 4)	All	9,10,11	$\frac{1}{f_{CLK}}$ +50	t_C	ns
Data delay time	t_{DD}	5/ 6/ 11/ (see figure 4)	All	9,10,11		100	ns
$\overline{EOC}$ pulse width	t_{EPW}	5/ 6/ 11/ (see figure 4)	All	9,10,11	$\frac{4}{f_{CLK}}$ -20		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	5/ 6/ 11/ (see figure 5)	All	9,10,11	20		ns
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	5/ 6/ 11/ (see figure 5)	All	9,10,11	20		ns
$\overline{CS}$ or $\overline{RD}$ high to A0 invalid hold time	t_{AH}	5/ 6/ 11/ (see figure 5)	All	9,10,11	50		ns
$\overline{CS}$ high to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	5/ 6/ 11/ (see figure 5)	All	9,10,11	50		ns
$\overline{CS}$ low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0", 5/ 6/ 11/ (see figure 5)	All	9,10,11		150	ns
$\overline{RD}$ low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0", 5/ 6/ 11/ (see figure 5)	All	9,10,11		150	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Output float delay	t_{FD}	5/ 6/ 11/ (see figure 5)	All	9,10,11		140	ns
SDATA to SCLK rising setup time	t_{SS}	5/ 6/ 11/ (see figure 6)	All	9,10,11	$\frac{2}{f_{CLK}} - 50$		ns
SCLK rising to SDATA hold time	t_{SH}	5/ 6/ 11/ (see figure 6)	All	9,10,11	$\frac{2}{f_{CLK}} - 100$		ns

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = -5.0 V; V_{REF} = +4.5 V dc; f_{CLK} = 4 MHz; analog source impedance = 200 ohms; error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), interleave disabled.

3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.

4/ Total drift over -55°C to +125°C since calibration at power-up at +25°C.

5/ $+V_A$, $+V_D$ = +5.0 V dc ± 10%; $-V_A$, $-V_D$ = -5.0 V dc ± 10%.

6/ This parameter is guaranteed, if not tested, at T_A = +25°C. This parameter is tested at T_A = -55°C and +125°C.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; all inputs swinging between $+V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4 MHz. Analog parametric measurements are done with the maximum external clock (see 1/).

11/ Inputs: logic "0" = 0 V, logic "1" = $+V_D$; C_L = 50 pF.

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Device types	01 and 02		Device types	01 and 02	
Case outlines	Q	X	Case outlines	Q	X
Terminal number	Terminal symbols		Terminal number	Terminal symbols	
1	$\overline{HOLD}$	$\overline{HOLD}$	23	AO	CLKIN
2	D_0	D_0	24	BP/$\overline{UP}$	$\overline{CS}$
3	D_1	D_1	25	$+V_A$	$\overline{RD}$
4	D_2	D_2	26	AIN	AO
5	D_3	D_3	27	AGND	BP/$\overline{UP}$
6	D_4	D_4	28	V_{REF}	$+V_A$
7	D_5	D_5	29	REFBUF	AIN
8	D_6	D_6	30	$-V_A$	AGND
9	D_7	NC	31	TST	V_{REF}
10	DGND	D7	32	RST	REFBUF
11	$+V_D$	DGND	33	BW	NC
12	D_8	$+V_D$	34	$\overline{INTRLV}$	$-V_A$
13	D_9	NC	35	CAL	TST
14	D_{10}	D_8	36	$-V_D$	RST
15	D_{11}	NC	37	$\overline{EOT}$	BW
16	D_{12}	D_9	38	$\overline{EOC}$	$\overline{INTRLV}$
17	D_{13}	D_{10}	39	SCLK	CAL
18	D_{14}	D_{11}	40	SDATA	$-V_D$
19	D_{15}	D_{12}	41	---	$\overline{EOT}$
20	CLKIN	D_{13}	42	---	$\overline{EOC}$
21	$\overline{CS}$	D_{14}	43	---	SCLK
22	$\overline{RD}$	D_{15}	44	---	SDATA

FIGURE 1. Terminal connections

Function	$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST
Hold and start convert		X	X	X	X	*	0
Initiate burst calibration	X	0	1	X	X	*	0
Stop burst calibration and begin track	1	0	0	X	X	*	0
Initiate interleave calibration	X	0	X	0	X	*	0
Terminate interleave calibration	X	0	X	1	X	*	0
Read output data	X	0	X	X	0	1	0
Read status register	1	0	X	X	0	0	0
High impedence data bus	X	1	X	X	X	*	X
High impedence data bus	X	X	X	X	1	*	X
Reset	X	X	X	X	X	X	1
Reset	0	0	X	X	X	0	X

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table

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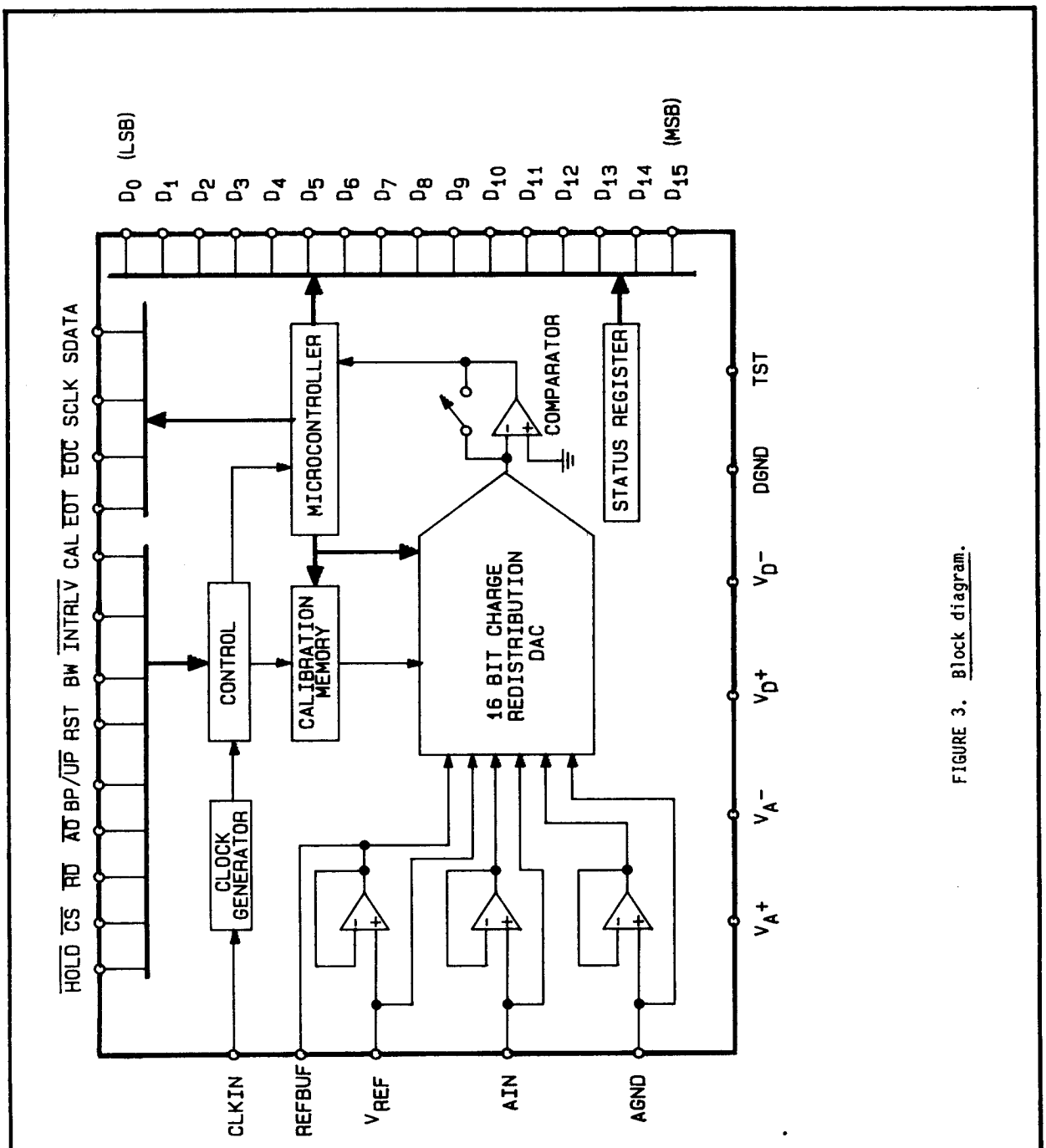

FIGURE 3. Block diagram.

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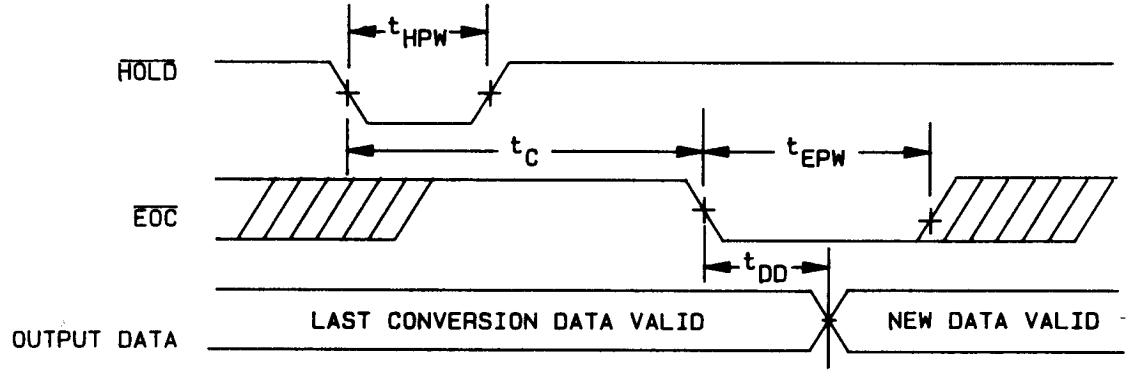

FIGURE 4. Conversion timing.

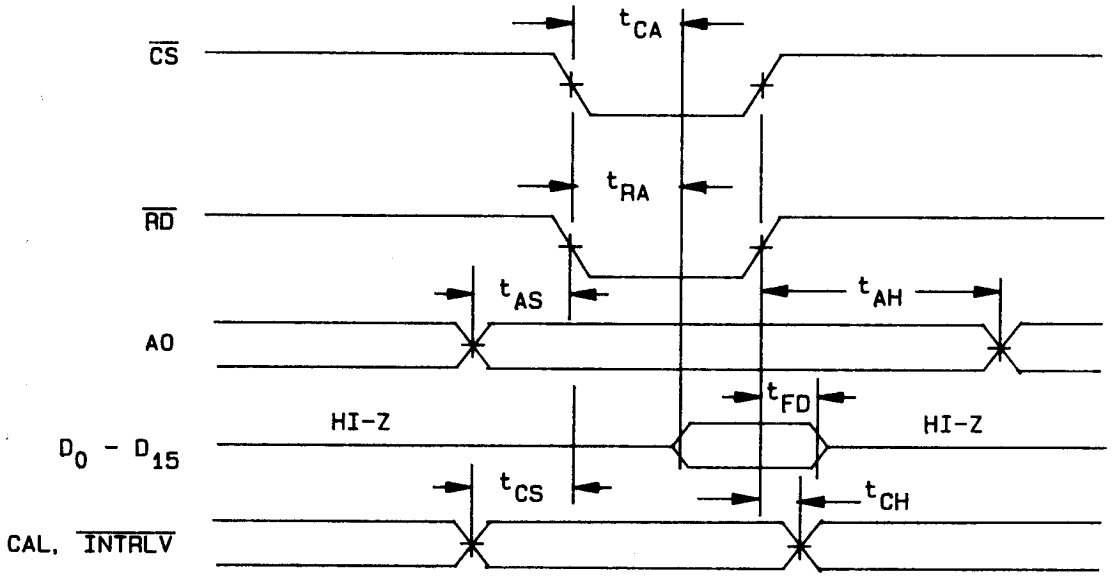

FIGURE 5. Read and calibration control timing.

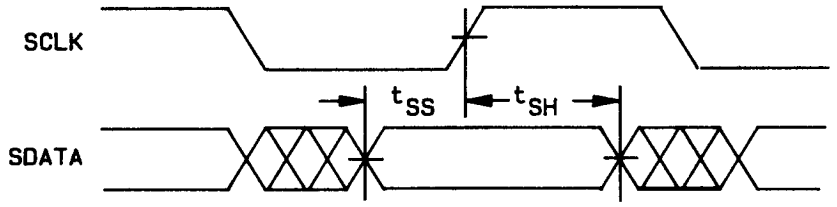

FIGURE 6. Serial output timing.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5004)	1, 2, 3, 4, 5, 6, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9, if not tested, shall be guaranteed to the limits specified in table I herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8967601QX	0A384	CS5016-SD16B
5962-8967601XX	0A384	CS5016-SE16B
5962-8967602QX	0A384	CS5016-TD16B
5962-8967602XX	0A384	CS5016-TE16B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin, Texas 78760

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