

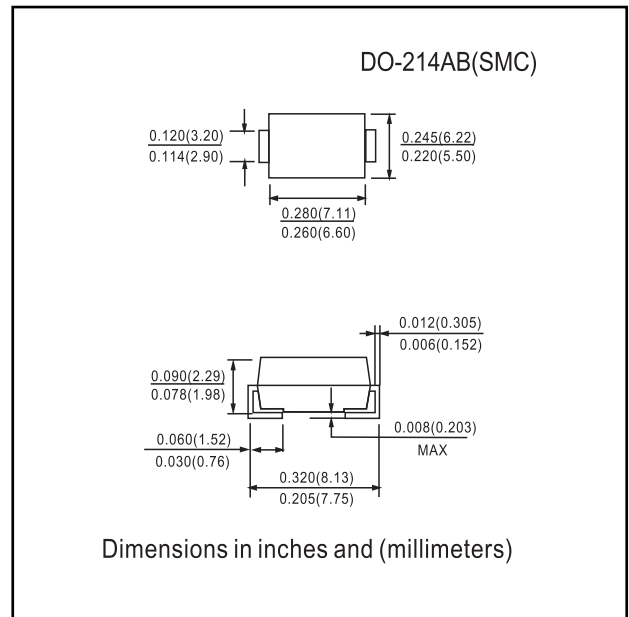


FEATURES

- Low power loss, high efficiency
- Low profile surface mount package
- Built-in strain relief
- For use in low voltage high frequency inverters, free wheeling, and polarity protection applications
- Guardring for overvoltage protection
- Plastic package has Underwriters Laboratory Flammability Classification 94V-0

MECHANICAL DATA

Case: JEDEC DO-214AB molded plastic body
Terminals: Solder plated, solderable per MIL-STD750, Method 2026
 High temperature soldering guaranteed: 250°C/10 seconds at terminals
Polarity: Color band denotes cathode end
Weight: 0.007 oz., 0.25 g



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)

Parameter	Symbol	SSC53L	SSC54	Unit
Device marking code		53L	S54	
Maximum repetitive peak reverse voltage	VRRM	30	40	V
Maximum RMS voltage	VRMS	21	28	V
Maximum DC blocking voltage	VDC	30	40	V
Maximum average forward rectified current at TL (See Fig. 1)	IF(AV)	5.0		A
Peak forward surge current 8.3ms single half sine-wave superimposed on rated load (JEDEC Method)	IFSM	175		A
Typical thermal resistance ⁽²⁾	RθJA RθJL	60 20		°C/W
Voltage rate of change (rated VR)	dv/dt	10,000		V/μs
Operating junction temperature range	TJ	-65 to +150		°C
Storage temperature range	TSTG	-65 to +150		°C

Electrical Characteristics (TA = 25°C unless otherwise noted)

Parameter	Symbol	Typ.	Max.	Typ.	Max.	Unit
Maximum instantaneous Forward voltage at 5.0A ⁽¹⁾	VF	0.42	0.45	0.45	0.49	V
		TJ=25°C TJ=125°C	0.33	0.38	0.36	0.42
Maximum DC reverse current at rated DC blocking voltage ⁽¹⁾	IR	-	0.7	-	0.5	mA
		TJ=25°C TJ=125°C	45	65	40	60

Notes: (1) Pulse test: 300μs pulse width, 1% duty cycle
 (2) Aluminum substrate mounted



RATINGS AND CHARACTERISTIC CURVES

SSC53L and SSC54

Fig. 1 – Forward Current Derating Curve

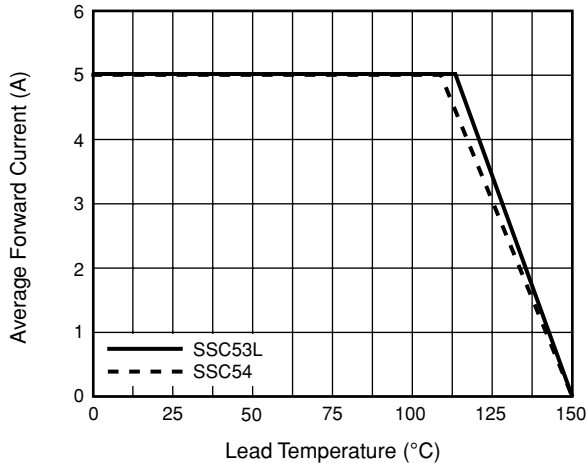


Fig. 2 – Maximum Non-Repetitive Peak Forward Surge Current

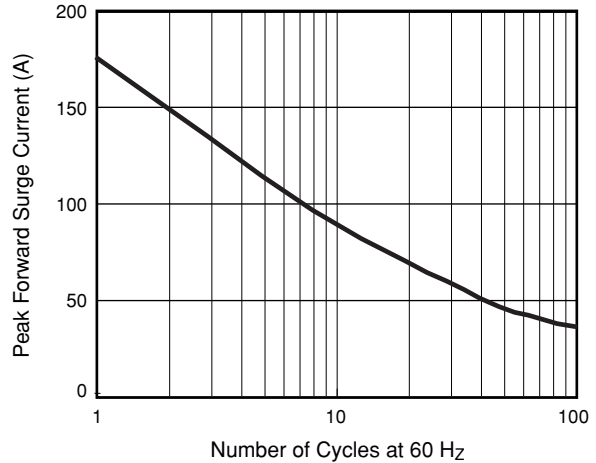


Fig. 3 – Typical Instantaneous Forward Characteristics

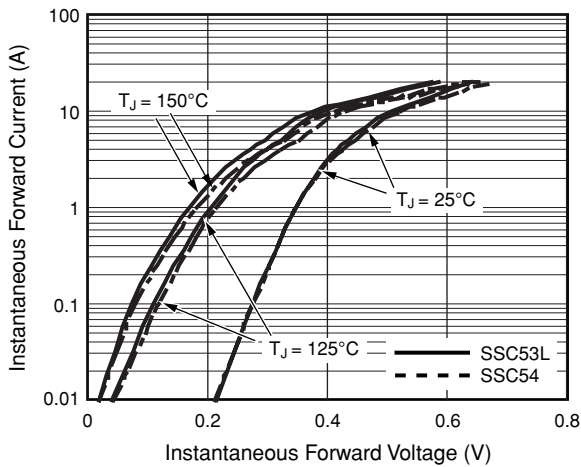


Fig. 4 – Typical Reverse Characteristics

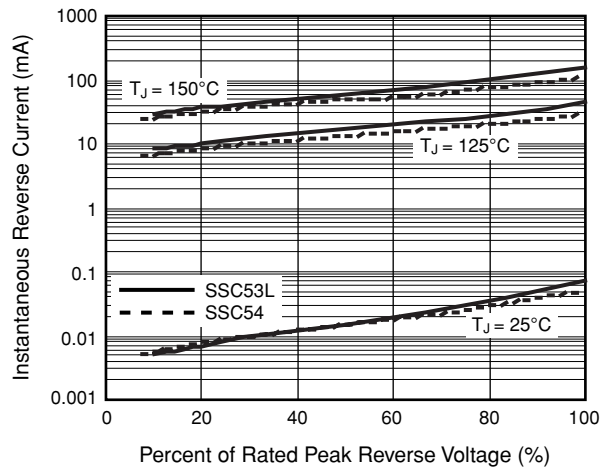


Fig. 5 – Typical Junction Capacitance

