Ordering number : ENA0788

SANYO Semiconductors
DATA SHEET

LC72131K, LC72131KM — CMOS IC PLL Frequency Synthesizer

Overview

The LC72131K and LC72131KM are PLL frequency synthesizers for use in tuners in radio/cassette players. They allow high-performance AM/FM tuners to be implemented easily.

Features

- High speed programmable dividers
  - FMIN: 10 to 160MHz …………………….. pulse swallower (built-in divide-by-two prescaler)
  - AMIN: 2 to 40MHz ………………………. pulse swallower
    0.5 to 10MHz …………………….. direct division
- IF counter
  - IFIN: 0.4 to 12MHz ………………………. AM/FM IF counter
- Reference frequencies
  - Twelve selectable frequencies (4.5 or 7.2MHz crystal)
  - 100, 50, 25, 15, 12.5, 6.25, 3.125, 10, 9, 5, 3, 1kHz
- Phase comparator
  - Dead zone control
  - Unlock detection circuit
  - Deadlock clear circuit
  - Built-in MOS transistor for forming an active low-pass filter
- I/O ports
  - Dedicated output ports: 4 • Input or output ports: 2 • Support clock time base output

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- Serial data I/O
  - Support CCB format communication with the system controller.
- Operating ranges
  - Supply voltage ....4.5 to 5.5V
  - Operating temperature .... -40 to +85°C
- Packages
  - DIP22S/MFP20

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Pins	Conditions	Ratings	Unit
Supply voltage	V_{DD} max	V_{DD}		-0.3 to +7.0	V
Maximum input voltage	$V_{IN}1$ max	CE, CL, DI, AIN		-0.3 to +7.0	V
	$V_{IN}2$ max	XIN, FMIN, AMIN, IFIN		-0.3 to V_{DD}+0.3	V
	$V_{IN}3$ max	$\overline{IO1}$, $\overline{IO2}$		-0.3 to +15	V
Maximum output voltage	V_O1 max	DO		-0.3 to +7.0	V
	V_O2 max	XOUT, PD		-0.3 to V_{DD}+0.3	V
	V_O3 max	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$, AOUT		-0.3 to +15	V
Maximum output current	I_O1 max	$\overline{BO1}$		0 to 3.0	mA
	I_O2 max	DO, AOUT		0 to 6.0	mA
	I_O3 max	$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$		0 to 10	mA
Allowable power dissipation	Pd max		Ta≤85°C [LC72131K]	350	mW
			Ta≤85°C [LC72131KM]	180	mW
Operating temperature	Topr			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

Note 1: Power pins V_{DD} and V_{SS}: Insert a capacitor with a capacitance of 2,000pF or higher between these pins when using the IC.

Allowable Operating Ranges at Ta = -40°C to +85°C, V_{SS} = 0V

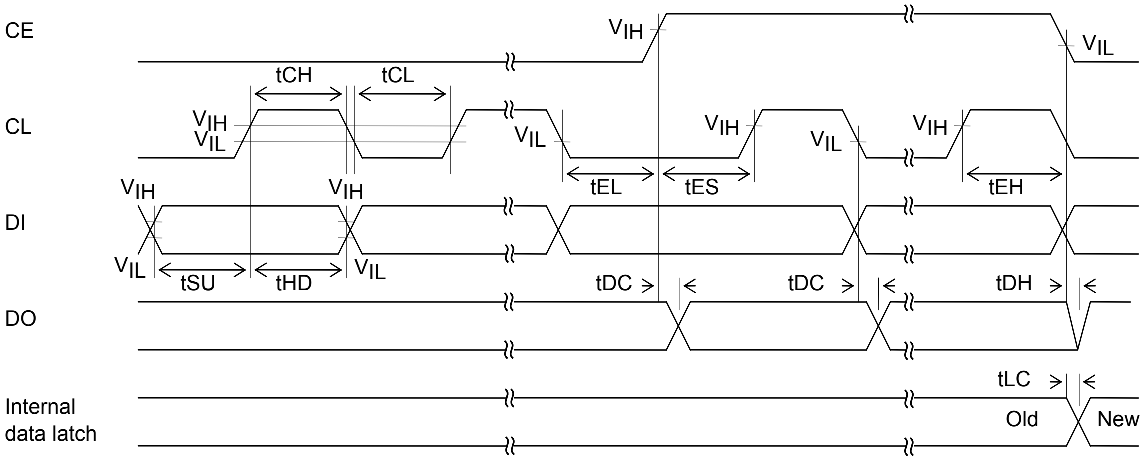
Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Supply voltage	V_{DD}	V_{DD}		4.5		5.5	V
Input high-level voltage	$V_{IH}1$	CE, CL, DI		$0.7V_{DD}$		6.5	V
	$V_{IH}2$	$\overline{IO1}$, $\overline{IO2}$		$0.7V_{DD}$		13	V
Input low-level voltage	V_{IL}	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$		0		$0.3V_{DD}$	V
Output voltage	V_O1	DO		0		6.5	V
	V_O2	$\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$, AOUT		0		13	V
Input frequency	fIN1	XIN	$V_{IN}1$	1.0		8.0	MHz
	fIN2	FMIN	$V_{IN}2$	10		160	MHz
	fIN3	AMIN	$V_{IN}3$	2.0		40	MHz
	fIN4	AMIN	$V_{IN}4$	0.5		10	MHz
	fIN5	IFIN	$V_{IN}5$	0.4		12	MHz
Supported crystals	X'tal	XIN, XOUT	Note 1	4.0		8.0	MHz
Input amplitude High-level clock pulse width tφH CL [Figure 1][Figure 2] 160 ns Low-level clock pulse width	$V_{IN}1$	XIN	fIN1	400		1500	mVrms
	$V_{IN}2$-1	FMIN	f=10 to 130MHz	40		1500	mVrms
	$V_{IN}2$-2	FMIN	f=130 to 160MHz	70		1500	mVrms
	$V_{IN}3$	AMIN	fIN3	40		1500	mVrms
	$V_{IN}4$	AMIN	fIN4	40		1500	mVrms
	$V_{IN}5$	IFIN	fIN5 (IFS=1)	40		1500	mVrms
	$V_{IN}6$	IFIN	fIN5 (IFS=0)	70		1500	mVrms
Data setup time	tSU	DI, CL	Note 2	0.75			µs
Data hold time	tHD	DI, CL	Note 2	0.75			µs
Clock low-level time	tCL	CL	Note 2	0.75			µs
Clock high-level time	tCH	CL	Note 2	0.75			µs
CE wait time	tEL	CE, CL	Note 2	0.75			µs
CE setup time	tES	CE, CL	Note 2	0.75			µs
CE hold time	tEH	CE, CL	Note 2	0.75			µs
Data latch change time	tLC		Note 2			0.75	µs
Data output time	tDC	DO, CL	Differs depending on the value of the pull-up resistor. Note 2			0.35	µs
	tDH	DO, CE					

Note 1: Recommended crystal oscillator CI values:
CI≤120Ω (For a 4.5MHz crystal)
CI≤70Ω (For a 7.2MHz crystal)
The characteristics of the oscillation circuit depends on the printed circuit board, circuit constants, and other factors. Therefore we recommend consulting with the anufacturer of the crystal for evaluation and reliability.
Note 2: Refer to "Serial Data Timing".

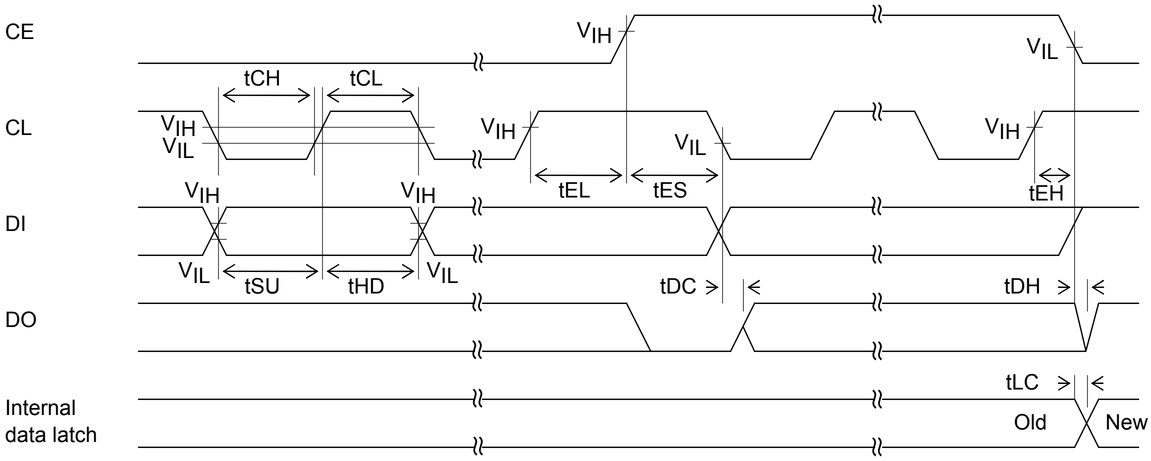
Electrical Characteristics in the Allowable Operating Ranges

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Built-in feedback resistance	Rf1	XIN			1.0		MΩ
	Rf2	FMIN			500		kΩ
	Rf3	AMIN			500		kΩ
	Rf4	IFIN			250		kΩ
Built-in pull-down resistor	Rpd1	FMIN			200		kΩ
	Rpd2	AMIN			200		kΩ
Hysteresis	VHYS	CE, CL, DI, $\overline{IO1}$, $\overline{IO2}$			$0.1V_{DD}$		V
Output high-level voltage	V_{OH}	PD	I_O=1mA	V_{DD}-0.1			V
Output low-level voltage	$V_{OL}1$	PD	I_O=1mA			1.0	V
	$V_{OL}2$	$\overline{BO1}$	I_O=0.5mA			0.5	V
			I_O=1mA			1.0	V
	$V_{OL}3$	DO	I_O=1mA			0.2	V
			I_O=5mA			1.0	V
	$V_{OL}4$	$\overline{BO2}$ to $\overline{BO4}$, $\overline{IO1}$, $\overline{IO2}$	I_O=1mA			0.2	V
			I_O=5mA			1.0	V
			I_O=8mA			1.6	V
	$V_{OL}5$	AOUT	I_O=1mA AIN=1.3V			0.5	V
Input high-level current	$I_{IH}1$	CE, CL, DI	V_I=6.5V			5.0	µA
	$I_{IH}2$	$\overline{IO1}$, $\overline{IO2}$	V_I=13V			5.0	µA
	$I_{IH}3$	XIN	$V_I=V_{DD}$	2.0		11	µA
	$I_{IH}4$	FMIN, AMIN	$V_I=V_{DD}$	4.0		22	µA
	$I_{IH}5$	IFIN	$V_I=V_{DD}$	8.0		44	µA
	$I_{IH}6$	AIN	V_I=6.5V			200	nA
Input low-level current	$I_{IL}1$	CE, CL, DI	V_I=0V			5.0	µA
	$I_{IL}2$	$\overline{IO1}$, $\overline{IO2}$	V_I=0V			5.0	µA
	$I_{IL}3$	XIN	V_I=0V	2.0		11	µA
	$I_{IL}4$	FMIN, AMIN	V_I=0V	4.0		22	µA
	$I_{IL}5$	IFIN	V_I=0V	8.0		44	µA
	$I_{IL}6$	AIN	V_I=0V			200	nA
Output off leakage current	IOFF1	$\overline{BO1}$ to $\overline{BO4}$, AOUT, $\overline{IO1}$, $\overline{IO2}$	V_O=13V			5.0	µA
	IOFF2	DO	V_O=6.5V			5.0	µA
High-level three-state off leakage current	IOFFH	PD	$V_O=V_{DD}$		0.01	200	nA
Low-level three-state off leakage current	IOFFL	PD	V_O=0V		0.01	200	nA
Input capacitance	CIN	FMIN			6		pF
Current drain	$I_{DD}1$	V_{DD}	X'tal=7.2MHz $f_{IN}2$=130MHz $V_{IN}2$=40mVrms		5	10	mA
	$I_{DD}2$	V_{DD}	PLL block stopped (PLL INHIBIT) X'tal oscillator operating (X'tal=7.2MHz)		0.5		mA
	$I_{DD}3$	V_{DD}	PLL block stopped X'tal oscillator operating			10	µA

Serial Data Timing



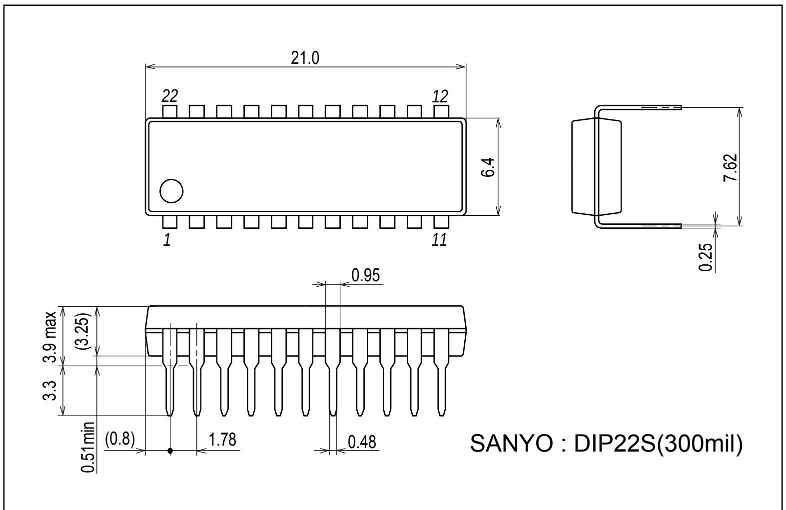
When stopped with CL low



When stopped with CL high

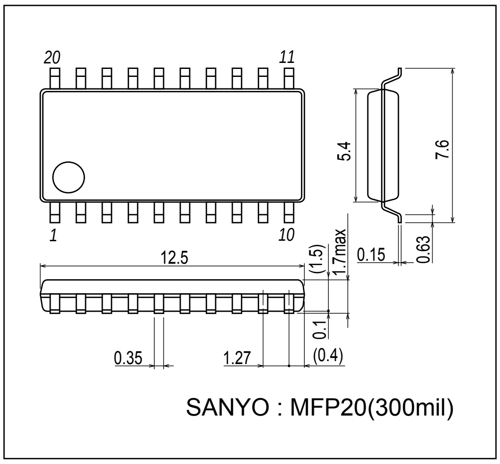
Package Dimensions

unit : mm (typ)
3059A [LC72131K]

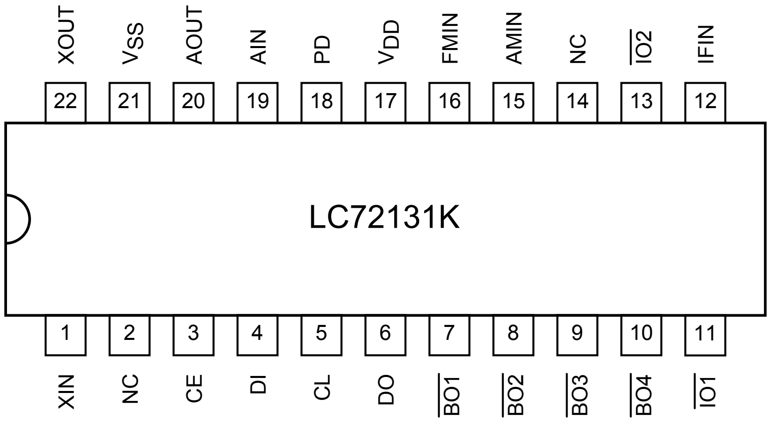


Package Dimensions

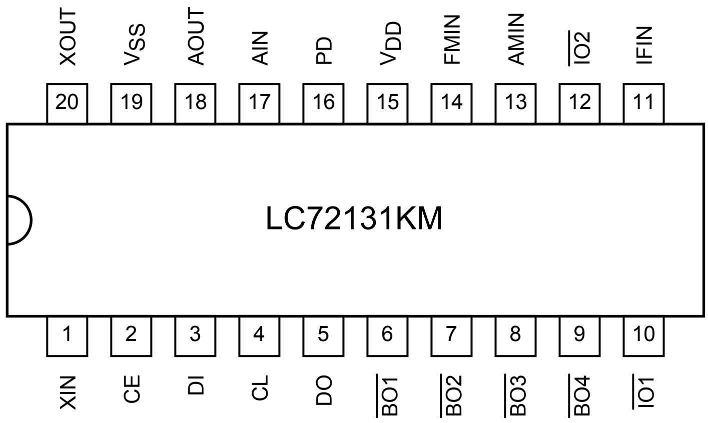
unit : mm (typ)
3036C [LC72131KM]



Pin Assignments

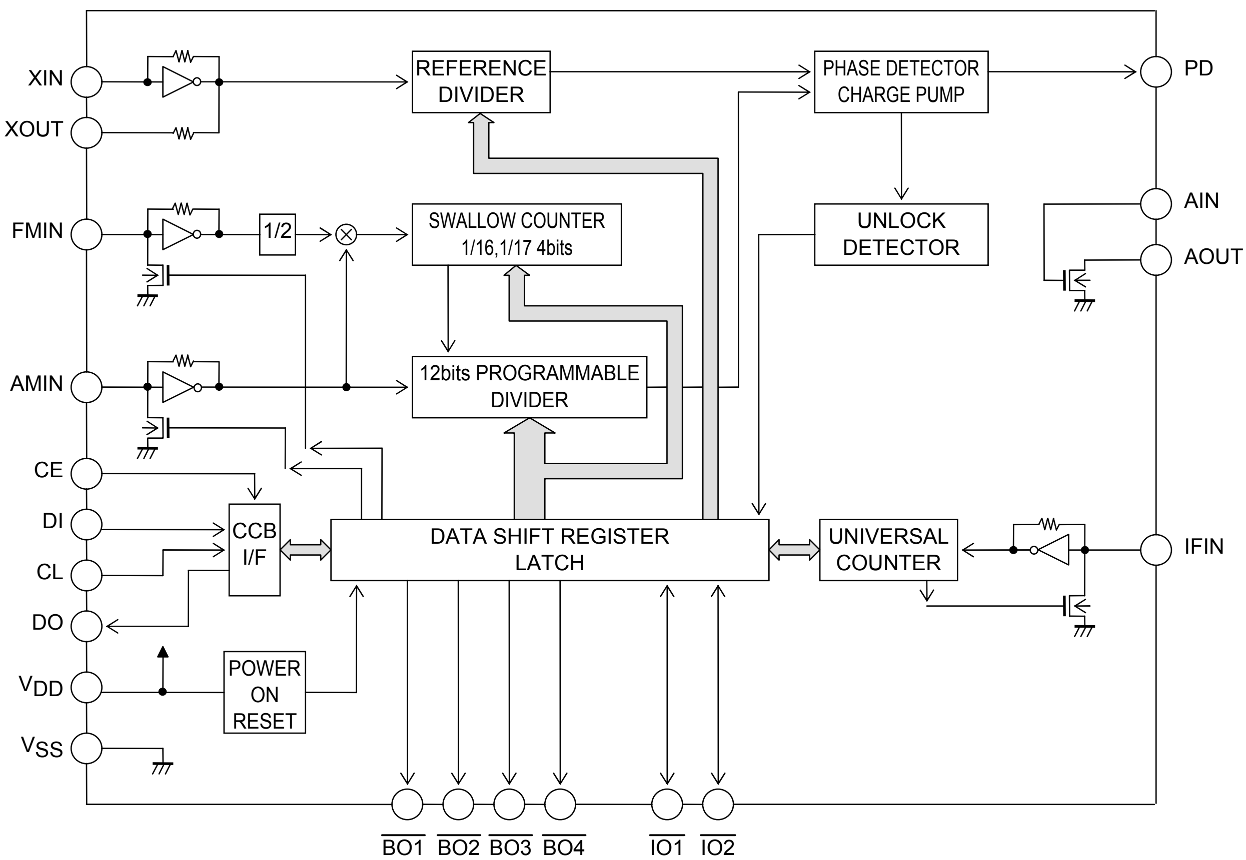


Top view

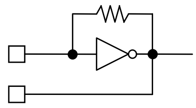
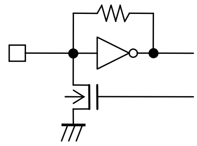
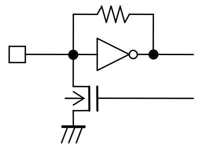
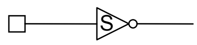
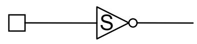
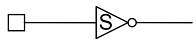
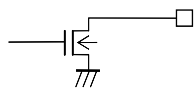
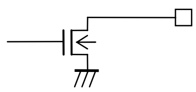
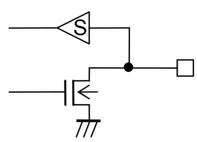


Top view

Block Diagram



Pin Functions

Symbol	Pin No.		Type	Functions	Circuit configuration
	LC72131K	LC72131KM			
XIN XOUT	1 22	1 20	X'tal OSC	Crystal resonator connection (4.5MHz/7.2MHz)	
FMIN	16	14	Local oscillator signal input	FMIN is selected when the serial data input DVS bit is set to 1. The input frequency range is from 10 to 160MHz. The input signal passes through the internal divide-by-two prescaler and is input to the swallow counter. The divisor can be in the range 272 to 65535. However, since the signal has passed through the divide-by-two prescaler, the actual divisor is twice the set value.	
AMIN	15	13	Local oscillator signal input	AMIN is selected when the serial data input DVS bit is set to 0. When the serial data input SNS bit is set to 1: • The input frequency range is 2 to 40MHz. • The signal is directly input to the swallow counter. • The divisor can be in the range 272 to 65535, and the divisor used will be the value set. When the serial data input SNS bit is set to 0: • The input frequency range is 0.5 to 10MHz. • The signal is directly input to a 12-bit programmable divider. • The divisor can be in the range 4 to 4095, and the divisor used will be the value set.	
CE	3	2	Chip enable	Set this pin high when inputting (DI) or outputting (DO) serial data.	
DI	4	3	Input data	Inputs serial data transferred from the controller to the LC72131.	
CL	5	4	Clock	Used as the synchronization clock when inputting (DI) or outputting (DO) serial data.	
DO	6	5	Output data	Outputs serial data transferred from the LC72131 to the controller. The content of the output data is determined by the serial data DOC0 to DOC2.	
V_{DD}	17	15	Power supply	The LC72131 power supply pin (V_{DD}=4.5 to 5.5V) The power on reset circuit operates when power is first applied.	-
V_{SS}	21	19	Ground	The LC72131 ground	-
$\overline{BO1}$ $\overline{BO2}$ $\overline{BO3}$ $\overline{BO4}$	7 8 9 10	6 7 8 9	Output port	Dedicated output pins The output states are determined by $\overline{BO1}$ to $\overline{BO4}$ bits in the serial data. Data: 0=open, 1=low A time base signal (8Hz) can be output from the $\overline{BO1}$ pin. (When the serial data TBC bit is set to 1.) Care is required when using the $\overline{BO1}$ pin, since it has a higher on impedance that the other output ports (pins $\overline{BO2}$ to $\overline{BO4}$).	
$\overline{IO1}$ $\overline{IO2}$	11 13	10 12	I/O port	I/O dual-use pins The direction (input or output) is determined by bits IOC1 and IOC2 in the serial data. Data: 0=input port, 1=output port When specified for use as input ports: The state of the input pin is transmitted to the controller over the DO pin. Input state: low=0 data value high=1 data value When specified for use as output ports: The output states are determined by the IO1 and IO2 bits in the serial data. Data: 0=open, 1=low These pins function as input pins following a power on reset.	

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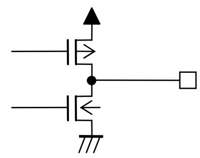
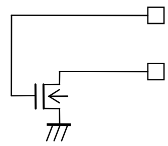
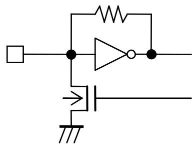
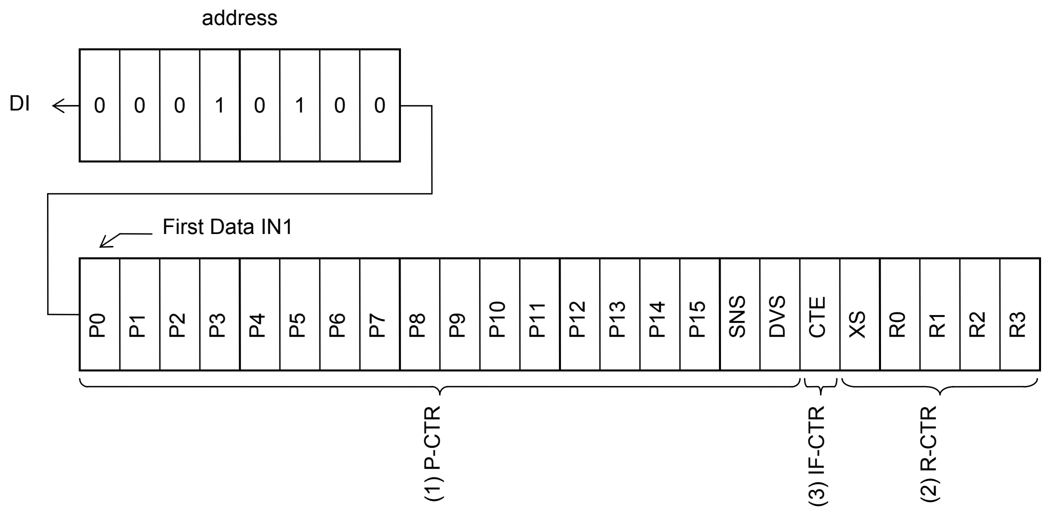
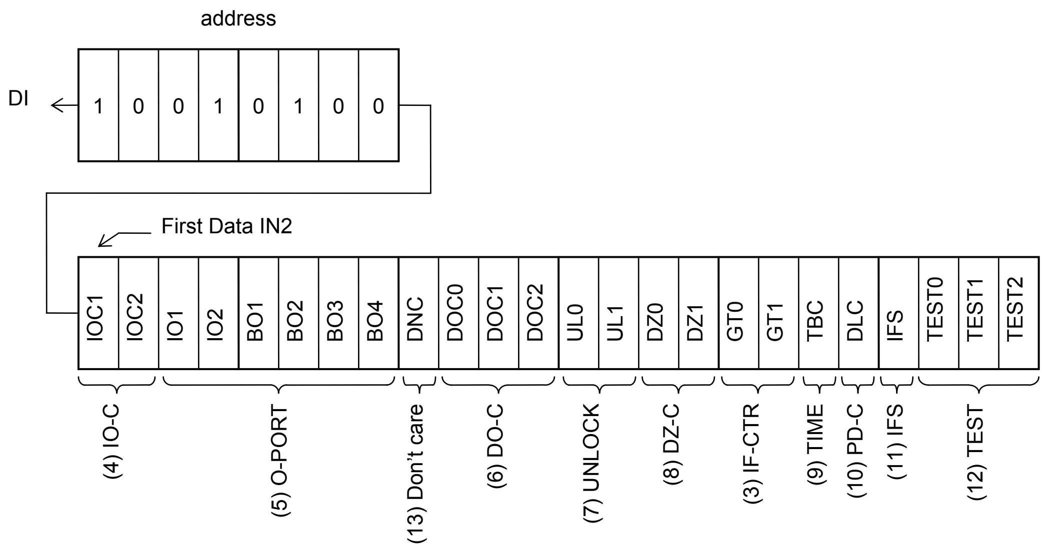
Symbol	Pin No. LC72131K	Pin No. LC72131KM	Type	Functions	Circuit configuration
PD	18	16	Charge pump output	PLL charge pump output When the frequency generated by dividing the local oscillator frequency by N is higher than the reference frequency, a high level is output from the PD pin. Similarly, when that frequency is lower, a low level is output. The PD pin goes to the high impedance state when the frequencies match.	
AIN AOUT	19 20	17 18	LPF amplifier transistors	The n-channel MOS transistor used for the PLL active low-pass filter.	
IFIN	12	11	IF counter	Accepts an input in the frequency range 0.4 to 12MHz. The input signal is directly transmitted to the IF counter. The result is output starting the MSB of the IF counter using the DO pin. Four measurement periods are supported: 4, 8, 32, and 64ms.	

DI Control Data (Serial Data Input) Structure

[1] IN1 mode



[2] IN2 mode



Control Data Functions

<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data
P0 to P15</td><td>Data that sets the divisor of the programmable divider.
A binary value in which P15 is the MSB. The LSB changes depending on DVS and SNS. (*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>Divisor setting (N)</th><th>Actual divisor</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the value of the setting</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>The value of the setting</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>The value of the setting</td></tr>
</table>
Note: P0 to P3 are ignored when P4 is the LSB.</td><td></td></tr>
<tr><td></td><td>DVS, SNS</td><td>Selects the signal input pin (AMIN or FMIN) for the programmable divider, switches the input frequency range. (*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input pin</th><th>Input frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
Note: See the "Programmable Divider Structure" item for more information.</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data
R0 to R3</td><td>Reference frequency (fref) selection data.
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>9</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>* PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>* PLL INHIBIT</td></tr>
</table>
Note *: PLL INHIBIT
The programmable divider block and the IF counter block are stopped, the FMIN, AMIN, and IFIN pins are set to the pull-down state (ground), and the charge pump goes to the high impedance state.</td><td></td></tr>
<tr><td></td><td>XS</td><td>Crystal resonator selection
XS=0: 4.5MHz
XS=1: 7.2MHz
The 7.2MHz frequency is selected after the power-on reset.</td><td></td></tr>
<tr><td>(3)</td><td>IF counter control data
CTE
GT0, GT1</td><td>IF counter measurement start data
CTE=1: Counter start
=0: Counter reset
Determines the IF counter measurement period.
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th><th>Wait time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td><td>3 to 4</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>32</td><td>7 to 8</td></tr>
<tr><td>1</td><td>1</td><td>64</td><td>7 to 8</td></tr>
</table>
Note: See the "IF Counter Structure" item for more information.</td><td>IFS</td></tr>
</table>

Continued on next page.

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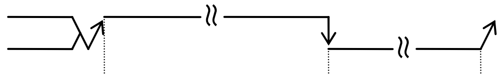
<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(4)</td><td>I/O port specification data
IOC1, IOC2</td><td>Specifies the I/O direction for the bidirectional pins $\overline{IO1}$ and $\overline{IO2}$.
Data: 0=input mode, 1=output mode</td><td></td></tr>
<tr><td>(5)</td><td>Output port data
BO1 to BO4
IO1, IO2</td><td>Data that determines the output from the $\overline{BO1}$ to $\overline{BO4}$, $\overline{IO1}$ and $\overline{IO2}$ output ports
Data: 0=open, 1=low
The data=0 (open) state is selected after the power-on reset.</td><td>IOC1
IOC2</td></tr>
<tr><td>(6)</td><td>DO pin control data
DOC0
DOC1
DOC2</td><td>Data that determines the DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>Do pin state</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when the unlock state is detected</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC *1</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>The $\overline{IO1}$ pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The $\overline{IO2}$ pin state *2</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
The open state is selected after the power-on reset.
Note: 1. end-UC: Check for IF counter measurement completion
DO pin

(1) Count start (2) Count end (3)CE: High
(1) When end-UC is set and the IF counter is started (i.e., when CTE is changed from zero to one), the DO pin automatically goes to the open state.
(2) When the IF counter measurement completes, the DO pin goes low to indicate the measurement completion state.
(3) Depending on serial data I/O (CE: high) the DO pin goes to the open state.
Note: 2. Goes to the open state if the I/O pin is specified to be an output port.
Caution: The state of the DO pin during a data input period (an IN1 or IN2 mode period with CE high) will be open, regardless of the state of the DO control data (DOC0 to DOC2). Also, the DO pin during a data output period (an OUT mode period with CE high) will output the contents of the internal DO serial data in synchronization with the CL pin signal, regardless of the state of the DO control data (DOC0 to DOC2).</td><td>UL0, UL1
CTE

IOC1
IOC2</td></tr>
<tr><td>(7)</td><td>Unlock detection data
UL0, UL1</td><td>Selects the phase error (φE) detection width for checking PLL lock.
A phase error in excess of the specified detection width is seen as an unlocked state.
<table>
<tr><th>UL1</th><th>UL0</th><th>φE detection width</th><th>Detector output</th></tr>
<tr><td>0</td><td>0</td><td>stopped</td><td>Open</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>φE is output directry</td></tr>
<tr><td>1</td><td>0</td><td>±0.55μs</td><td>φE is extended by 1 to 2ms</td></tr>
<tr><td>1</td><td>1</td><td>±1.11</td><td>↑</td></tr>
</table>
Note: In the unlocked state the DO pin goes low and the UL bit in the serial data becomes zero.</td><td>DOC0
DOC1
DOC2</td></tr>
</table>

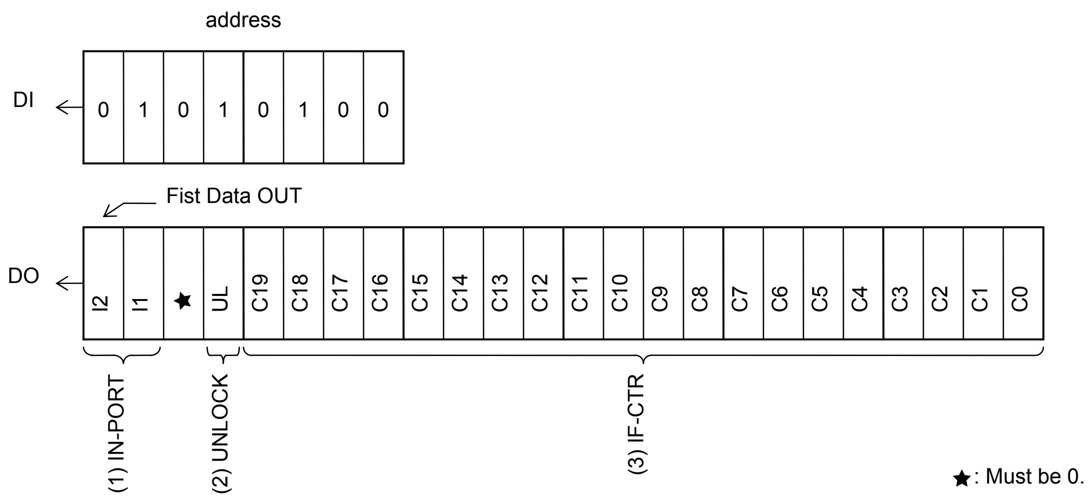
Continued on next page.

Continued from preceding page.

<table>
<tr><th>No.</th><th>Control block/data</th><th>Functions</th><th>Related data</th></tr>
<tr><td>(8)</td><td>Phase comparator control data
DZ0, DZ1</td><td>• Controls the phase comparator dead zone.
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr>
<tr><td>0</td><td>0</td><td>DZA</td></tr>
<tr><td>0</td><td>1</td><td>DZB</td></tr>
<tr><td>1</td><td>0</td><td>DZC</td></tr>
<tr><td>1</td><td>1</td><td>DZD</td></tr>
</table>
Dead zone width: DZA<DZB<DZC<DZD</td><td></td></tr>
<tr><td>(9)</td><td>Clock time base
TBC</td><td>Setting TBC to one causes an 8Hz, 40% duty clock time base signal to be output from the $\overline{\text{BO1}}$ pin. (BO1 data is invalid in this mode.)</td><td>BO1</td></tr>
<tr><td>(10)</td><td>Charge pump control data
DLC</td><td>Forcibly controls the charge pump output.
<table>
<tr><th>DLC</th><th>Charge pump output</th></tr>
<tr><td>0</td><td>Normal operation</td></tr>
<tr><td>1</td><td>Forced low</td></tr>
</table>
Note: If deadlock occurs due to the VCO control voltage (Vtune) going to zero and the VCO oscillator stopping, deadlock can be cleared by forcing the charge pump output to low and setting Vtune to V_{CC}. (This is the deadlock clearing circuit.)</td><td></td></tr>
<tr><td>(11)</td><td>IF counter control data
IFS</td><td>This data must be set 1 in normal mode.
IFS Though if this value is set to zero, the system enters input sensitivity degradation mode, and the sensitivity is reduced to 10 to 30mVrms.
* See the “IF Counter Operation” item for details.</td><td></td></tr>
<tr><td>(12)</td><td>LSI test data
TEST0 to 2</td><td>LSI test data
TEST0
TEST1 These values must all be set to 0.
TEST2
These test data are set to 0 automatically after the power-on reset.</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>Don’t care. This data must be set to 0.</td><td></td></tr>
</table>

DO Control Data (Serial Data Output) Structure

[3] OUT Mode



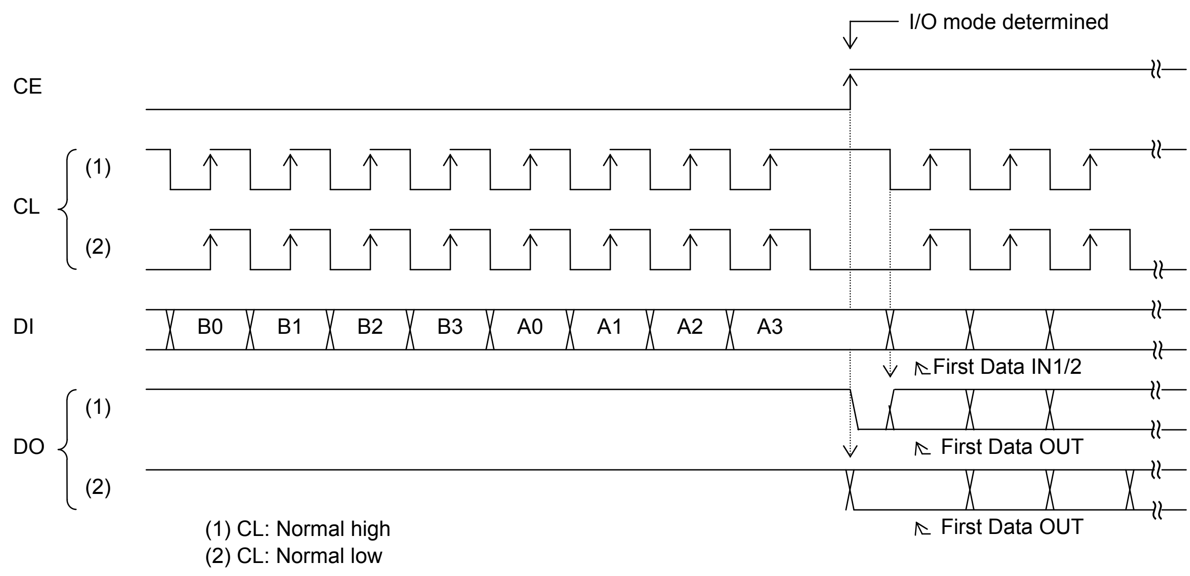
Control Data Functions

No.	Control block/data	Functions	Related data
(1)	I/O port data I2, I1	Latched from the pin states of the $\overline{IO1}$ and $\overline{IO2}$ I/O ports. These values follow the pin states regardless of the input or output setting. I1 ← $\overline{IO1}$ pin state High: 1 I2 ← $\overline{IO2}$ pin state Low: 0	IOC1 IOC2
(2)	PLL unlock data UL	Latched from the state of the unlock detection circuit. UL ← 0: Unlocked UL ← 1: Locked or detection stopped mode	UL0 UL1
(3)	IF counter binary counter C19 to C0	Latched from the value of the IF counter (20-bit binary counter). C19 ← MSB of the binary counter C0 ← LSB of the binary counter	CTE GT0 GT1

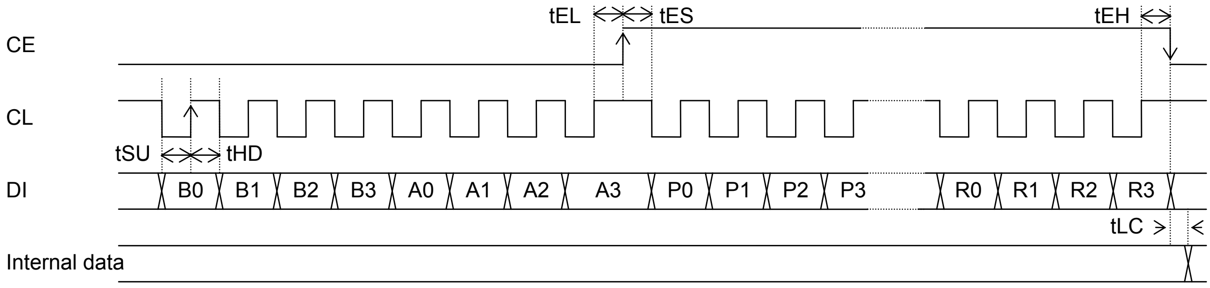
Serial Data I/O Methods

The LC72131 inputs and outputs data using the SANYO CCB (computer control bus) audio LSI serial bus format. This LSI adopts an 8-bit address format CCB.

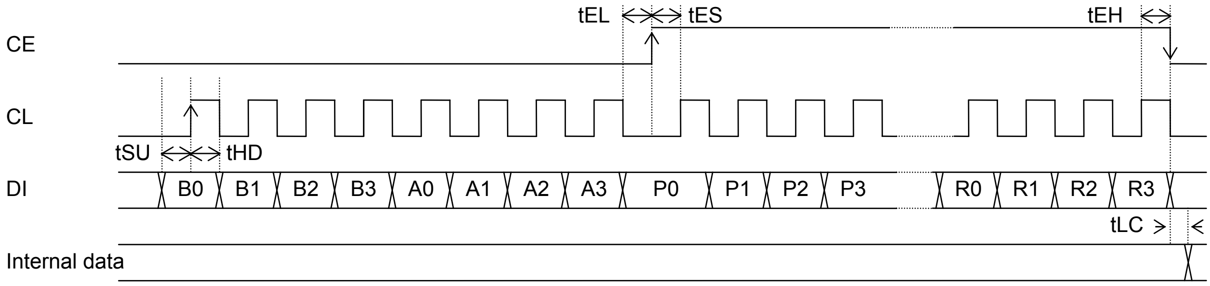
	I/O mode	Address								Function
		B0	B1	B2	B3	A0	A1	A2	A3	
[1]	IN1 (82)	0	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
[2]	IN2 (92)	1	0	0	1	0	1	0	0	• Control data input mode (serial data input) • 24 data bits are input. • See the “DI Control Data (serial data input) Structure” item for details on the meaning of the input data.
[3]	OUT (A2)	0	1	0	1	0	1	0	0	• Data output mode (serial data output) • The number of bits output is equal to the number of clock cycles. • See the “DO Control Data (serial data output) Structure” item for details on the meaning of the output data.



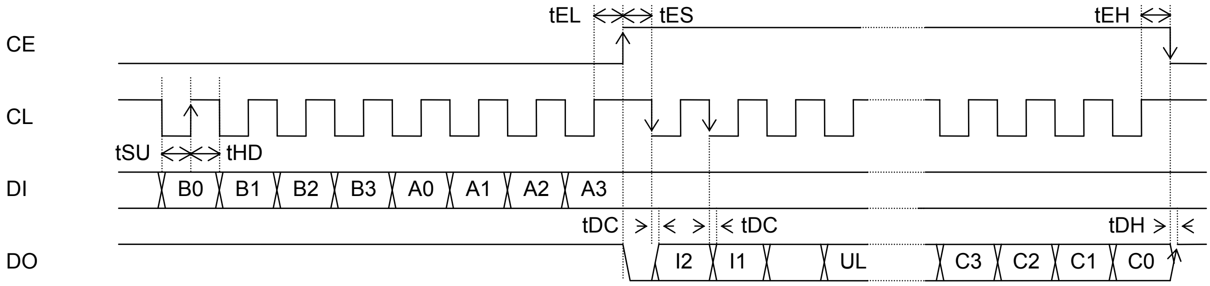
1. Serial Data Input (IN1/IN2) tSU, tHD, tES, tEH≥0.75µs tLC<0.75µs
   (1) CL: Normal high



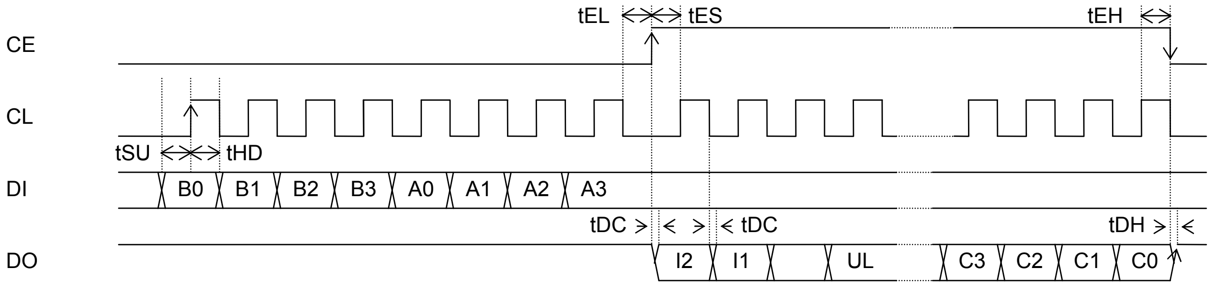
   (2) CL: Normal low



2. Serial Data Output (OUT) tSU, tHD, tEL, tES, tEH≥0.75µs tDC, tDH<0.35µs
   (1) CL: Normal high

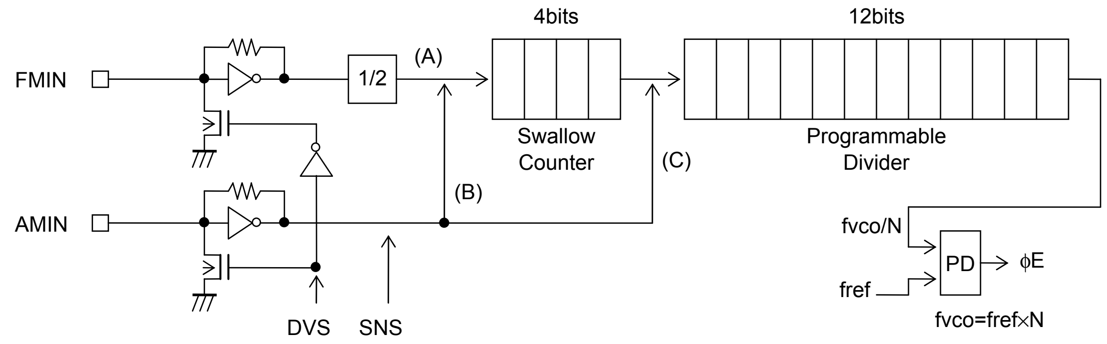


   (2) CL: Normal low



Note: Since the DO pin is an N-channel open-drain pin, the time for the data to change (tDC and tDH) will differ depending on the value of the pull-up resistor and printed circuit board capacitance.

Programmable Divider Structure



	DVS	SNS	Input pin	Set divisor	Actual divisor: N	Input frequency range
(A)	1	*	FMIN	272 to 65535	Twice the set value	10 to 160MHz
(B)	1	1	AMIN	272 to 65535	The set value	2 to 40MHz
(C)	0	0	AMIN	4 to 4095	The set value	0.5 to 10MHz

*: Don't care

Programmable Divider Calculation Examples

(1) FM, 50kHz steps (DVS=1, SNS=*: FMIN selected)
FM RF=90.0MHz (IF=+10.7MHz)
FM VCO=100.7MHz
PLL fref=25kHz (R0 to R1=1, R2 to R3=0)
100.7MHz (FMVCO)÷25kHz (fref) ÷2 (FMIN: divide-by-two prescaler) =2014→07DE (HEX)

E				D				7				0											
0	1	1	1	1	0	1	1	1	1	1	0	0	0	0	0	*	1			1	1	0	0
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

(2) SW 5kHz steps (DVS=0, SNS=1: AMIN high-speed side selected)
SW RF=21.75MHz (IF=+450kHz)
SW VCO=22.20MHz
PLL fref=5kHz (R0=R2=0, R1=R3=1)
22.2MHz (SW VCO) ÷5kHz (fref) =4440→1158 (HEX)

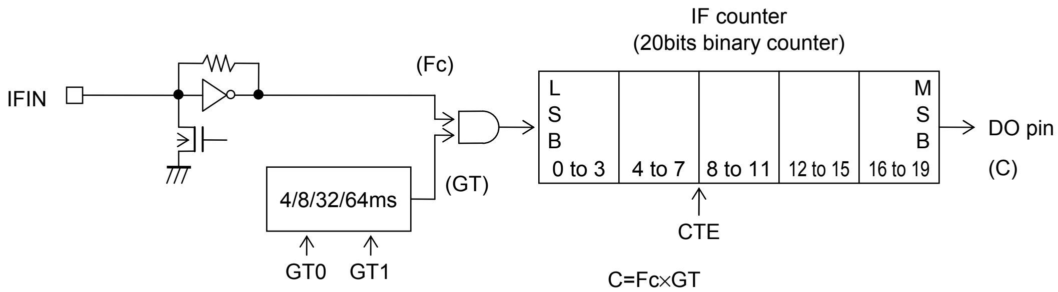
8				5				1				1											
0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1	0			0	1	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

(3) MW 10kHz steps (DVS=0, SNS=0: AMIN low-speed side selected)
MW RF=1000kHz (IF=+450kHz)
MW VCO=1450kHz
PLL fref=10kHz (R0 to R2=0, R3=1)
1450kHz (MW VCO) ÷10kHz (fref)=145→091 (HEX)

				1				9				0											
*	*	*	*	1	0	0	0	1	0	0	1	0	0	0	0	0	0			0	0	0	1
P0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	SNS	DVS	CTE	XS	R0	R1	R2	R3

IF Counter Structure

The LC72131K/KM IF counter is a 20-bit binary counter. The result, i.e., the counter's msb, can be read serially from the DO pin.



GT1	GT0	Measurement time	
		Measurement time (GT) (ms)	Wait time (twu) (ms)
0	0	4	3 to 4
0	1	8	3 to 4
1	0	32	7 to 8
1	1	64	7 to 8

The IF frequency (Fc) is measured by determining how many pulses were input to an IF counter in a specified measurement period, GT.

$$Fc=\frac{C}{GT}\ (C=Fc\times GT)\quad \text{C: Count value (number of pulses)}$$

IF Counter Frequency Calculation Examples

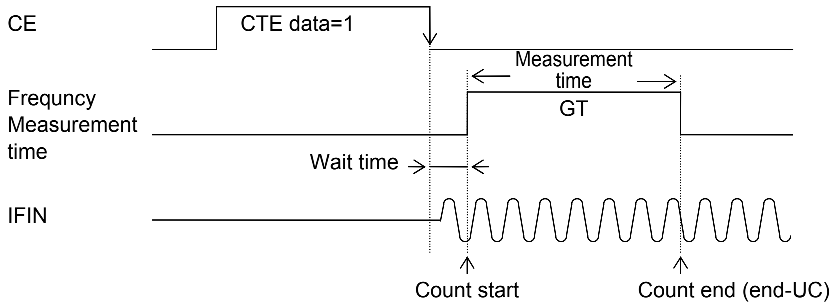
(1) When the measurement period (GT) is 32ms, the count (C) is 53980 hexadecimal (342400 decimal):
IF frequency (Fc) =342400÷32ms=10.7MHz

				5				3				9				8				0			
				0	1	0	1	0	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0
I2	I1		UL	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

(2) When the measurement period (GT) is 8ms, the count (C) is E10 hexadecimal (3600 decimal):
IF frequency (Fc) =3600÷8ms=450kHz

				0				0				E				1				0			
				0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0
I2	I1		UL	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

IF Counter Operation



Before starting the IF count, the IF counter must be reset in advance by setting CTE in the serial data to 0.
The IF count is started by changing the CTE bit in the serial data from 0 to 1. The serial data is latched by the LC72131 when the CE pin is dropped from high to low. The IF signal must be supplied to the IFIN pin in the period between the point the CE pin goes low and the end of the wait time at the latest. Next, the value of the IF counter at the end of the measurement period must be read out during the period that CTE is 1. This is because the IF counter is reset when CTE is set to 0.

Note: When operating the IF counter, the control microprocessor must first check the state of the IF-IC SD (station detect) signal and only after determining that the SD signal is present turn on IF buffer output and execute an IF count operation. Autosearch techniques that use only the IF counter are not recommended, since it is possible for IF buffer leakage output to cause incorrect stops at points where there is no station.

IFIN minimum input sensitivity standard f [MHz]

IFS	0.4≤f<0.5	0.5≤f<8	8≤f≤12
1: Normal mode	40mVrms (0.1 to 3mVrms)	40mVrms	40mVrms (1 to 10mVrms)
0: Degradation mode	70mVrms (10 to 15mVrms)	70mVrms	70mVrms (30 to 40mVrms)

Note: Values in parentheses are actual performance values presented as reference data.

Unlock Detection Timing

Unlock Detection Determination Timing

Unlocked state detection is performed in the reference frequency (fref) period (interval). Therefore, in principle, unlock determination requires a time longer than the period of the reference frequency. However, immediately after changing the divisor N (frequency) unlock detection must be performed after waiting at least two periods of the reference frequency.

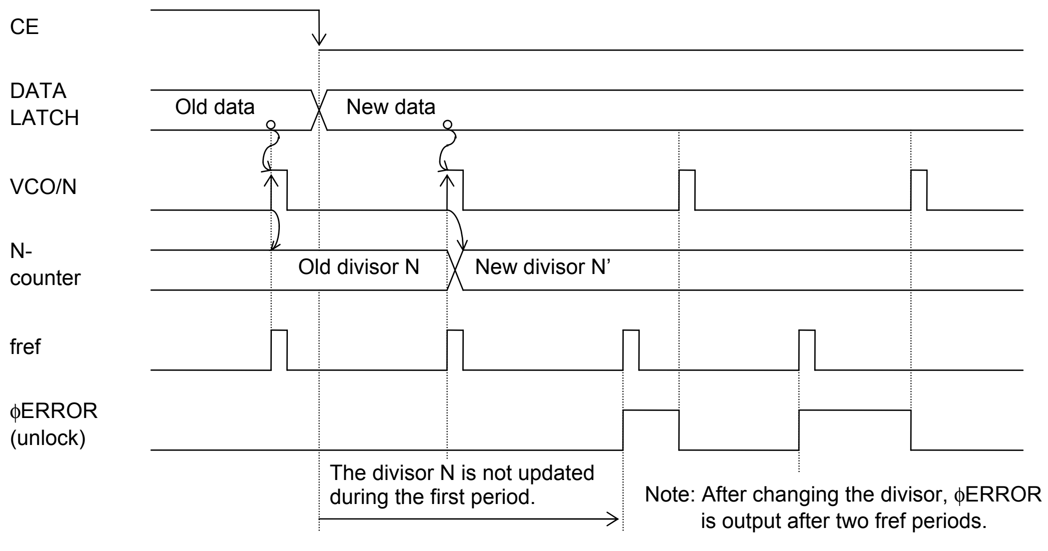


Figure 1 Unlocked State Detection Timing

For example, if fref is 1kHz, i.e., the period is 1ms, after changing the divisor N, the system must wait at least 2ms before checking for the unlocked state.

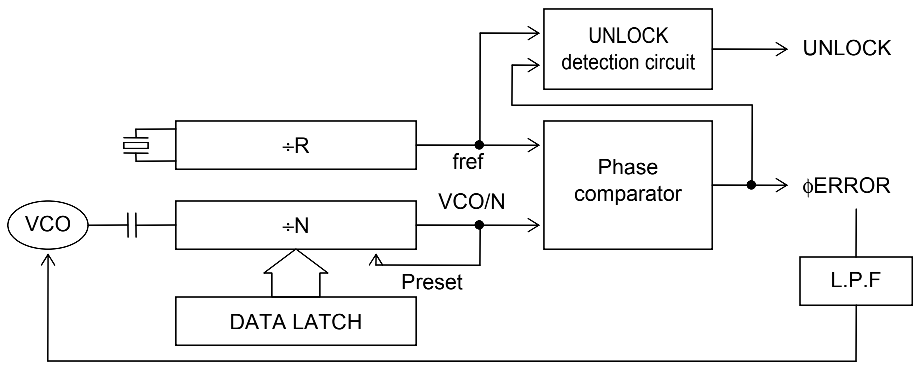


Figure 2 Circuit Structure

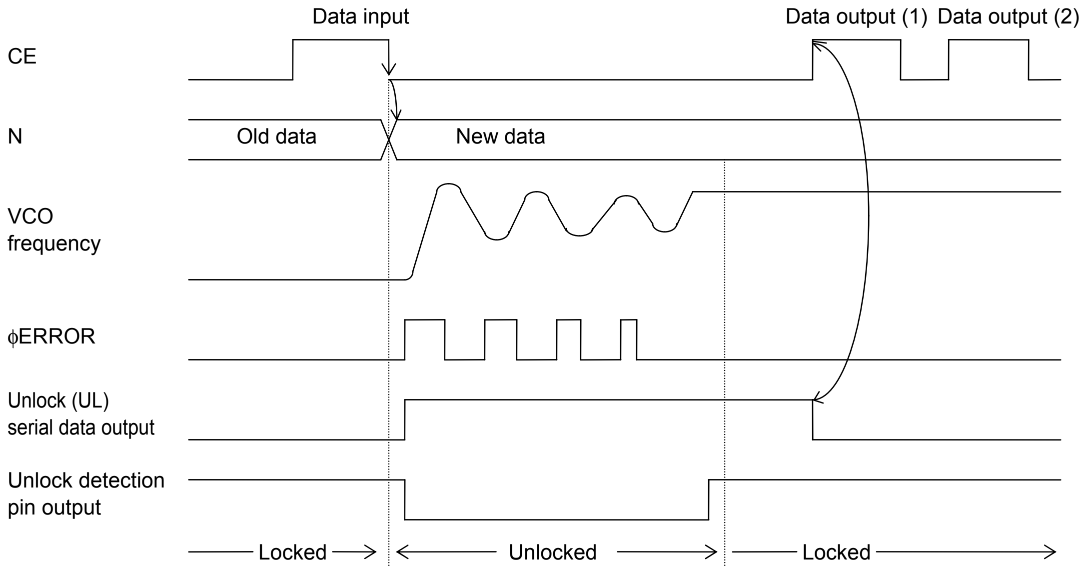


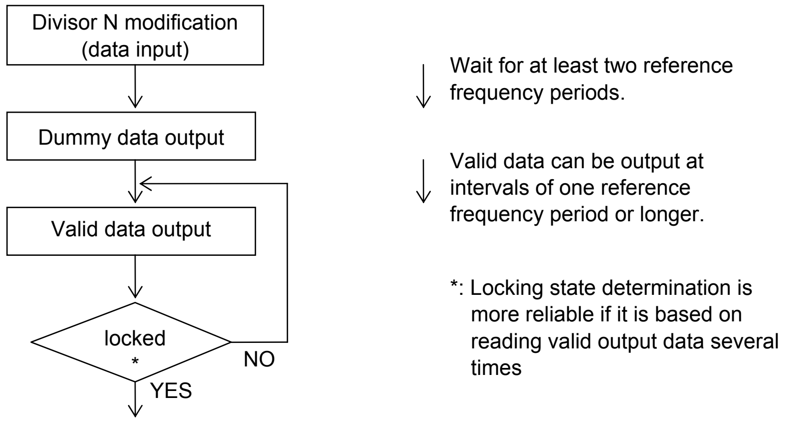
Figure 3

Unlocked State Data Output Using Serial Data Output

In the LC72131, once an unlocked state occurs, the unlocked state serial data (UL) will not be reset until a data input (or output) operation is performed. At the data output (1) point in Figure 3, although the VCO frequency has stabilized (locked), since no data output has been performed since the divisor N was changed the unlocked state data remains in the unlocked state. As a result, even though the frequency has stabilized (locked), the system remains (from the standpoint of the data) in the unlocked state.

Therefore, the unlocked state data acquired at data output (1), which occurs immediately after the divisor N was changed, should be treated as a dummy data output and ignored. The second data output (data output (2)) and following outputs are valid data.

<Locked State Determination Flowchart Example>

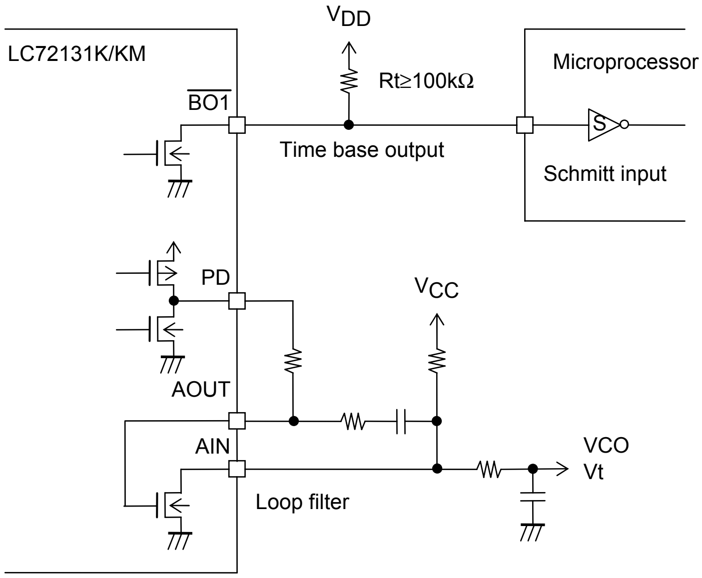


Directly Outputting Unlocked State Data from the DO Pin (Set by the DO pin control data)

Since the unlocked state (high=locked, low=unlocked) is output directly from the DO pin, the dummy data processing described in section 3 above is not required. After changing the divisor N, the locking state can be checked after waiting at least two reference frequency periods.

Clock Time Base Usage Notes

The pull-up resistor used on the clock time base output pin ($\overline{\text{BO1}}$) should be at least 100kΩ. This is to prevent degrading the VCO C/N characteristics when a loop filter is formed using the built-in low-pass filter transistor. Since the clock time base output pin and the low-pass filter have a common ground internal to the IC, it is necessary to minimize the time base output pin current fluctuations and to suppress their influence on the low-pass filter. Also, to prevent chattering we recommend using a Schmitt input at the controller (microprocessor) that receives this signal.



Other Items

[1] Notes on the Phase Comparator Dead Zone

DZ1	DZ0	Dead zone mode	Charge pump	Dead zone
0	0	DZA	ON/ON	- -0s
0	1	DZB	ON/ON	-0s
1	0	DZC	OFF/OFF	+0s
1	1	DZD	OFF/OFF	++0s

Since correction pulses are output from the charge pump even if the PLL is locked when the charge pump is in the ON/ON state, the loop can easily become unstable. This point requires special care when designing application circuits.

The following problems may occur in the ON/ON state.

(1) Side band generation due to reference frequency leakage

(2) Side band generation due to both the correction pulse envelope and low frequency leakage

Schemes in which a dead zone is present (OFF/OFF) have good loop stability, but have the problem that acquiring a high C/N ratio can be difficult. On the other hand, although it is easy to acquire a high C/N ratio with schemes in which there is no dead zone, it is difficult to achieve high loop stability. Therefore, it can be effective to select DZA or DZB, which have no dead zone, in applications which require an FM S/N ratio in excess of 90 to 100dB, or in which an increased AM stereo pilot margin is desired. On the other hand, we recommend selecting DZC or DZD, which provide a dead zone, for applications which do not require such a high FM signal-to-noise ratio and in which either AM stereo is not used or an adequate AM stereo pilot margin can be achieved.

Dead Zone

The phase comparator compares fp to a reference frequency (fr) as shown in Figure 1. Although the characteristics of this circuit (see Figure 2) are such that the output voltage is proportional to the phase difference ø (line A), a region (the dead zone) in which it is not possible to compare small phase differences occurs in actual ICs due to internal circuit delays and other factors (line B). A dead zone as small as possible is desirable for products that must provide a high S/N ratio.

However, since a larger dead zone makes this circuit easier to use, a larger dead zone is appropriate for popularlypriced products. This is because it is possible for RF signals to leak from the mixer to the VCO and modulate the VCO in popularly-priced products in the presence of strong RF inputs. When the dead zone is narrow, the circuit outputs correction pulses and this output can further modulate the VCO and generate beat frequencies with the RF signal.

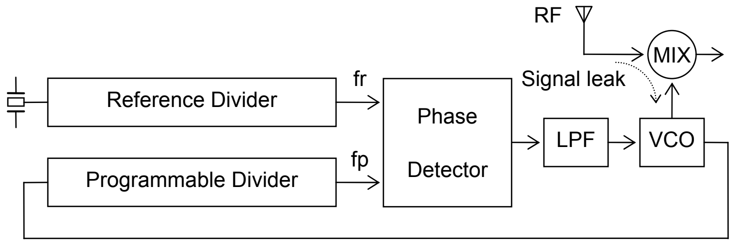


Figure 1

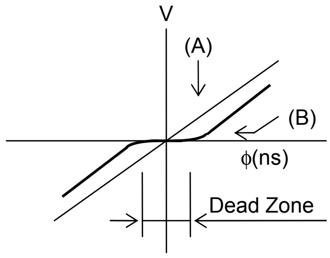


Figure 2

[2] Notes on the FMIN, AMIN, and IFIN Pins

Coupling capacitors must be placed as close as possible to their respective pin. A capacitance of about 100pF is desirable. In particular, if a capacitance of 1000pF or over is used for the IF pin, the time to reach the bias level will increase and incorrect counting may occur due to the relationship with the wait time.

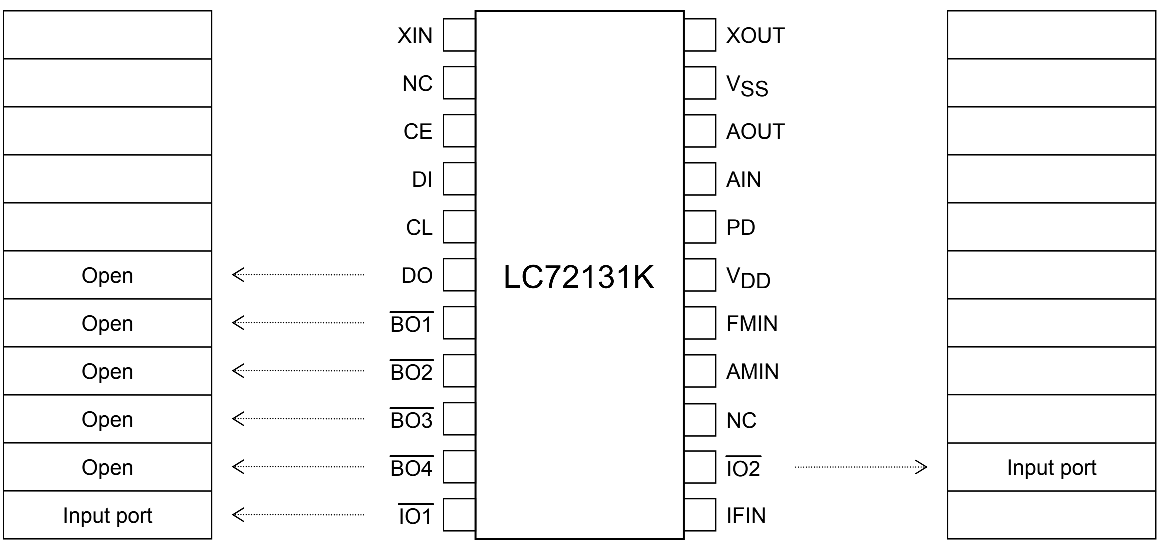
[3] Notes on IF Counting→SD must be used in conjunction with the IF counting time

When using IF counting, always implement IF counting by having the microprocessor determine the presence of the IF-IC SD (station detect) signal and turn on the IF counter buffer only if the SD signal is present. Schemes in which auto-searches are performed with only IF counting are not recommended, since they can cause false detection where there is no signal due to overflow from the IF counter buffer.

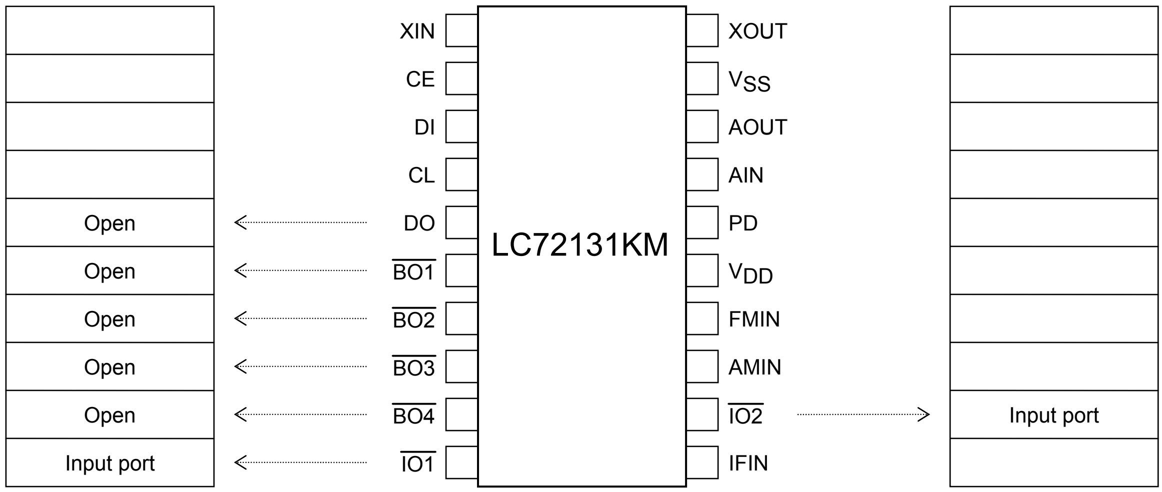
[4] DO Pin Usage Techniques

In addition to data output mode times, the DO pin can also be used to check for IF counter count completion and for unlock detection output. Also, an input pin state can be output unchanged through the DO pin and input to the controller.

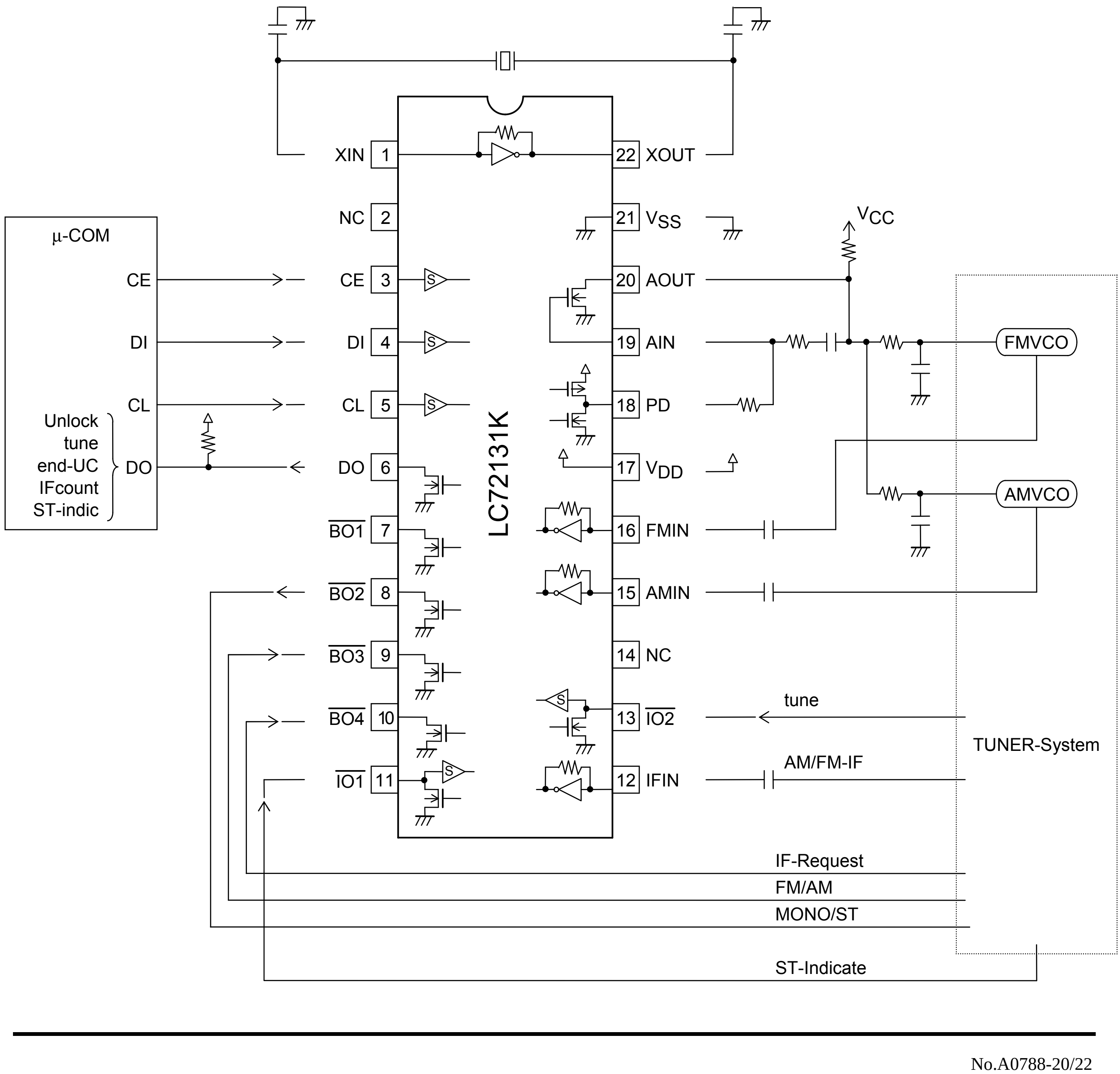
Pin States After the Power ON Reset [LC72131K]



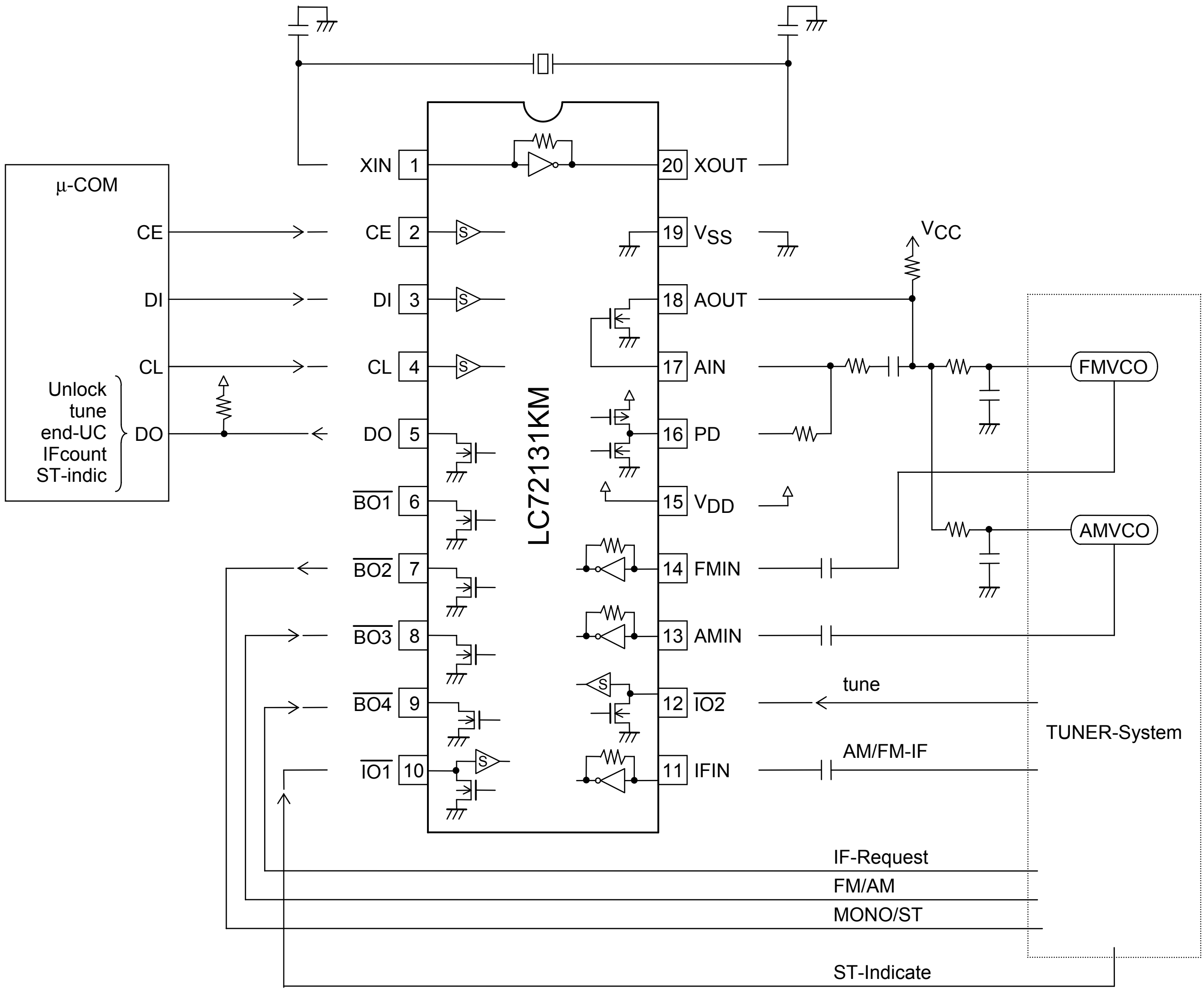
Pin States After the Power ON Reset [LC72131KM]



Application System Example [LC72131K]



Application System Example [LC72131KM]



This catalog provides information as of May, 2009. Specifications and information herein are subject to change without notice.