**Structure** Silicon monolithic Integrated circuit
**Product** Clock Generator With Built-in VCXO

**Type** **BU3058FV**

**Feature** To generate clocks for the Digital-TV.
Clock signals are generated by connecting crystal oscillator.
Built-in VCXO has the variable width of Typ±105ppm.

## ○Absolute Maximum Ratings (Ta=25℃)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | -0.3 ～4.0 | V |
| Input Voltage | VIN | -0.3～VDD+0.3 | V |
| Storage Temperature range | Tstg | -55～125 | ℃ |
| Power dissipation | PD | 450※1 | mW |

※1 A measure value at mounting on 70x70x1.6mm glass epoxy substrate.
In the case of exceeding Ta=25°C, 4.5mW should be reduced per 1°C.
※ The radiation-resistance design is not carried out.
※ Operation is not guaranteed.

## ○Operating Conditions

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply voltage | VDD | 3.135 ～ 3.465 | V |
| Input ”H” Voltage | VIH | 0.8VDD ～ VDD | V |
| Input ”L” Voltage | VIL | 0.0 ～ 0.2VDD | V |
| Operating Temperature | topr | -10 ～ 75 | ℃ |
| Frequency Control Voltage | Vc | 0.0 ～ VDD | V |

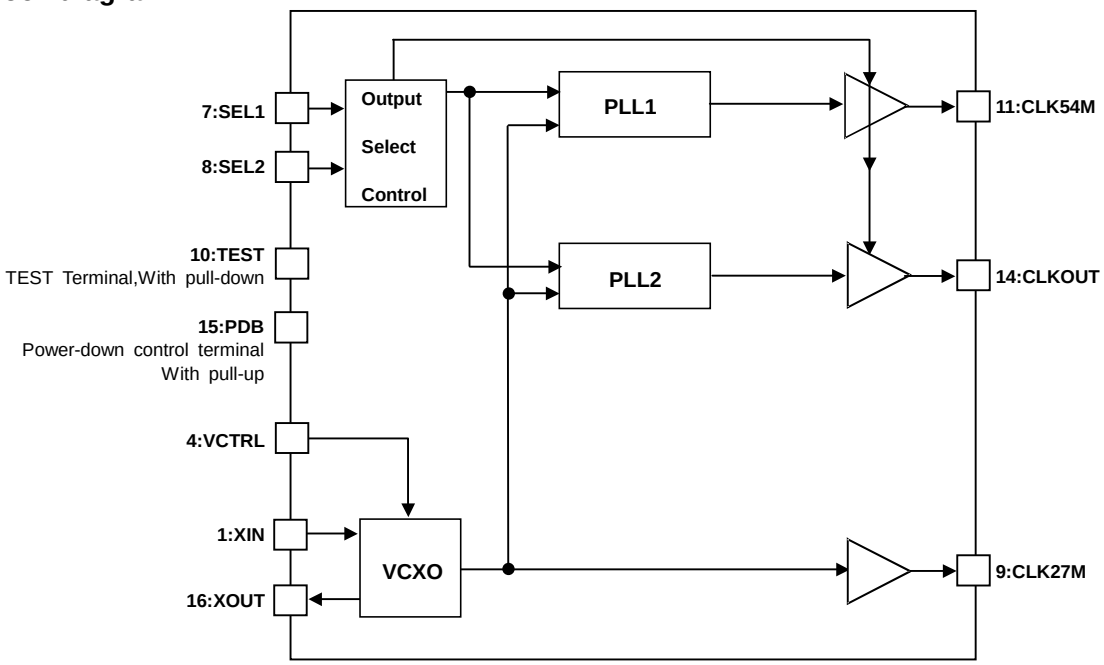
## ○Electrical Characteristics

**（VDD=3.3V, Ta=25°C, Crystal Frequency=27.000000MHz, at No Load, unless otherwise specified）**

| Parameter | Symbol | Limit | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output H voltage | VOH | VDD-0.4 | – | – | V | IOH=4.0mA |
| Output L voltage | VOL | – | – | 0.4 | V | IOL=4.0mA |
| Operating circuit current | IDD | – | 40.0 | 52.0 | mA | Output No Load |
| Input H current 1 | IupH | -1.5 | – | 1.5 | μA | PDB Terminal,VIH=VDD |
| Input H current 2 | IdnH | 19.0 | 69.0 | 136.5 | μA | TEST Terminal,VIH=VDD |
| Input H current 3 | IdirH | -1.5 | – | 1.5 | μA | VCTRL, SEL1, SEL2 Terminal,VIH=VDD |
| Input L current 1 | IupL | -126.0 | -53.0 | -17.0 | μA | PDB Terminal,VIL=0.0V |
| Input L current 2 | IdnL | -1.5 | – | 1.5 | μA | TEST Terminal,VIL=0.0V |
| Input L current 3 | IdirL | -1.5 | – | 1.5 | μA | VCTRL, SEL1, SEL2 Terminal,VIL=0.0V |
| Crystal Pullability | fp | ±80 | ±105 | ±130 | ppm | 0≦VCTRL≦VDD ※ |

※ This is a guarantee with only IC.
The arrangement with a crystal maker is required separately about crystal variation.

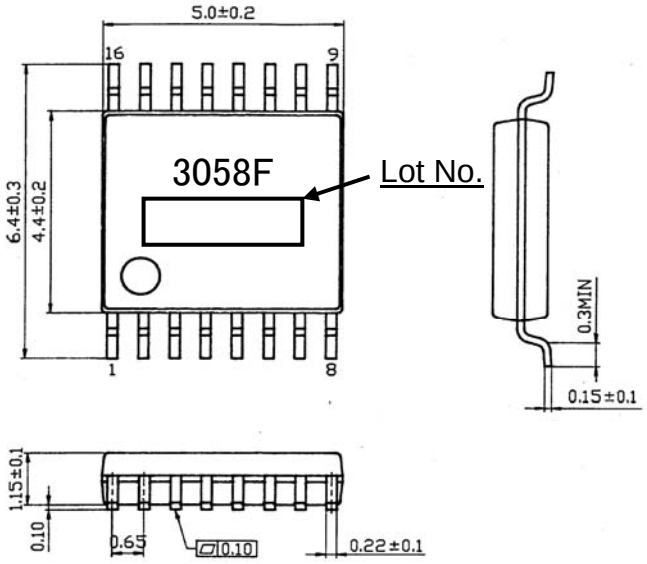
## ○Block diagram




## ○Table of Output Frequency（Crystal Frequency=27.000000MHz）

| mode No. | SEL1 | SEL2 | 14pin | 11pin | 9pin |
|---|---|---|---|---|---|
| | | | CLKOUT | CLK54M | CLK27M |
| ① | L | L | 66.000000MHz | 54.000000MHz | 27.000000MHz |
| ② | L | H | 74.250000MHz | 54.000000MHz | 27.000000MHz |
| ③ | H | L | 77.000000MHz | 54.000000MHz | 27.000000MHz |
| ④ | H | H | 82.000000MHz | 54.000000MHz | 27.000000MHz |

## ○Package Outline, Appearance of Marker




SSOP-B16

(UNIT : mm)

## ○Pin Function

| PIN No. | PIN Name | Function |
|---|---|---|
| 1 | XIN | Crystal Input terminal |
| 2 | AVDD1 | Power supply for VCXO |
| 3 | AVSS1 | GND for VCXO |
| 4 | VCTRL | VCXO control input terminal |
| 5 | AVDD2 | Power supply for PLL-Analog |
| 6 | AVSS2 | GND for PLL-Analog |
| 7 | SEL1 | CLKOUT output control terminal1 |
| 8 | SEL2 | CLKOUT output control terminal2 |
| 9 | CLK27M | 27.000000MHz Output |
| 10 | TEST | Test terminal with pull-down |
| 11 | CLK54M | 54.000000MHz Output |
| 12 | VSS | GND for PLL-Digital |
| 13 | VDD | Power supply for PLL-Digital |
| 14 | CLKOUT | 66.000000MHz / 74.250000MHz / 77.000000MHz / 82.000000MHz Output |
| 15 | PDB | Power-down control terminal,with pull-up |
| 16 | XOUT | Crystal Output terminal |

●Cautions on use（BU3058FV）

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)

Mount 0.1μF capacitors in the vicinity of the IC PINs between 2PIN (AVDD1), 3PIN (AVSS1), and 5PIN(AVDD2), 6PIN(AVSS2), and 12PIN (VSS), 13PIN (VDD) respectively.

To obtain accurate frequency, capacitance (pF) need to be placed between 3PIN (AVSS1) and 1PIN (XIN), 3PIN (AVSS1) and 16PIN(XOUT).

Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.

For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU3058FV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of GND wiring, and routing of wiring.

●Cautions on use（common）

（1）Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

（2）Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

（3）Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

（4）Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

（5）GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

（6）Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

（7）Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

（8）Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

（9）Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

（10）Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

（11）External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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