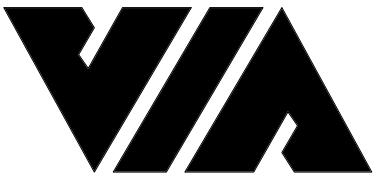


VT83C469

PCMCIA Socket Controller

DATA SHEET
(Preliminary)

DATE : March 13, 1995

VIA TECHNOLOGIES, INC.

VIA VT83C469 PCMCIA SOCKET CONTROLLER

DATE: MARCH 13, 1995

OVERVIEW

The VIA VT83C469 is a highly integrated PC Card socket controller chip that implements the PCMCIA 2.0/JEIDA 4.1 specifications. The chip is register compatible with the INTEL 82365SL and supports two PC card sockets with a fully buffered PCMCIA interface. No external buffer is required between the ISA bus and PCMCIA bus. For systems requiring more than two sockets, the VT83C469 can be cascaded to support up to eight sockets without external logic. Under EEPROM IO resource data, the VT83C469 can support unlimited sockets under ISA Plug and Play mode

In addition, the VT83C469 offers a jumperless configuration mechanism which allows the system manufacturer to set up a configuration (CONFIG.SYS) driver for PC card setup.

FEATURES

- Single chip PCMCIA controller between ISA bus and PCMCIA bus
- Full ExCA implementation of two PCMCIA 2.0/JEIDA 4.1 PC Card sockets
- Register-compatible with INTEL 82365SL
- Supports memory cards, I/O cards and DMA cards
- Supports PCMCIA-ATA disk interface
- 8 or 16-bit CPU interface
- 8 or 16-bit PCMCIA interface support
- High integration without any external logic or buffers
- Five mappable memory windows and two I/O windows for each socket
- Pin to Pin compatibility with Vadem VG-468
- 208 PQFP/Two sockets support
- Plug and Play ISA specifications version 1.0 with EEPROM
  - — Supports dynamic relocation of address space to avoid conflicts with system resources.
  - — Supports multiple PCMCIA controllers
  - — Features easy interface and design for docking stations
- Mixed voltage operation
  - — Support 3.3v or 5v PCMCIA socket interface
- Support PC card DMA operation
- Dual configuration for drive bay: socket controller can be located either on motherboard/ISA plug-in board or in the drive bay housing
- Support up to 8 sockets without external decoding

ARCHITECTURAL OVERVIEW

The VT83C469 functional blocks include the PCMCIA/JEIDA PC Card socket interface, ISA interface, memory and I/O window mapping, socket power management, interrupt steering, configuration registers and ATA mode operation.

PCMCIA/JEIDA PC Card Socket Interface

The PCMCIA/JEIDA interface consists of 60 signals and 8 power connections that interfaces to PC Cards through a 68 pin socket. A single VT83C469 can be configured to support either one or two sockets. Up to eight PC Card sockets may be supported by cascading VT83C469 chips. This chip supports memory, I/O and ATA card interchangeably.

ISA Interface

The VT83C469 interfaces directly to the ISA bus. No external buffers or transceivers are needed. For systems based on the 386SL, this chip provides the special signals INTR, RIO#, PWRGOOD, HDREQ, HDACK#, HTC, DREQ#, DACK, TC#, HBUFDIR, LBUFDIR, D7BUFDIR, A_5VDECT AND B_5VDECT.

Memory and I/O Window Mapping

Multiple PC cards in a system could conflict if they try to utilize the same system memory and I/O space. The VT83C469 allows the drivers to map a memory card into up to five separate windows and an I/O card into two separate windows, thus avoiding system configuration conflicts.
The VT83C469 provides memory paging, memory address mapping for PC card attribute and common memory, and I/O address mapping. The VT83C469 includes registers which provide access to the card information structure and card configuration registers within PC card's attribute memory (as described by the PCMCIA/JEIDA PC Card Standard).

Power Management for Socket Side and Core

At power on, if there is no card plugged into any socket, power to the socket is turned off. When a card is inserted, one of two events occur. If the chip has been set for automatic power on, then the VT83C469 automatically enables the power to socket. If the VT83C469 has been configured to cause management interrupts for card detection events, a management interrupt is generated to inform driver of the fact that a card was installed. Software driver can then initialize the card, or in the case of manual power detection, power the socket up manually and then initialize it.
When a card is removed from a socket, and if the VT83C469 has been configured for automatic power on, the VT83C469 automatically disables VCC and VPP supplies to the socket.

Interrupt Steering

The VT83C469 steers the interrupt from the PC card to one of ten system interrupts. Multiple PC cards in a system can conflict if they try to utilize the same interrupt level. The VT83C469 can be programmed to eliminate this conflict by steering each PC card interrupt request to a different system interrupt.

Configuration Registers

The VT83C469 provides a register containing interface identity and version information for each socket.

ATA Mode Operation

The VT83C469 supports direct connection to AT attached interface hard drives. ATA drives use an interface that is very similar to the IDE interface found on many popular portable computers. In this mode, the address and data conflict with the floppy drive is handled automatically.

Chip Mode Selection and Power-On Strapping

The VT83C469 can be set to four different modes: PCMCIA B Socket bus mode, ISA bus mode, normal mode and Plug and Play mode. In the normal mode (under VG-468 pin definition), no advanced features of the VT83C469 such as Plug and Play, DMA and 3.3/5V sockets power supports are available. The ISA bus mode and the PCMCIA B socket mode allows for add-on applications to control the data buffer's (ie. 74245) direction control. The Plug and Play mode changes these pins to EEPROM for Plug and Play resource data support.

Mode Configuration

HDACK# (PIN 67)	HTC (PIN 68)	MODE
Pull up	Pull up	normal mode
Pull up	Pull down	ISA bus buffer mode
Pull down	Pull up	PCMCIA bus buffer mode
Pull down	Pull down	PnP mode

Buffered bus direction support and PnP mode

PINS	PCMCIA B SOCKET BUS MODE	ISA BUS MODE	NORMAL MODE (VG-468 MODE)	PNP MODE
136	**SHBUFDIR**	**HHBUFDIR**	IRQ15	**E2CS**
152	**SLBUFDIR**	**HLBUFDIR**	INTR#	**E2SK**
153	**---**	**D7BUFDIR**	SPKROUT	**E2DIO**

Note: SHBUFDIR Socket Data high byte direction
SLBUFDIR Socket Data low byte direction
HHBUFDIR ISA Data high byte direction
HLBUFDIR ISA Data high byte direction

PC Card interface I/O Register Addressing

The VT83C469 registers are accessed through an 8-bit indexing mechanism. Two I/O addresses are used to access the VT83C469 registers. The first I/O address is the index register, which is fixed at 3E0h or 3E2h. The second I/O address is the data register, which is fixed at 3E1h or 3E3h. During PnP mode, the contents of the EEPROM resource data will determine whether the IO base will be set by the PnP BIOS or PnP utility. Each VT83C469 contains a block of 64 indirectly access registers. The starting base of the index register values in each VT83C469 is selected by pull-up/pull-down strapping resistor on INTR# and SPKROUT# pin, according to the table below. While RESETDRV is true, this pin is used for input. The falling edge of RESETDRV latches the pull up or down state of this pin, and thereafter this pin is used for normal operation. The VT83C469 will not respond to a data register read or write operation or to an index register read operation unless the index register has first been written to with a valid index.

INTR#	SPKROUT# RESISTOR	BASE	INDEX	DATA
Pull up	Pull up	00h	3E0h	3E1h
Pull up	Pull down	80h	3E0h	3E1h
Pull down	Pull up	00h	3E2h	3E3h
Pull down	Pull down	80h	3E2h	3E3h

Memory and I/O Mapping

The VT83C469 provides logic to map portions of the 64MB common memory and/or 64MB attribute memory spaces on the PC Card into the smaller 16MB (ISA) system address space. The VT83C469 mapping function provides extension of the system address space up to the full 64MB PC Card capability.
Start and stop addresses are specified with ISA address bits 23 through 12. This sets the minimum size of a memory window into 4KB. Memory windows are specified in the ISA address from 64K to 16MB. Note that no memory window can be mapped in the first 64K of the ISA address space. Only I/O address windows are allowed to be mapped between 0 and 64KB in the ISA address space.

PC Card memory is accessed only when all of the following conditions are satisfied:

1. The system memory address mapping window is enabled.
2. The system memory address is greater than or equal to the system memory address mapping start register A23:A12.
3. The system memory address is less than or equal to the system memory address mapping stop register A23:A12..

An I/O PC Card is accessed when the following conditions are satisfied:

1. The I/O address window is enabled.
2. The system address is greater than or equal to the I/O address start register A15:A0.
3. The system address is less than or equal to the I/O address stop register A15:A0
4. The access is not a DMA transfer. AEN = 0 to access the I/O PC Card.

Mixed Voltage Operation

The VT83C469 has three power planes: the ISA bus interface, socket A interface and socket B interface. The ISA bus power planes connect to the core power plane and supports 5v operation. Socket A and socket B power planes each can be independently connected to 3v or 5v. The two voltage detect pins are: A_5VDECT and B_5VDECT.

PINS	VT83C469 PIN DEFINITION	VG-468 PIN DEFINITION
191	A_5VDet	Vcc
141	B_5VDet	Vcc
27	A_3Ven	GND
101	B_3Ven	GND

In a mixed voltage implementation, the socket will not be powered unless there is a card in the socket. After the card is inserted, the system reads the voltage sensor pins and allows the CIS to determine the voltage to be applied to the card. Then it writes to the POWER control register, bit 4, which enables the outputs to the voltage switch.

Plug and Play

The VT83C469 supports the Plug and Play 1.0 specifications which provides automatic configuration capability. This feature allows the Plug and Play BIOS or Operating System (i.e. Windows 95) to relocate the VT83C469 register from the default to 3E0h/3E1h, 3E2h/3E3h or any other I/O address from the EEPROM containing the I/O resource.

When Plug and Play is enabled, the drive bay buffer mode cannot be enabled and the INTR# output cannot be used. In order to enable Plug and Play mode, the following register strapping must be used: pull down HDACK# and pull down HTC.

Three 8 bit ports are used by the software to access the Plug and Play configuration space. The ports are listed in the following table:

PORT NAME	LOCATION	LOCATION
Address	279H	Write only
Write_data	A79H	Write only
Read_data	200H ~ 3FFH	Read only

Auto Configuration Registers

PnP Register set

ADD	STD	DESCRIPTION	DEF	Type
0x00	X	SET READ_DATA PORT	0x00	W
0x01	X	SERIAL ISOLATION	0x00	R
0x02	X	CONFIGURE CONTROL	0x00	W
0x03	X	WAKE CSN	0x00	W
0x04	X	RESOURCE DATA	0x00	R/W
0x05	X	STATUS	0x00	R
0x06	X	CARD SELECT NUMBER	0x00	R/W
0x07	X	LOGICAL DEVICE NUMBER	0x00	R
0x30	X	ACTIVES	0x00	W
0x31	X	I/O RANGE CHECK	0x00	R/W
0x60	X	I/O BASE ADDRESS 0 [15:8]	0x00	R/W
0x61	X	I/O BASE ADDRESS 0 [7:0]	0x00	R/W

PC Card DMA Operations

The VT83C469 supports the use of a PC card as an interface with a DMA device. The VT83C469 defines an extension to the I/O card definition that allows ISA compatible DMA operation, including the Terminal Count signal required by the standard ISA floppy disk controller.

Only one socket at a time should be enabled for DMA transfer because the ISA bus DMA handshake is shared between both socket interfaces. Note: the original VG-468 pins 67 and 68 are defined as GPIO. The VT83C469 defines these pins as HDACK# and HTC.

The PCMCIA interface signals are redefined as the DMA interface signals according to the following table:

DMA Mode Socket Side Signal		
Pin	**Default Pin Function**	**Alternate Pin Function**
61,132	IOIS16#	DREQ#
54,125	SPKR#	DREQ#
49,120	INPACK#	DREQ#
1,72	REG#	DACK
16,87	OE#	TC#
30,100	WE#	TC#

Register Set

The following is a list of VT83C469 registers and their offset values. The General Registers, Interrupt Registers, I/O Registers and Memory Registers are fully compatible with the Intel 82365SL. The other registers are unique to the VT83C469.

SOCKET A OFFSET	SOCKET B OFFSET	REGISTER NAME
00h	40h	Identification and Revision
01h	41h	Interface Status
02h	42h	Power Control
03h	43h	Interrupt and General Control
04h	44h	Card Status Change
05h	45h	Card Status Change Interrupt Configuration
06h	46h	Address Window Enable
07h	47h	I/O Control
08h	48h	I/O Address 0 Start Low Byte
09h	49h	I/O Address 0 Start High Byte
0Ah	4Ah	I/O Address 0 Stop Low Byte
0Bh	4Bh	I/O Address 0 Stop High Byte
0Ch	4Ch	I/O Address 1 Start Low Byte
0Dh	4Dh	I/O Address 1 Start High Byte
0Eh	4Eh	I/O Address 1 Stop Low Byte
0Fh	4Fh	I/O Address 1 Stop High Byte
10h	50h	System Memory Address 0 Mapping Start Low Byte
11h	51h	System Memory Address 0 Mapping Start High Byte
12h	52h	System Memory Address 0 Mapping Stop Low Byte
13h	53h	System Memory Address 0 Mapping Stop High Byte
14h	54h	Card Memory Offset Address 0 Low Byte
15h	55h	Card Memory Offset Address 0 High Byte
16h	56h	Misc Control 1
17h	57h	Reserved
18h	58h	System Memory Address 1 Mapping Start Low Byte
19h	59h	System Memory Address 1 Mapping Start High Byte
1Ah	5Ah	System Memory Address 1 Mapping Stop Low Byte
1Bh	5Bh	System Memory Address 1 Mapping Stop High Byte
1Ch	5Ch	Card Memory Offset Address 1 Low Byte
1Dh	5Dh	Card Memory Offset Address 1 High Byte
1Eh	5Eh	Misc Control 2
1Fh	5Fh	Chip Information
20h	60h	System Memory Address 2 Mapping Start Low Byte
21h	61h	System Memory Address 2 Mapping Start High Byte
22h	62h	System Memory Address 2 Mapping Stop Low Byte
23h	63h	System Memory Address 2 Mapping Stop High Byte
24h	64h	Card Memory Offset Address 2 Low Byte
25h	65h	Card Memory Offset Address 2 High Byte
26h	66h	ATA Mode Control
27h	67h	Reserved
28h	68h	System Memory Address 3 Mapping Start Low Byte
29h	69h	System Memory Address 3 Mapping Start High Byte

SOCKET A OFFSET	SOCKET B OFFSET	REGISTER NAME
2Ah	6Ah	System Memory Address 3 Mapping Stop Low Byte
2Bh	6Bh	System Memory Address 3 Mapping Stop High Byte
2Ch	6Ch	Card Memory Offset Address 3 Low Byte
2Dh	6Dh	Card Memory Offset Address 3 High Byte
2Eh	6Eh	VIA ID
2Fh	6Fh	DMA Control
30h	70h	System Memory Address 4 Mapping Start Low Byte
31h	71h	System Memory Address 4 Mapping Start High Byte
32h	72h	System Memory Address 4 Mapping Stop Low Byte
33h	73h	System Memory Address 4 Mapping Stop High Byte
34h	74h	Card Memory Offset Address 4 Low Byte
35h	75h	Card Memory Offset Address 4 High Byte
36h	76h	Reserved
37h	77h	Reserved
38h	78h	Reserved
39h	79h	Reserved
3Ah	7Ah	Reserved
3Bh	7Bh	Reserved
3Ch	7Ch	Reserved
3Dh	7Dh	Reserved
3Eh	7Eh	Reserved
3Fh	7Fh	Reserved

CHIP CONTROL REGISTERS

Identification and Revision Register (Read Only)
Address : Index (Base + 00h)

BIT	FUNCTION
D[7:6]	VT83C469 Interface Type Type of PC Card supported by the socket. These bits do not identify the type of card that is present at the socket. 00: I/O only. 01: Memory only. 10: Memory & I/O. 11: Reserved.
D[5:4]	Reserved. These bits will be read back as zero.
D[3:0]	These four bits indicate the revision of the chip. 0010 is compatible with Intel.

Interface Status Register (Read Only)
Address : Index (Base + 01h)

BIT	FUNCTION
D7	Reserved
D6	PC Card Power Active 0: Power to the socket is off (Vcc and Vpp1 are no connection). 1: Power to the socket is on (Vcc is set according to bit 1 in Miscellaneous Control 1 register and DET_5 pin, Vpp1 is set according to bit 1:0 in the power control register).
D5	Ready/Busy# 0: PC Card is busy. 1: PC Card is ready.
D4	Memory Write Protect. Bit value is the logic level of the WP signal on the memory PC Card interface. 0: PC Card is not write protected. 1: PC Card is write protected.
D3	Card Detect 2 Together with card detect 1 indicates a card is present at the socket and fully seated. 0: CD2# signal on the PC Card interface is inactive. 1: CD2# signal on the PC Cars interface is active.
D2	Card Detect 1 Together with card detect 2 indicates a card is present at the socket and fully seated. 0: CD1# signal on the PC Card interface is inactive. 1: CD1# signal on the PC Cars interface is active.
D[1:0]	Battery Voltage Detect 2 and 1. BVD1 BVD2 Status 0 0 battery dead 0 1 battery dead 1 0 warning 1 1 battery good For I/O PC Cards, bit 0 indicates the current status of the (STSCHG/RI#) signal from the PC Card when the ring indicate enable bit in the Interrupt and General control register is set to 0.

Power Control Register (Read/Write)
Address : Index (Base + 02h)

BIT	FUNCTION
D7	Output Enable. If this bit set to zero, the PC Card outputs listed below are tri-stated. CADR<25:0>, D<15:0>, CE2#, CE1#, IORD#, IOWR#, OE#, WE#, REG#, RESET. This bit should not be set until after this register has been written setting PC Card Power Enable previously.
D6	Reserved.
D5	Auto Power Switch Enable. 0: automatic socket power switching based on card detects is disable. 1: automatic socket power switching based on card detects is enable.
D4	PC Card Power Enable. 0: power to the socket is disabled. (Vcc and Vpp1 are all no connection) 1: power to the socket is enabled. (Vcc is set according to bit 1 in Miscellaneous Control 1 register and DET_5 pin, and Vpp1 is set according to bit 1:0 in this register)
D[3:2]	Reserved
D[1:0]	Vpp1 Power Control 00: no connection. 01: Vcc. 10: 12V. 11: reserved.(this setting then Vpp1 will be a no connection)

The following table describes the slot power control function.

OUTPUT	PC CARD POWER ENABLE	AUTO POWER SWITCH ENABLE	CD1#	CD2#	TRI-STATE OUTPUTS	PC CARD POWER ACTIVE
x	0	x	x	x	OFF	0
0	1	0	0	0	OFF	1
1	1	0	0	0	ON	1
x	1	0	x	1	OFF	1
x	1	0	1	x	OFF	1
0	1	1	0	0	OFF	1
1	1	1	0	0	ON	1
x	1	1	x	1	OFF	0
x	1	1	1	x	OFF	0

Interrupt Register (Read/Write)
Address : Index (Base + 03h)

BIT	FUNCTION
D7	Ring Indicate Enable. 0: For I/O PC Card, the STSCHG/RI# signal from card is used as the status change signal STSCHG#. The current status of this signal is then available to be read from the interrupt status register and this signal can be configured as a source for the card status change interrupt. 1: For I/O PC Card, the STSCHG/RI# signal from card is used as ring indicator signal and is passed through to the IRQ15(multi pin, set Misc Control 2 bit 7 to one is used as RI_OUT#). The ring indicate enable bit has no function when the PC Card type bit is set to zero (memory card).
D6	PC Card Reset This is a software reset to PC Card. 0: Activates the RESET to the PC Card. The RESET signal will be active until bit is set to one. 1: Deactivates the RESET signal to the PC Card.
D5	PC Card Type. 0: Memory PC Card. 1: I/O PC Card.
D4	INTR# Enable. 0: The INTR# does not indicate a card status change interrupt is steered to one of the IRQs lines according to bit 7:4 in the card status change interrupt configuration register. 1: Enable the card status change interrupt on the INTR# signal.
D[3:0]	IRQ Level Selection (I/O Cards Only). Refer to following table is the redirection of the PC Card interrupt according to these bits.

IRQ BIT3	IRQ BIT2	IRQ BIT1	IRQ BIT0	INTERRUPT REQUEST LEVEL
0	0	0	0	IRQ not select
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	IRQ3 enable
0	1	0	0	IRQ4 enable
0	1	0	1	IRQ5 enable
0	1	1	0	Reserved
0	1	1	1	IRQ7 enable
1	0	0	0	Reserved
1	0	0	1	IRQ9 enable
1	0	1	0	IRQ10 enable
1	0	1	1	IRQ11 enable
1	1	0	0	IRQ12 enable
1	1	0	1	Reserved
1	1	1	0	IRQ14 enable
1	1	1	1	IRQ15 enable

Card Status Change Register (Read Only)
Address : Index (Base + 04h)

BIT	FUNCTION
D[7:4]	R. 0000
D3	Card Detect Change. 0: No change detected on either CD2# or CD1#. 1: A change has been detected on CD2# and CD1#.
D2	Ready Change. 0: No change on RDY/BSY#, or I/O PC Card installed. 1: When a low to high has been detected on the RDY/BSY# signal indicating that the memory PC Card is ready to accept a new data transfer.
D1	Battery Warning. 0: No battery warning condition, or I/O PC Card installed. 1: A battery warning condition has been detected.
D0	Battery Dead (STSCHG#) For memory PC Cards, bit is set one when a battery dead condition has been detected. For I/O PC Cards, bit is set to one if ring indicate enable bit in the interrupt and general control register is set to zero and the STSCHG/RI# signal from the I/O PC Card has been pulled low. The system software then has to read the status change register in the PC Card to determine the cause of the status change signal STSCHG#. This bit reads zero for I/O PC Cards if the ring indicate enable bit in the interrupt and general control register is set to one.

NOTE : The Card Status Change Register contains the status for sources of the card status change interrupt. These sources can be enabled to generate a card status change interrupt by setting the corresponding bit in the card status change interrupt configuration register. Reading the Card Status Change Register causes the register bits to be reset to zero.
If the card status change interrupt is enabled to one of the system bus interrupt request lines, the corresponding IRQ signal remains active high until this register is read.

Card Status Change Interrupt Configuration Register (Read/Write)
Address : Index (Base + 05h)

BIT	FUNCTION
D[7:4]	Interrupt Steering for the Card Status Change Interrupt. These bits select the redirection of the card status change interrupt if the interrupt is not select to the output on the INTR# pin.
D3	Card Detect Enable. 0: Disables the generation of a card status change interrupt when the card detect signals changed. 1: Enables a card status change interrupt when a change has been detected on CD2# or CD1#.
D2	Ready Enable (Memory Card Only). 0: Disables the generation of a card status change interrupt when a low to high transition has been detected on the RDY/BSY# signal. 1: Enables a card status change interrupt when a low to high transition has been detected on the RDY/BSY# pin.
D1	Battery Warning Enable (Memory Card Only). 0: Disables the generation of a card status change interrupt when a battery warning condition has been detected. 1: Enables a card status change interrupt when a battery warning condition has been detected.
D0	Battery Dead Enable (STSCHG#). 0: Disables the generation of a card status change interrupt when a battery dead condition has been detected. (Memory PC Cards used). For I/O PC Cards, bit is ignored when a Ring Indicate Enable bit is set one. 1: For memory PC Cards, enables a card status change interrupt when a battery dead condition has been detected. For I/O PC Cards, enables the VT83C469 to generate a card status change interrupt if the STSCHG# signal has been pulled low by the I/O PC Card, assuming that the Ring Indicate Enable bit is set zero.

INTR ENABLE	IRQ BIT3	IRQ BIT2	IRQ BIT1	IRQ BIT0	INTERRUPT REQUEST LEVEL
0	0	0	0	0	IRQ not select
0	0	0	0	1	Reserved
0	0	0	1	0	Reserved
0	0	0	1	1	IRQ3 enable
0	0	1	0	0	IRQ4 enable
0	0	1	0	1	IRQ5 enable
0	0	1	1	0	Reserved
0	0	1	1	1	IRQ7 enable
0	1	0	0	0	Reserved
0	1	0	0	1	IRQ9 enable
0	1	0	1	0	IRQ10 enable
0	1	0	1	1	IRQ11 enable
0	1	1	0	0	IRQ12 enable
0	1	1	0	1	Reserved
0	1	1	1	0	IRQ14 enable
0	1	1	1	1	IRQ15 enable
1	x	x	x	x	Card Status Change Interrupt on INTR#

Address Window Enable Register (Read/Write)

Address : Index (Base + 06h)

BIT	FUNCTION
D[7:6]	I/O Window Enable [1:0]. 0: Inhibit the card enable signals to the PC Card when an I/O access occurs within the corresponding I/O address window. 1: Generate the card enable signals to PC card when an I/O access occurs within the corresponding I/O address window. I/O accesses pass addresses from the system bus directly through to the PC Card. The start and stop register pairs must all be set to the desired window values before setting this bit to one.
D5	MS16# Decode A23:12. 0: Generated MS16# from a decode of the system address lines A23:17 only. This means that a minimum, a 128K block of system memory address space is set aside as 16-bit memory only. 1: Generated MS16# from a decode of the system address lines A23:12.
D4	Memory Window 4 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D3	Memory Window 3 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D2	Memory Window 2 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D1	Memory Window 1 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card.
D0	Memory Window 0 Enable. 0: Inhibit the card enable signals to the PC Card when a memory access occurs within the corresponding system memory address window. 1: Generate the card enable signals when a memory access occurs within the corresponding system memory address window. When the system address is within the window, the computed address will be generated to the PC Card. NOTE: The start, stop and offset registers pairs must all be set to the desired window values before setting bit to one.(All Memory Windows).

I/O Control Register (Read/Write)
Address : Index (Base + 07h)

BIT	FUNCTION
D7	I/O Window 1 Wait State. 0: 16-bit system accesses occur with no additional wait state. 1: 16-bit system accesses occur with one additional wait state(4 BUSCLKs).
D6	I/O Window 1 zero wait state. 0: 8-bit system I/O access will occur with additional wait state. 1: 8-bit system I/O access will occur with no additional wait state and the NOWS# will be returned to the system bus.
D5	I/O Window 1 IOCS16# Source. 0: IOCS16# is generated based on the value of the data size bit. 1: IOCS16# is generated based on the IOIS16# signal from PC Card.
D4	I/O Window 1 Data Size. 0: 8-bit I/O data path to PC Card. 1: 16-bit I/O data path to PC Card.
D3	I/O Window 0 Wait State. 0: 16-bit system accesses occur with no additional wait state. 1: 16-bit system accesses occur with one additional wait state(4 BUSCLKs).
D2	I/O Window 0 zero wait state. 0: 8-bit system I/O access will occur with additional wait state. 1: 8-bit system I/O access will occur with no additional wait state and the NOWS# will be returned to the system bus.
D1	I/O Window 0 IOCS16# Source. 0: IOCS16# is generated based on the value of the data size bit. 1: IOCS16# is generated based on the IOIS16# signal from PC Card.
D0	I/O Window 0 Data Size. 0: 8-bit I/O data path to PC Card. 1: 16-bit I/O data path to PC Card.

I/O Address Start Register Low Byte (Read/Write)
Address : Window 0 Index (Base + 08h)
Address : Window 1 Index (Base + 0Ch)

BIT	FUNCTION
D[7:0]	I/O Window Start Address A[7:0] Low order address bits used to determine the start address of the corresponding I/O address window. This provides a minimum 1 byte window for I/O address window.

I/O Address Start Register High Byte (Read/Write)
Address : Window 0 Index (Base + 09h)
Address : Window 1 Index (Base + 0Dh)

BIT	FUNCTION
D[7:0]	I/O Window Start Address A[15:8] High order address bits used to determine the start address of the corresponding I/O address window.

I/O Address Stop Register Low Byte (Read/Write)
Address : Window 0 Index (Base + 0Ah)
Address : Window 1 Index (Base + 0Eh)

BIT	FUNCTION
D[7:0]	I/O Window Stop Address A[7:0] Low order address bits used to determine the stop address of the corresponding I/O address window. This provides a minimum 1 byte window for I/O address window.

I/O Address Stop Register High Byte (Read/Write)
Address : Window 0 Index (Base + 0Bh)
Address : Window 1 Index (Base + 0Fh)

BIT	FUNCTION
D[7:0]	I/O Window Stop Address A[15:8] High order address bits used to determine the stop address of the corresponding I/O address window.

System Memory Address Mapping Start Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 10h)
Address : Window 1 Index (Base + 18h)
Address : Window 2 Index (Base + 20h)
Address : Window 3 Index (Base + 28h)
Address : Window 4 Index (Base + 30h)

BIT	FUNCTION
D[7:0]	System Memory Window Start Address A[19:12] Low order address bits used to determine the start address of the corresponding system memory address mapping window. This provides a minimum 4K bytes window for memory address mapping window.

System Memory Address Mapping Stop High Byte Register (Read/Write)
Address : Window 0 Index (Base + 11h)
Address : Window 1 Index (Base + 19h)
Address : Window 2 Index (Base + 21h)
Address : Window 3 Index (Base + 29h)
Address : Window 4 Index (Base + 31h)

BIT	FUNCTION
D7	Data Size. 0: 8-bit memory data path to the PC Card. 1: 16-bit memory data path to the PC Card.
D6	Zero Wait State. 0: System memory access will occur with additional wait states. 1: System memory access will occur with no additional wait states and the NOWS# signal will be returned to the system bus. The WAIT# signal from PC Card will override this bit.
D[5:4]	R/W. 00
D[3:0]	System Memory Window Start Address A23:20. High order address bits used to determine the start address of the corresponding system memory address mapping window.

System Memory Address Mapping Stop Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 12h)
Address : Window 1 Index (Base + 1Ah)
Address : Window 2 Index (Base + 22h)
Address : Window 3 Index (Base + 2Ah)
Address : Window 4 Index (Base + 32h)

BIT	FUNCTION
D[7:0]	System Memory Window Stop Address A[19:12] Low order address bits used to determine the stop address of the corresponding system memory address mapping window. This provides a minimum 4K bytes window for memory address mapping window.

System Memory Address Mapping Start High Byte Register (Read/Write)
Address : Window 0 Index (Base + 13h)
Address : Window 1 Index (Base + 1Bh)
Address : Window 2 Index (Base + 23h)
Address : Window 3 Index (Base + 2Bh)
Address : Window 4 Index (Base + 33h)

BIT	FUNCTION
D[7:6]	Wait State bit 1:0. These bits determine the number of additional wait states for a 16-bit access to the system memory window. If the PC Card supports the WAIT# signal, wait states will be generated by the PC Card asserting the WAIT# signal. 00: standard 16-bit cycle (3 BUSCLKs per access) 01: 1 additional wait state (4 BUSCLKs per access) 10: 2 additional wait states (5 BUSCLKs per access) 11: 3 additional wait states (6 BUSCLKs per access)
D[5:4]	R/W. 00
D[3:0]	System Memory Window Stop Address A23:20. High order address bits used to determine the stop address of the corresponding system memory window.

System Memory Address Mapping Offset Low Byte Register (Read/Write)
Address : Window 0 Index (Base + 14h)
Address : Window 1 Index (Base + 1Ch)
Address : Window 2 Index (Base + 24h)
Address : Window 3 Index (Base + 2Ch)
Address : Window 4 Index (Base + 34h)

BIT	FUNCTION
D[7:0]	System Memory Window Offset Address A[19:12] Low order address bits which added to the system address bits A19:12 to generate card address.

System Memory Address Mapping Offset High Byte Register (Read/Write)
Address : Window 0 Index (Base + 15h)
Address : Window 1 Index (Base + 1Dh)
Address : Window 2 Index (Base + 25h)
Address : Window 3 Index (Base + 2Dh)
Address : Window 4 Index (Base + 35h)

BIT	FUNCTION
D7	Write Protect. 0: Write operations to PC Card through the corresponding system memory window are allowed. 1: Write operations to PC Card through the corresponding system memory window are inhibited.
D6	REG Active. 0: Access to the system memory will result in common memory space. 1: Access to the system memory will result in attribute memory space.
D[5:0]	Card Memory Offset Address A25:20. High order address bits which are added to the system address A23:20 to generate card address.

EXTENSION REGISTERS

Misc. Control 1 Register (Read/Write)
Address : Index (Base + 16h)

BIT	FUNCTION
D7	Inpack Support. 0: Inpack not support. 1: Inpack used to control data bus drivers during I/O read from the PC Card.
D[6:5]	Reserved
D4	Speaker Enable. 0: SPKCSEL# is tri-state. 1: SPKCSEL# is driven form the XOR of SPKR# from each enabled PC Card.
D[3:2]	Reserved
D1	V_{CC} 3v. This bit dtermines which output pin is to be used to enable V_{CC} power to be the socket when card power is to be applied. It is used in conjunction with bits 5-4 of the Power Control register. When this bit is "1," the 3.3v V_{CC} is applied to the PC card. When this bit is "0," 3.3v or 5v V_{CC} is determined by the DET_5 pin.
D0	This bit is connected to PCMCIA pin 43. Cards that will operate at 3.3v will drive this pin to a "0."

Misc. Control 2 Register (Read/Write)
Address : Index (Base + 1Eh)

BIT	FUNCTION
D7	RIOLED is RI Out. This bit determines the function of the RIOLED. When configured for ring indicate, RIOLED is used to resume the 386SL when a high to low change is detected on the STSCHG#. 0: Tri-state RIOLED if RIOLED is not used as LED output 1: RIOLED is connected to Ring Indicate on the processor.
D6	R/W. 0
D5	Tri-state SD7 bit. This bit enables floppy change bit compatibility. 0: Normal operation. 1: For I/O PC Card at address 03F7h and 0377h, do not drive SD7 bit.
D4	Drive LED Enable. This bit determines when SPKR# is used to drive an LED on RIOLED for disk access. 0: Tri-state RIOLED if RIOLED is not used as RI out. 1: RIOLED becomes an open drain output suitable for driving an LED.
D[3:0]	R/W. 0000

Compatible Chip Information with Cirrus Logic CL-6722 Register (Read/Write)
Address : Index (Base + 1Fh)

BIT	FUNCTION
D[7:6]	Chip Identification. (Read Only) This field identifies the VT83C469 device and compatible with Cirrus Logic CL-6722 device. For the first read of this register this field will be 11h; on the next read will be 00h.
D5	Dual/Single Socket. (Read Only) This bit will be 1b, because the VT83C469 is support two sockets.
D[4:2]	VT83C469 Revision. (Read Only) This field identifies the revision of this controller. It's initial value is 110h.
D[1:0]	R/W. 00

ATA Mode Control Register (Read/Write)
Address : Index (Base + 26h)

BIT	FUNCTION
D7	A25/CSEL. In ATA mode, this bit is applied to the ATA A25/CSEL and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D6	A24/M/S#. In ATA mode, this bit is applied to the ATA A24/M/S# and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D5	A23/VU. In ATA mode, this bit is applied to the ATA A23/VU and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D4	A22. In ATA mode, this bit is applied to the ATA A22 and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
9D3	A21. In ATA mode, this bit is applied to the ATA A21 and is vendor specific. Certain ATA drive vendor specific performance enhancements beyond the PCMCIA 2.0 standard may be controlled through use of this bit. This bit has no hardware control function when not in ATA mode.
D2	R/W. 0
D1	Speaker is LED Input. 0: Normal operation. 1: The PC Card SPKR# pin will be used to drive IRQ12 if Drive LED Enable is set.
D0	ATA Mode. 0: Normal operation. 1: Configures the socket interface to handle ATA type III disk drives.

VIA ID Register (Read)
Address: Index (Base + 2Eh)

BIT	FUNCTION
D [7:4]	Major Version R. 1000
D [3:0]	Minor Version R. 0001

DMA Control (Read/Write)
Address: Index (Base + 2Fh)

BIT	FUNCTION
D [7:6]	DMA Enable. At reset these bits are set to a "0," which is the non-DMA mode. If either or both of these bits is set, the socket is in DMA mode. The three codes select the use of one of three pins for the active low DREQ# input at the PCMCIA interface. 01: INPACK# 10: WP/IOIS16# 11: BVD2/SPKR#
D5	Reserved.
D4	DMA Data Size 0: During DMA read/write cycles, data size is 8-bit. 1: During DAM read/write cycles, data size is 16-bit. The I/O window data size bit in I/O control register and the IOIS16# signal are irrelevant during actual DMA cycles.
D [3:0]	Reserved.

VT83C469 PIN DESCRIPTION

BUS TYPE	SIGNAL	DESCRIPTION	PIN	TYPE
I	AEN	System Address Enable. High during DMA cycles, low otherwise	204	I
I	BALE	Bus Address Latch Enable. An active high input used to latch LA [23:17] at the beginning of the bus cycle	205	I
S	BVD1 (STSCHG#/ RI#)	If BVD1 is negated by a memory PC Card with a battery, it indicates that the battery is no longer serviceable and data is lost. For I/O PC Cards, this signal is held high when either or both the Signal on Change bit and Changed bit in the Card Status Register on the PC Card are set to zero. When both of the bits are one, the signal is held low. The Changed bit is the logical OR of the bits CVBAT1, CVBAT2, CWP and CBSYRDY in the Pin Replacement Register on the PC Card. Or this pin is connected to Ring Indicate, which is qualified by Ring Indicate Enable to be passed on to the *RIO pin.	54, 125	I
S	BVD2 (SPKR#)	BVD1 and BVD2 are generated by memory PC Cards with onboard batteries. These signals indicate the health of the battery. Both are asserted high when the battery is in good condition. When BVD2 is negated while BVD1 is still asserted, the battery should be replaced, although data integrity on the memory PC Card is still assured. When the I/O interface is selected, BVD2 may be used to provide a single amplitude Digital Audio waveform intended to be passed through to the system's speaker without signal conditioning.	52, 123	I
S	CA [25:0]	Card Address	15,19, 21, 23-26, 28, 31, 33-41, 43-44, 46, 48, 50-51, 53, 86, 90, 92, 94-99, 102, 104-107, 109-115, 117, 119, 121-122, 124	O
S	CD# [2:1]	Detects proper card insertion. The signals are connected to ground internally on the PC Card and will be forced low whenever a card is placed in a host socket. Status is available to software through the Interface Status Register.	63, 3, 134, 74	I
S	CE# [2:1]	Active low card enable signals. CE#1 is used to enable even bytes, CE#2 for odd bytes. A multiplexing scheme based on A0, CE#1, CE#2 allows 8-bit hosts to access all data on Card Data [7:0] if desired.	89, 83, 18, 11	O
I	CLK	System Clock	187	I

BUS TYPE	SIGNAL	DESCRIPTION	PIN	TYPE
I	D [15:0]	Card data	2, 4-10, 12, 13, 55-58, 60, 62, 73, 76-82, 84-85, 126-130, 133	I/O
I	HDACK#	HDACK: Host DMA Acknowledge	67	I
I	HTC	HTC: Host Terminal Count	68	I
S	INPACK#	Input acknowledge. Asserted by some PC Cards during I/O read cycles. This signal is used by the VG-468 to control the enable of its input data buffer between the card and CPU.	49, 120	I
S	INTR#	Interrupt Request output: Active low output requesting a nonmaskable interrupt to the CPU. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.	152	I/O
I	IOCHRDY	I/O Channel Ready. This active high signal indicates that the current I/O bus cycle has been completed. When a PC Card needs to extend a Read or Write cycle, the VG-468 pulls IOCHRDY low. IOCHRDY can be deasserted by either WAIT#, or by programming to add wait states for 16-bit memory and I/O cycles. If WAIT# is used in 16-bit mode, the wait state generator has to be set to 1 wait state.	150	O
I	IOCS16#	This active low I/O 16-bit chip select signal indicates to the host system the current I/O cycle is a 16-bit access. A 16-bit to 8-bit conversion is done if it is inactive.	148	O
I	IORD#	I/O Read signal is driven active to read data from the PC Card's I/O space. The REG# signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.	20, 91	O
I	IOWR#	I/O Write signal is driven active to write data to the PC Card's I/O space. The REG# signal and at least one of the Card Enable signals must also be active for the I/O transfer to take place.	22, 93	O
I	IRQs	IRQ [15, 14, 12:9, 7, 5:3]	136-140, 146-142	O
I	LA [23:17]	Local Address bus used to address memory devices on the ISA-bus. Together with the system address signals, they address up to 16MB on the ISA bus.	181-175	I
I	MEMCS16#	This active low 16-bit memory chip select signal indicates to the host system that the current memory cycle is a 16-bit access cycle. A 16-bit to 8-bit conversion is done if it is inactive.	149	O
I	MEMR#	Active low signal indicated a memory read cycle.	174	I
I	MEMW#	Active low signal indicates a memory write cycle.	174	I
S	OE#	Active low signal used to gate memory reads from memory cards.	16, 87	O

BUS TYPE	SIGNAL	DESCRIPTION	PIN	TYPE
I	HDREQ	Host DMA Request. This is the DMA request from a DMA device to the host.	208	I
	RDY/ BSY# (IREQ#)	Memory PC Cards drive Ready/Busy# low to indicate that the memory card circuits are busy processing a previous write command. It is set high when they are ready to accept a new data transfer command. For I/O PC Cards, this pin is used as an interrupt request and driven low to indicate to the host that a device on the I/O PC Card requires service by the host software. The signal is held at the inactive level when no interrupt is requested.	32, 103	I
S	REG#	Select attribute memory. This signal is set inactive (high) for all accesses to common memory of a PC Card. When it is active, access is limited to Attribute Memory when WE# or OE# are active, and to I/O ports when IORD# or IOWR# are active. I/O PC Cards will not respond to IORD# or IOWR# when the REG# signal is inactive. During DMA operations the REG# signal is inactive.	1, 72	O
S	RESET	Provides a hard reset to a PC Card and clears the Card Configuration Option Register, thus placing card in an unconfigured (memory interface) state.	45, 116	O
I	RESETDRV	Active high indicates a main system reset.	189	I
S	RIO#/LED	Ring Indicate Output. Pass through of Ring Indicate output from I/O PC Card. VG-468 can also be configured to activate RIO# on card detect changes. RIO# will be functional in CS# controlled power down. When disk drive LED enable is set, this signal becomes a driver for disk drive LED. Also, a resistor strapping input during RESETDRV to determine the functions of pin B_CA [11:4].	151	I/O
I	SA [16:0]	System Address bus used to address memory and I/O devices on the ISA bus. These signals are latched and are valid throughout the bus cycle.	203-192, 190, 186-183	I
I	SBHE#	System Byte High Enable. When asserted, this active low signal indicates that a data transfer is occurring on the upper byte of the system data bus.		
I	SD [15:0]	System Data Bus.	155-162, 172-170, 168, 167, 165-163	I/O
I	SIOR#	This active low I/O read signal instructs the VG-468 to drive data onto the data bus.	206	I
I	SIOW#	This active low I/O write signal instructs the VG-468 to latch the data on the data bus.	207	I

BUS TYPE	SIGNAL	DESCRIPTION	PIN	TYPE
MISC	SPKROUT#	Digital audio signal which provides a single amplitude (digital) audio waveform to drive the system's speaker. Passes through SPKR# from an I/O PC Card. This signal must be held high when no audio signal is present. Also, a resistor strapping input during RESETDRV to determine the mapping of socket A and socket B to one of four groups.	153	I/O
S	5Ven	Power Control signal for card Vcc.	66, 69	O
S	VPP1EN1	Power Control signal for card Vpp1	65, 70	O
S	VPP2EN1	Power Control signal for card Vpp2	64, 71	O
S	WAIT#	This signal is driven by the PC Card to delay completion of the memory or I/O cycle in progress.	47. 118	I
S	WE#/PRGM#	The host uses WE# for gating memory write data, and for memory PC Cards that employ programmable memory.	30, 100	O
S	WP (IOIS16#)	Reflects the status of the Write Protect switch on some memory PC Cards. If the memory PC Card has no write protect switch, the card will connect this line to ground (the card can always be written) or to Vcc (permanently write protected). When the I/O interface is selected, this pin is used for the "I/O is 16-bit Port" function: asserted by the PC Card when the address on the bus corresponds to an address to which the PC Card responds, and the I/O Port which is addressed is capable of 16 bit access. If this signal is not asserted during a 16-bit I/O access, the system will generate 8-bit references to the even and odd byte of the 16-bit port being accessed. If the 8-bit window size is selected, the IOIS16# is ignored.	61, 132	I
I	ZWS#	Zero Wait State. An active low output indicates that the PC Card wishes to terminate the present bus cycle without inserting additional wait states. This cycle will not be driven during a 16-bit I/O access.	147	O
S	A_Vcc	Socket A power signal for 3.3v or 5v	17, 59	P
S	B_Vcc	Socket B power signal for 3.3v or 5v	88, 108	P

VT83C469 NUMERICAL PINOUT

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	A_REG	53	A_CA0	105	B_CA16	157	SD13
2	A_D3	54	A_BVD1	106	B_CA22	158	SD12
3	A_CD1#	55	A_D0	107	B_CA15	159	SD11
4	A_D4	56	A_D8	108	B_VCC	160	SD10
5	A_D11	57	A_D1	109	B_CA23	161	SD9
6	A_D5	58	A_D9	110	B_CA12	162	SD8
7	A_D6	59	A_VCC	111	B_CA24	163	SD0
8	A_D12	60	A_D2	112	B_CA7	164	SD1
9	A_D13	61	A_WP	113	B_CA25	165	SD2
10	A_D7	62	A_D10	114	B_CA6	166	VCC
11	A_CE1#	63	A_CD2#	115	B_CA5	167	SD3
12	A_D14	64	A_VPP2EN1	116	B_RESET	168	SD4
13	A_D15	65	A_VPP1EN1	117	B_VA4	169	GND
14	GND	66	A_5Ven	118	B_WAIT#	170	SD5
15	A_CA10	67	HDACK#	119	B_CA3	171	SD6
16	A_OE#	68	HTC	120	B_INPACK#	172	SD7
17	A_VCC	69	B_5Ven	121	B_CA2	173	MEMW#
18	A_CE2#	70	B_VPP1EN1	122	B_CA1	174	MEMR#
19	A_CA11	71	B_VPP2EN1	123	B_BVD2	175	LA17
20	A_IORD#	72	B_REG#	124	B_CA0	176	LA18
21	A_CA9	73	B_D3	125	B_BVD1	177	LA19
22	A_IOWR#	74	B_CD1#	126	B_D0	178	LA20
23	A_CA8	75	GND	127	B_D8	179	LA21
24	A_CA17	76	B_D4	128	B_D1	180	LA22
25	A_CA13	77	B_D11	129	B_D9	181	LA23
26	A_CA18	78	B_D5	130	B_D2	182	SBHE#
27	A_3VEN	79	B_D6	131	B_GND	183	SA0
28	A_CA14	80	B_D12	132	B_WP	184	SA1
29	A_CA19	81	B_D13	133	B_D10	185	SA2
30	A_WE#	82	B_D7	134	B_CD2#	186	SA3
31	A_CA20	83	B_CE1#	135	GND	187	CLK
32	A_RDY	84	B_D14	136	IRQ 15	188	GND
33	A_CA21	85	B_D15	137	IRQ 14	189	RESETDRV
34	A_CA16	86	B_CA10	138	IRQ 12	190	SA4
35	A_CA22	87	B_OE#	139	IRQ 11	191	A_5VDET
36	A_CA15	88	B_VCC	140	IRQ 10	192	SA5
37	A_CA23	89	B_CE2#	141	B_5VDET	193	SA6
38	A_CA12	90	B_CA11	142	IRQ 3	194	SA7
39	A_CA24	91	B_IORD#	143	IRQ 4	195	SA8
40	A_CA7	92	B_CA9	144	IRQ 5	196	SA9
41	A_CA25	93	B_IOWR#	145	IRQ 7	197	SA10
42	GND	94	B_CA8	146	IRQ 9	198	SA11
43	A_CA6	95	B_CA17	147	ZWS#	199	SA12
44	A_CA5	96	B_CA13	148	IOCS16#	200	SA13
45	A_RESET	97	B_CA18	149	MEMCS16#	201	SA14
46	A_CA4	98	B_CA14	150	IOCHRY	202	SA15
47	A_WAIT#	99	B_CA19	151	RIO#	203	SA16
48	A_CA3	100	B_WE#	152	INTR#	204	AEN
49	A_INPACK#	101	B_3VEN	153	SPKROUT#	205	BALE
50	A_CA2	102	B_CA20	154	GND	206	SIOR#
51	A_CA1	103	B_RDY	155	SD15	207	SIOW#
52	A_BVD2	104	B_CA21	156	SD14	208	HDREQ

VT83C469 PIN DIAGRAM

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Ambient operating temperature	0	70	^{o}C
Storate temperature	-55	125	^{o}C
Input voltage	-0.5	5.5	V
Output voltage	-0.5	5.5	V

Note :
Stress above these listed cause permanent damage to device. Functional operation of this device should be restricted to the conditions described under operating conditions.

DC Characteristics

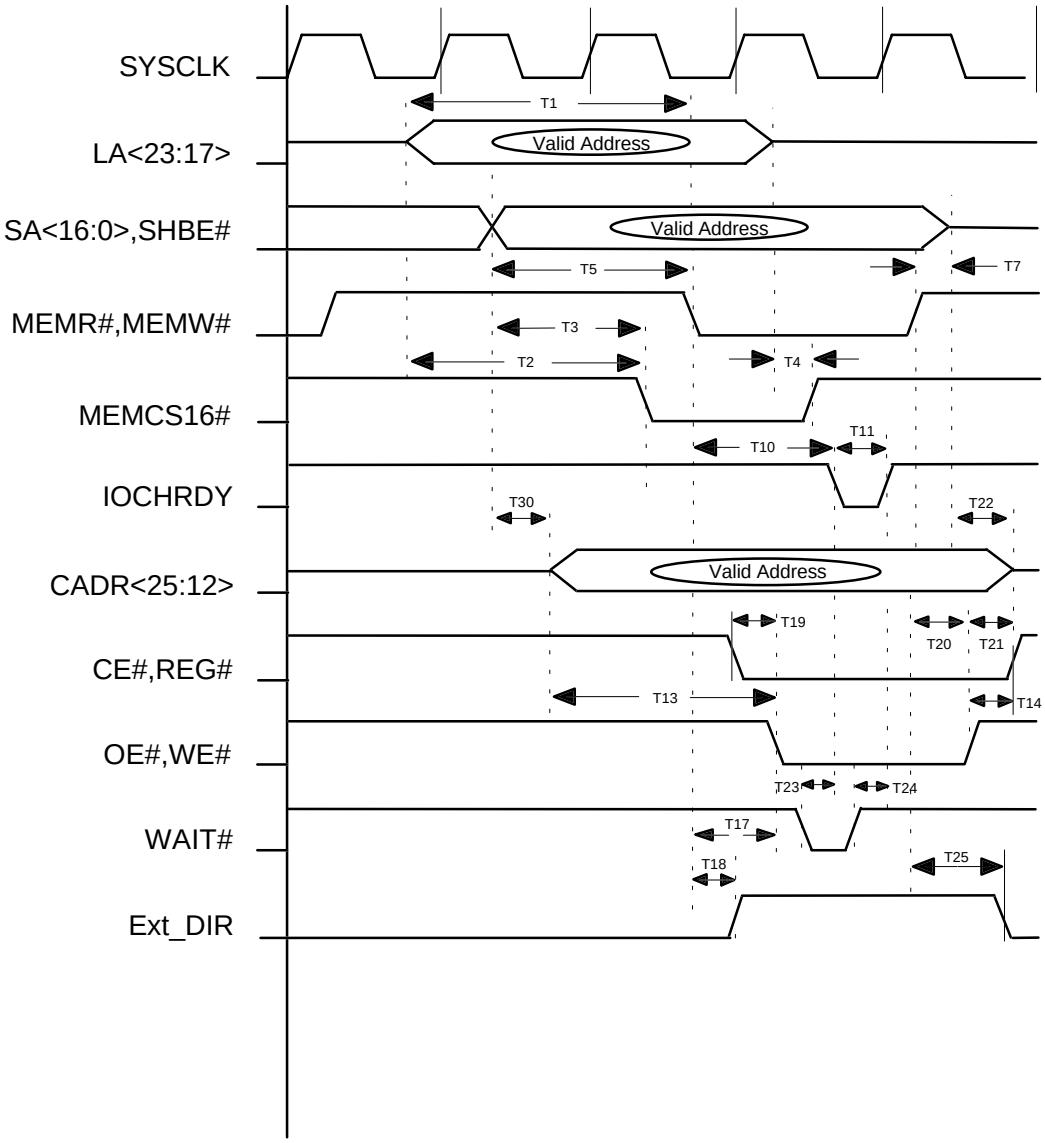
TA-0-70^{o}C, V_{DD}=5V=/-5%, GND=0V

Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input low voltage	-.50	0.8	V	
V_{IH}	Imput high voltage	2.0	V_{DD}+0.5	V	
V_{OL}	Output low voltage	-	0.45	V	I_{OL}=4.0mA
V_{OH}	Output high voltage	2.4	-	V	I_{OH}=-1.0mA
I_{IL}	Input leakage current	-	+/-10	uA	$0<V_{IN}<V_{DD}$
I_{OZ}	Tristate leakage current	-	+/-20	uA	$0.45<V_{OUT}<V_{DD}$
I_{CC}	Power supply current	-	80	mA	

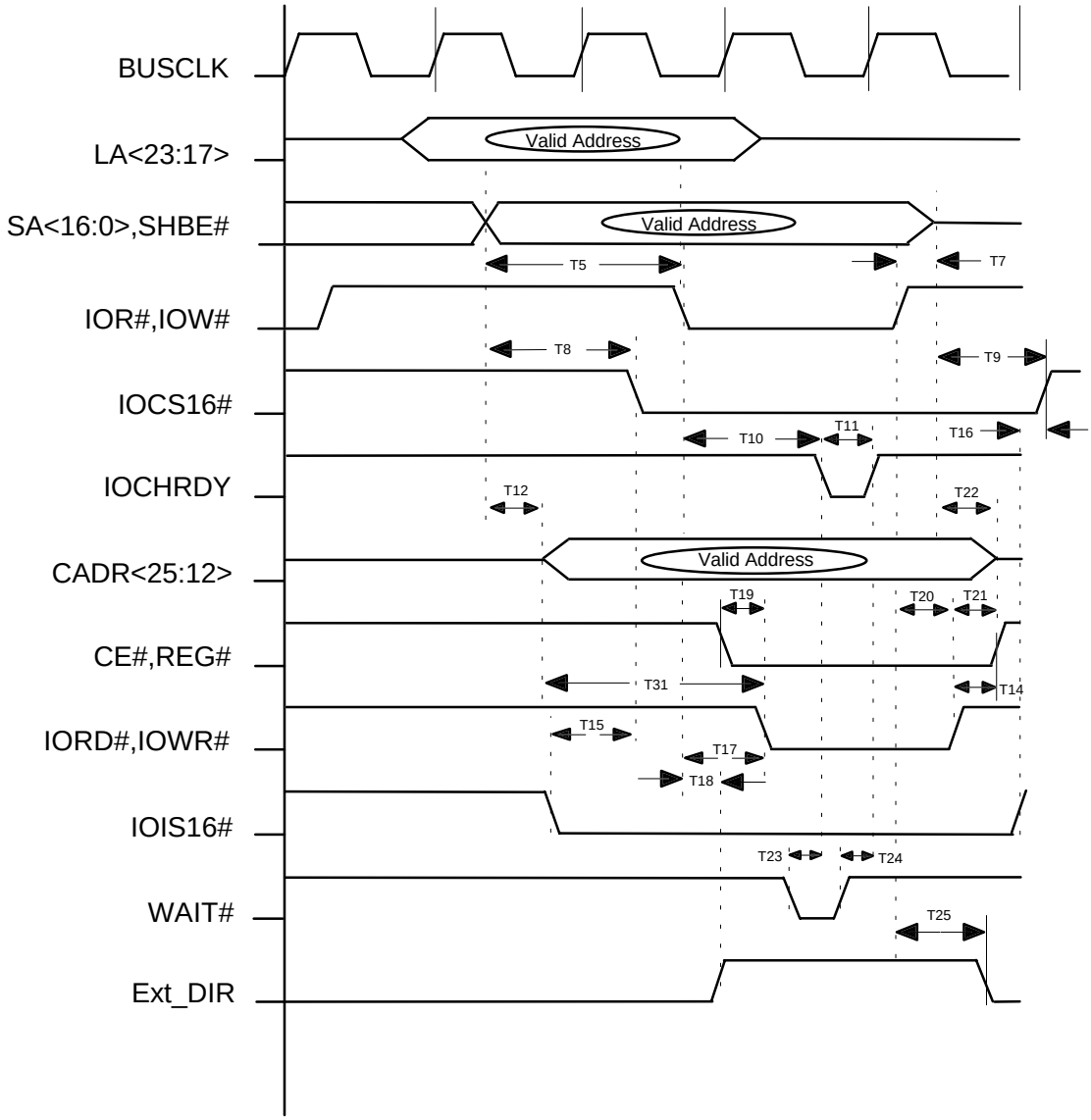
Parameter	Description	Min	Max
T1A	A<23:17> Setup to 16-Bit Memory Command	102	
T1B	A<23:17> Setup to 8-Bit Memory Command	162	
T2	MEMCS16# Valid from A<23:17>		58
T3	MEMCS16# Hold from A<16:00>		31
T4	MEMCS16# Hold from A<23:17>	0	
T5A	A<16:12> and SBHE# to 16-Bit Memory Command	18	
T5B	A<16:12> and SBHE# to 8-Bit Memory Command	84	
T5C	A<15:00> and SBHE# Setup to I/O Command	84	
T6	A<16:00> and SBHE# Hold from Command	25	
T7	IOCS16# Valid from A <15:00>		25
T8	IOCS16# Hold from A <15:00>	0	
T9	IOCHRDY Low from 16-Bit Command (Internal Wait State Generation)		20
T10	IOCHRDY Active Pulse Width (Memory Cycle) (Internal Wait State Generation)	123	363
T11	IOCHRDY Active Pulse Width (I/O Cycle) (Internal Wait State Generation)		63
T12A	A <15:12> to CA <25:12> Valid Delay, Memory Cycles		40
T12B	A <15:12> to CA <25:12> Valid Delay, I/O Cycles		26
T13A	CA <15:12> to Socket I/O CMD Setup	70	
T13B	CA <25:12> to Socket Memory CMD Setup	30	
T14A	Socket CMD to CE# Hold Time	20	
T14B	Socket CMD to REG# Hold Time	0	
T15	IOIS16# to IOCS16# Valid Delay		47
T16	IOCS16# Hold from IOIS16# Valid		12
T17	ISA CMD to SKT CMD Valid Delay for 8-Bit Memory, 8/16 I/O		22
T18	ISA Read CMD Falling to Data Output		21
T19	CE#, REG# Setup to Socket CMD Setup	5	
T20	ISA CMD Inactive to Socket CMD Inactive Valid Delay	0	20
T21	Socket CMD Inactive to CADR <25:12> Hold Time	20	
T22	CA <15:12> Hold from A <15:12> Memory	0	
T22	CA<15:12> Hold from A<15:12> I/O	0	

T23	WAIT# Active to IOCHRDY Inactive		16
T24	WAIT# Inactive to IOCHRDY Active		14
T25	EXT_DIR Hold from ISA Read Inactive	0	
T26	AEN Valid to ISA CMD Active Setup	40	
T27	AEN Hold from ISA Command Inactive	5	
T28	RI_to RI_OUT Delay		27
T29	SPKR_ to SPKR_OUT Delay		18
T30	Card Status Change to IRQ# Valid		7 BUSCLK
T31	PCMCIA IREQ# to IRQx Delay		24

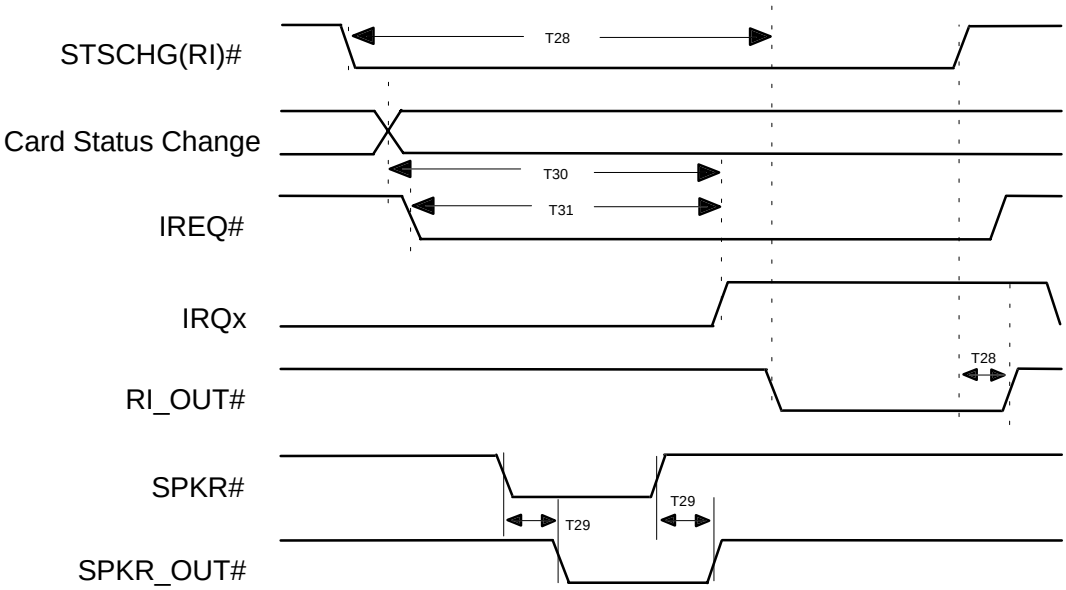
Memory: Standard/Extended



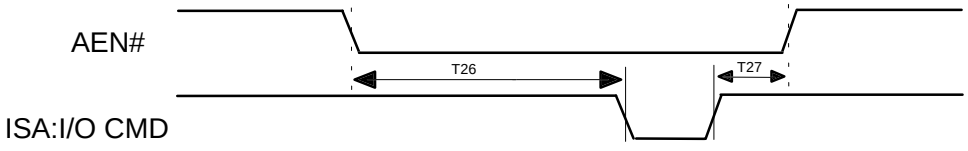
IO: Standard / Extended



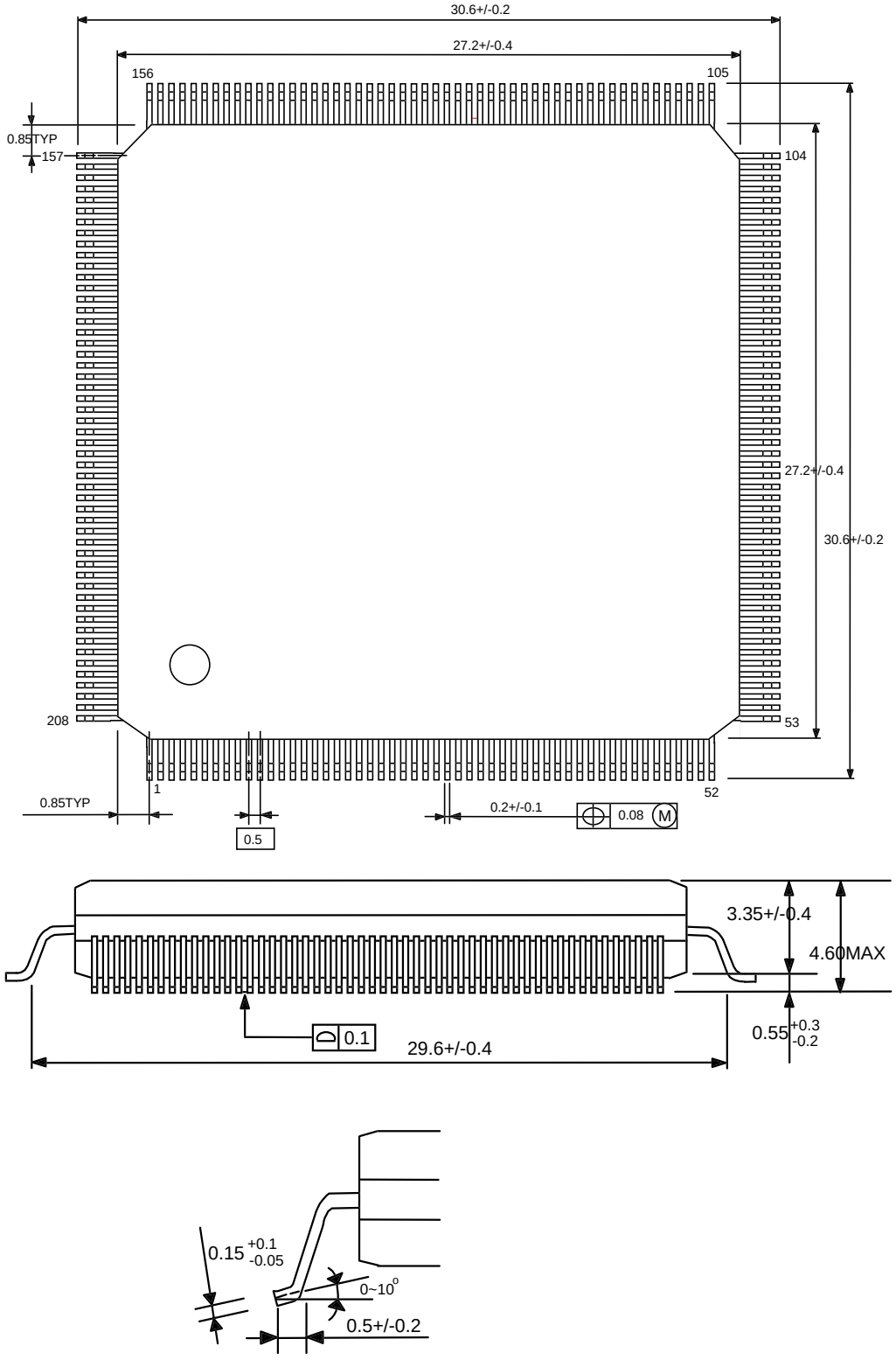
Interrupt, Ring Indicate, Speaker Timings



AEN Setup and Hold



208-Pin Plastic Flat Package



PROJECT SIGN OFF SHEET

FOR VT83C469 PRELIMINARY RELEASE

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