

Small Signal Diode


MSOP-10

Features

- ✧ Meet IEC61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)
- ✧ Meet IEC61000-4-4 (EFT) rating. 40A (5/50 μs)
- ✧ Meet IEC61000-4-5 (Lightning) rating. 5A (8/20 μs)
- ✧ Protects four high speed I/O lines
- ✧ Low working Voltage : 5V
- ✧ Pb free version, RoHS compliant, and Halogen free

Mechanical Data

- ✧ Case : MSOP-10 small outline plastic package
- ✧ Terminal: Matte tin plated, lead free, solderable per MIL-STD-202, Method 208 guaranteed
- ✧ High temperature soldering guaranteed: 260°C/10s
- ✧ Polarity : Indicated by cathode band
- ✧ Weight : 12mg (Approx.)
- ✧ Marking Code : R0544

Dimensions	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.17	0.27	0.007	0.011
D	0.50 _{REF}		0.020 _{REF}	
E	4.9 _{REF}		0.193 _{REF}	
F	-	1.11	-	0.044

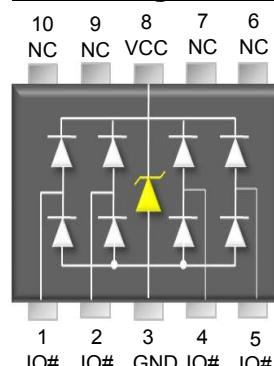
Ordering Information

Part No.	Package	Packing	Packing Code	Marking
TESDO5V0A	MSOP-10	3K / 7" Reel	ROG	R0544

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Pin Configuration



Maximum Ratings

Type Number	Symbol	Value	Units
Peak Pulse Power (tp=8/20 μs waveform)	P _{PP}	125	W
Peak Pulse Current (tp = 8/20 μs)	I _{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{ESD}	± 15 ± 8	KV
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to + 150	°C

Electrical Characteristics

Type Number	Symbol	Min	Max	Units
Reverse Stand-Off Voltage	V _{RWM}	-	5	V
Reverse Breakdown Volta	V _(BR)	6	-	V
Reverse Leakage Current	I _R	-	1	uA
Clamping Voltage	V _c	-	15	V
Junction Capacitance	C _J	1(Typ.)	-	pF

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Rating and Characteristic Curves

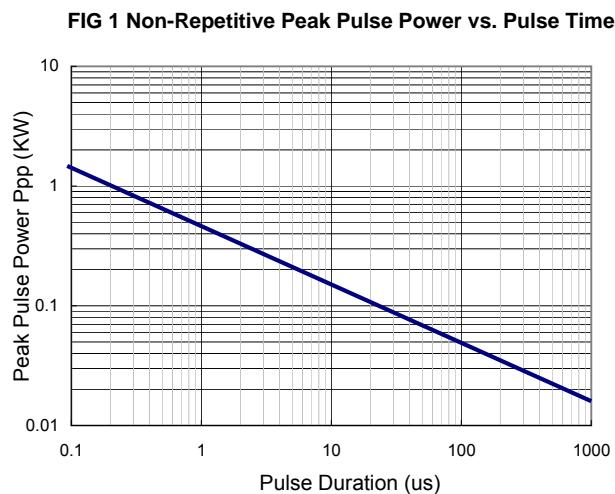


FIG 2 Pulse Waveform

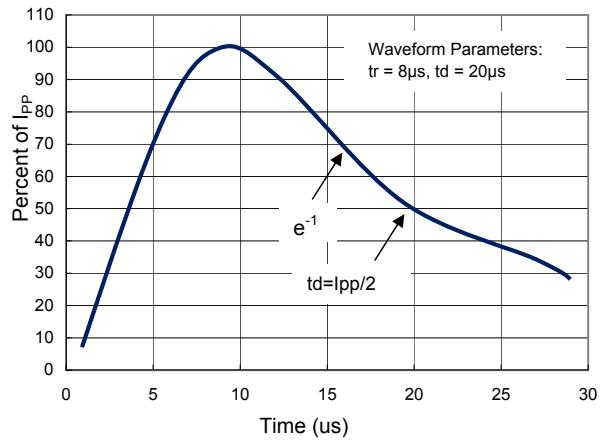


FIG 3 Admissible Power Dissipation Curve

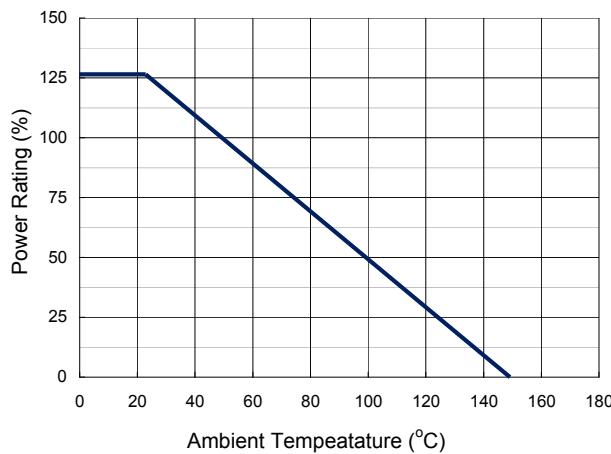


FIG 4 Typical Junction Capacitance

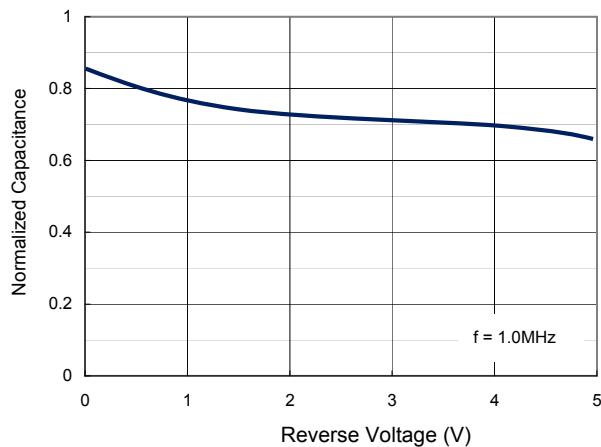
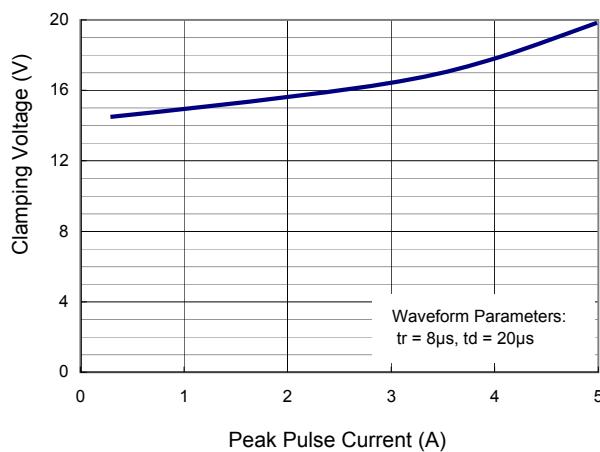


FIG 5 Clamping Voltage vs. Peak Pulse Current



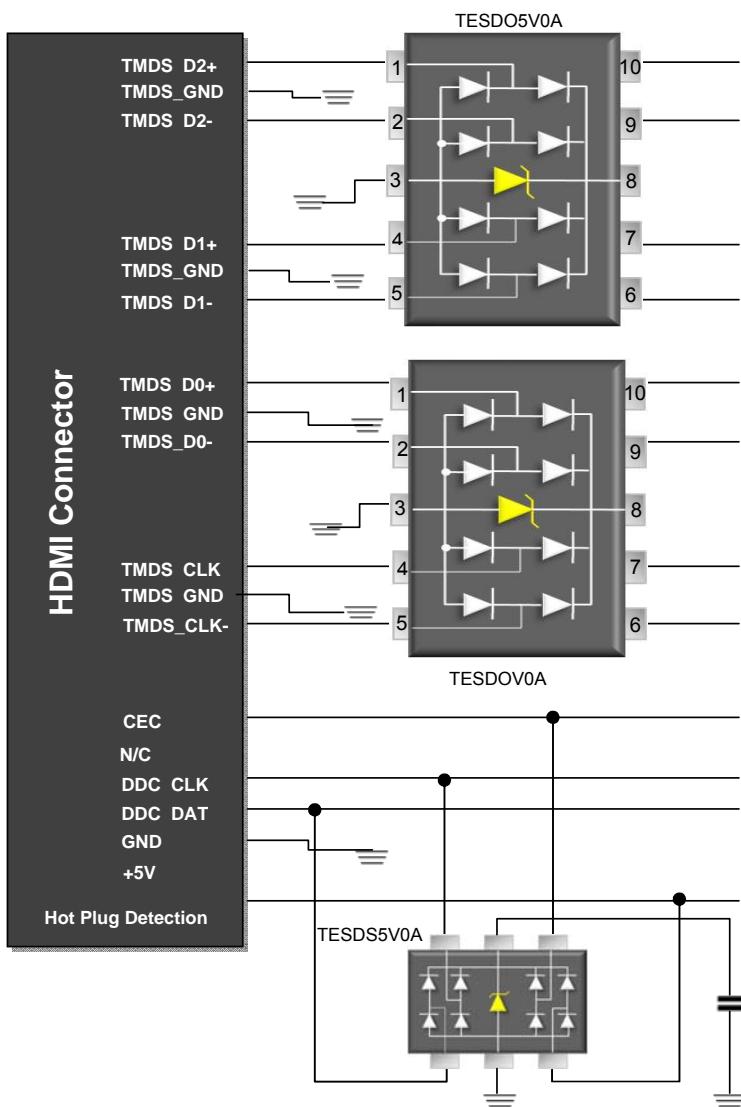
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Applications Information

- ◊ Designed for protection of high-speed interfaces such as HDMI
- ◊ Ultra low capacitance between the pairs while being rated to handle $>\pm 8\text{kV}$ ESD contact discharges and $>\pm 15\text{kV}$ air discharge
- ◊ Each device is in a leadless package that is less than 1.1mm wide
- ◊ Designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity
- ◊ TESDO5V0A is ultra low capacitance ESD protection array designed to protect high speed data interfaces
- ◊ The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications of high speed interface, ex HDMI, DisplayPortTM, MDDI, and eSATA interfaces.

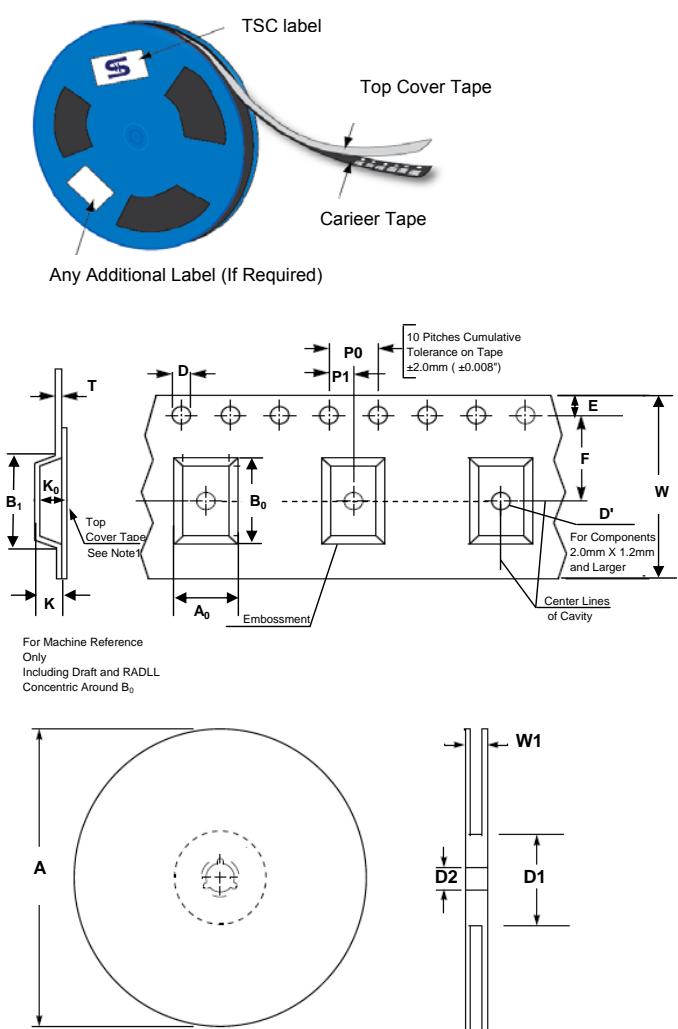
Circuit Board Layout Recommendations for HDMI application

- ◊ The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6)
- ◊ Signal line enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. Ground is connected at pins 3 and 8.
- ◊ One large ground pad should be used in lieu of two separate pads



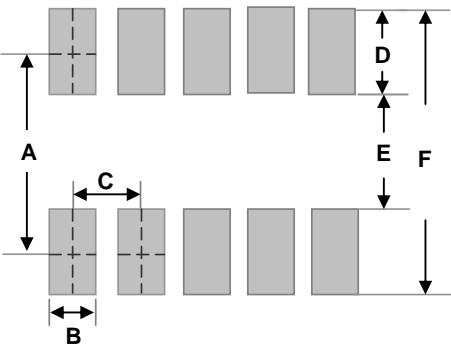
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Tape & Reel specification



Item	Symbol	Dimension (mm)
Carrier depth	K	1.22 Max.
Sprocket hole	D	1.50 +0.10
Reel outside diameter	A	180 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocket hole position	E	1.75 ± 0.10
Sprocket hole pitch	P0	4.00 ± 0.10
Embossment center	P1	2.00 ± 0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.

Suggested PAD Layout



Dimensions	Unit (inch)	Unit (mm)
A	0.161	4.10
B	0.012	0.30
C	0.020	0.50
D	0.063	1.60
E	0.098	2.50
F	0.224	5.70

Note 1: A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rotate more than 10° within the determined cavity.

Note 2: If B₁ exceeds 4.2 mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.

Note 3: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.