# STCL1100 STCL1120 STCL1160

High frequency silicon oscillator family

Features

- Fixed frequency 10/12/16 MHz
- ±1.5% frequency accuracy over all conditions
- 5 V ±10% operation
- Low operating current, ultra low standby current
- Push-pull, CMOS compatible frequency (square wave) output
- Chip enable input, active high
- Fast & stable start-up
- No external components required
- Temperature range: –20 to +85 °C
- Package: SOT23-5L
- RoHS compliant

SOT23-5L
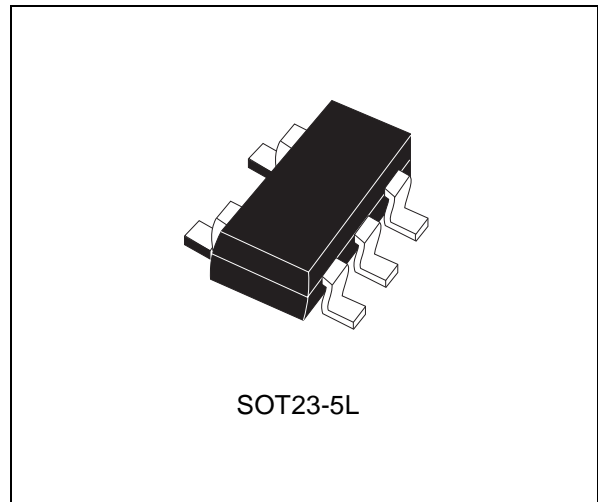
Description

The STCL1xx0 silicon oscillator devices are reliable, easy to use, 5-pin low-cost fixed frequency silicon oscillators developed primarily for microprocessor clock applications, display drivers or other system applications where tighter clock accuracy is not critical. Compared to ceramic resonators and crystal oscillators, silicon oscillators offer the advantages of faster start-up, smaller size and improved immunity to shock, vibration and EMI.

The STCL1xx0 silicon oscillator devices are equipped with chip enable input, offering an easy way to stop microprocessor clocking during a power saving mode while at the same time significantly reducing the oscillator current consumption.

Applications

- Motor control
- Home appliances
- Building control
- Advanced battery chargers
- Low speed USB applications
- Display drivers
- Generally where ceramic resonators are currently being used.

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1   Pin connections

1.1   Signal names

V_{CC} Positive supply voltage pin

F_{OUT} Frequency (square wave) output, CMOS compatible, push-pull

CE   Chip Enable input, active high, no internal pull-up resistor

GND   Ground

NC   No Connect

2   Typical application circuit

**Figure 2.   Microprocessor (MCU, microcontroller unit) clock example
- replacement of a crystal or ceramic resonator**
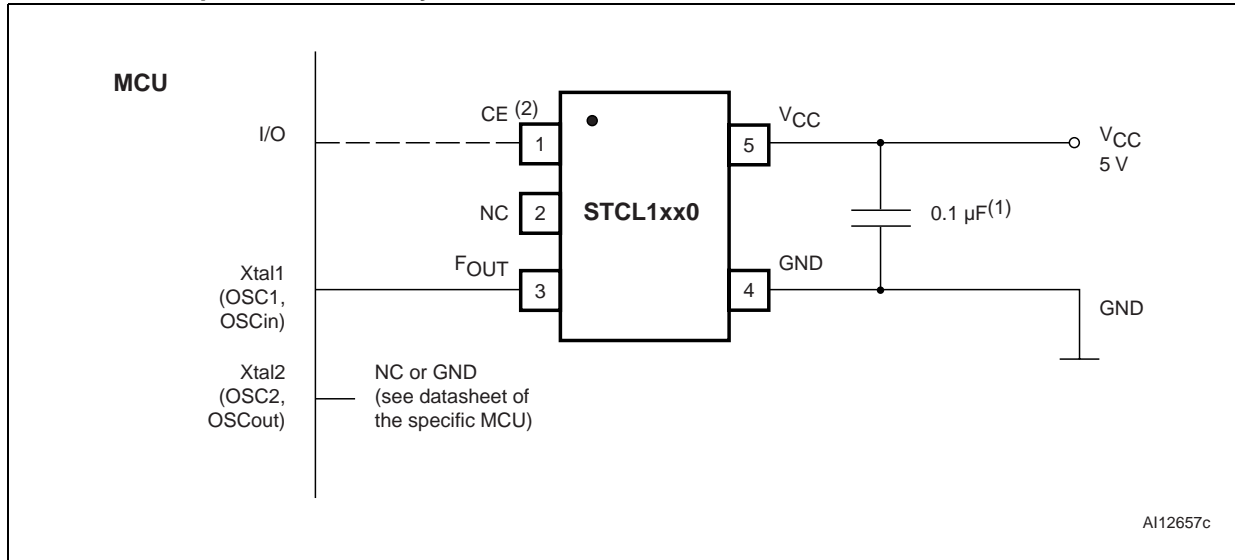
1. For reliable operation and to further improve immunity to harsh environment, the minimum 0.1 µF decoupling capacitor is recommended to be placed as close as possible to the V_{CC} and GND pins of the oscillator device. The whole oscillator block should then be placed near the microprocessor clock input.

2. To minimize standby current, no internal pull-up resistor to V_{CC} is implemented on the CE input, thus the input level must be permanently defined by the controlling signal. If the chip enable feature is not used, in active mode connect the CE pin to V_{CC}. In applications utilizing standby mode and where the CE pin is connected to the controlling I/O port of the clocked microprocessor, for successful start-up of the microprocessor at power-on, initial logic high level needs to be secured on the CE pin to provide clock already during the power-on reset until the microprocessor program starts and the controlling I/O port takes over the CE control.

3   Operation

Use of the STCL1xx0 silicon oscillator device is very simple. Once power is applied to V_{CC} pin, a CMOS-compatible square wave output signal is provided on the F_{OUT} output pin (in active mode the Chip Enable (CE) input pin must be at a logic high level).

3.1   Chip Enable (CE)

This feature allows the user to stop the clock and significantly reduce the current consumption when the application is put into power saving mode.

When used to clock the microprocessor in place of a crystal, the need for chip enable input stems from a difference in the way microprocessors normally disable their clock. In the case of a crystal or ceramic resonator, when going into power saving mode, the processor simply opens the internal Xtal inverter feedback which results in stopping the crystal oscillations; however in the case of the silicon oscillators this would not work and the oscillator would continue to run. So in order to use this feature, one of the microprocessor's output pins must be configured to control the silicon oscillator's Chip Enable (CE) input, see Typical Application Circuit diagram. To minimize standby current of the oscillator device, no internal pull-up resistor is implemented on the CE input, thus the input level must be permanently defined by the controlling signal.

3.2   Transition to disable

The device provides additional 32 complete clock cycles after the chip enable input went inactive to allow the clocked microprocessor to complete pipelined instructions before going into sleep mode. Then during disable the output remains low.

3.3   Fast start-up and wake-up from disable

The total start-up time until oscillations internally stabilize and remain within specifications is 50 µs max from the point when V_{CC} reached min operating voltage (at power on) or from the point when CE went active (wake-up from disable mode). The output remains low even during initial 16 cycles after CE went active to provide stabilized valid output waveform already from the first output cycle, see *Table 3: DC and AC parameters* and *Figure 8: Start-up output waveform, first cycles zoom (power-on), STCL1120*. Compare to milliseconds typical for crystal oscillators or hundreds of microseconds for ceramic resonators.

4   Maximum rating

Stressing the device above the rating listed in the *Table 1: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 1.   Absolute maximum ratings

Symbol	Parameter	Note	Value	Unit
T_{STG}	Storage temperature (V_{CC} Off)		−55 to 150	°C
T_{SLD}	Lead solder temperature for 10 seconds	Lead-free lead finish[1]	260	°C
V_{IO}	Input or output voltage		−0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage		−0.3 to 7	V

1.   Reflow at peak temperature of 260 °C (total thermal budget not to exceed 245 °C for more than 30 seconds).

5   DC and AC parameters

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following *Table 3: DC and AC parameters* are derived from tests performed under the DC and AC measurement conditions listed in the *Table 2*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 2.   DC and AC measurement conditions[1]

Parameter	
V_{CC} supply voltage	4.5 to 5.5 V
Ambient operating temperature	−20 to +85 °C
Load capacitance (C_L)	12 pF

1.   Unless other specified.

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Table 3.   DC and AC parameters[1]

Sym	Description	Test condition	Min	Typ	Max	Unit
V_{CC}	Operating voltage		4.5	5.0	5.5	V
I_{CC}	Operating current	F_{OUT} = 10 MHz, output unloaded		590	800	µA
		F_{OUT} = 12 MHz, output unloaded		650	900	µA
		F_{OUT} = 16 MHz, output unloaded		800	1050	µA
I_{CC2}	Standby current	CE = 0 V		2	3	µA
V_{OL}	Output voltage low	I_{OL} = 3 mA			0.4	V
V_{OH}	Output voltage high	I_{OH} = –3 mA	V_{CC} –0.4 V			V
V_{IL}	Input low voltage (CE input)				0.8	V
V_{IH}	Input high voltage (CE input)		2			V
I_{LI}	Input leakage current (CE input)		–1		+1	µA
	Frequency accuracy over all conditions[2], [3]	V_{CC} = 4.5 to 5.5 V, –20 to +85 °C, "B"			±1.5	%
	Frequency temperature drift				±150	ppm / °C
	Jitter	Cycle-to-cycle, 20 s measurement		±150		ps_{P-P}
	Duty cycle	Taken at half of the signal amplitude	40	50	60	%
t_{START}	Start-up time[4]	From the point when V_{CC} reached min operating voltage or CE went active until the oscillations stabilize within specifications.		30	50	µs
t_R, t_F	Rise/fall time	C_L = 12 pF; 10 to 90% of the amplitude		5		ns
C_L	Load capacitance			12		pF

1. Valid for Ambient Operating Temperature: T_A = –20 to +85 °C; V_{CC} = 4.5 to 5.5 V (except where noted).

2. Frequency vs. temperature characteristics has its maximum at room temperature, for both higher and lower temperatures the frequency decreases. Therefore, to reach symmetrical tolerances, the devices are factory-trimmed at room temperature to the frequency value close to higher tolerance limit. See Typical operating characteristics.

3. The specified values are for the recommended configuration, i.e. parts properly soldered on PCB, with 0.1 µF ceramic capacitor soldered close to the V_{CC}-GND pins and short leads between the output and scope probe (to minimize signal reflections; see output waveform screenshots for various conditions). Recommended is usage of the active scope probe that adds around 1 pF of the load capacity to the total load and having frequency counter connected to the scope output as input capacitance of the counter is typically in tens of pF. Installing the device in a socket may have an influence on the frequency and repeatability as well, depending on quality of its contacts.

4. For details see start-up waveform graph - *Figure 8*.

6   Typical operating characteristics and scope plots

Figure 3.   Frequency vs. temperature, STCL1120
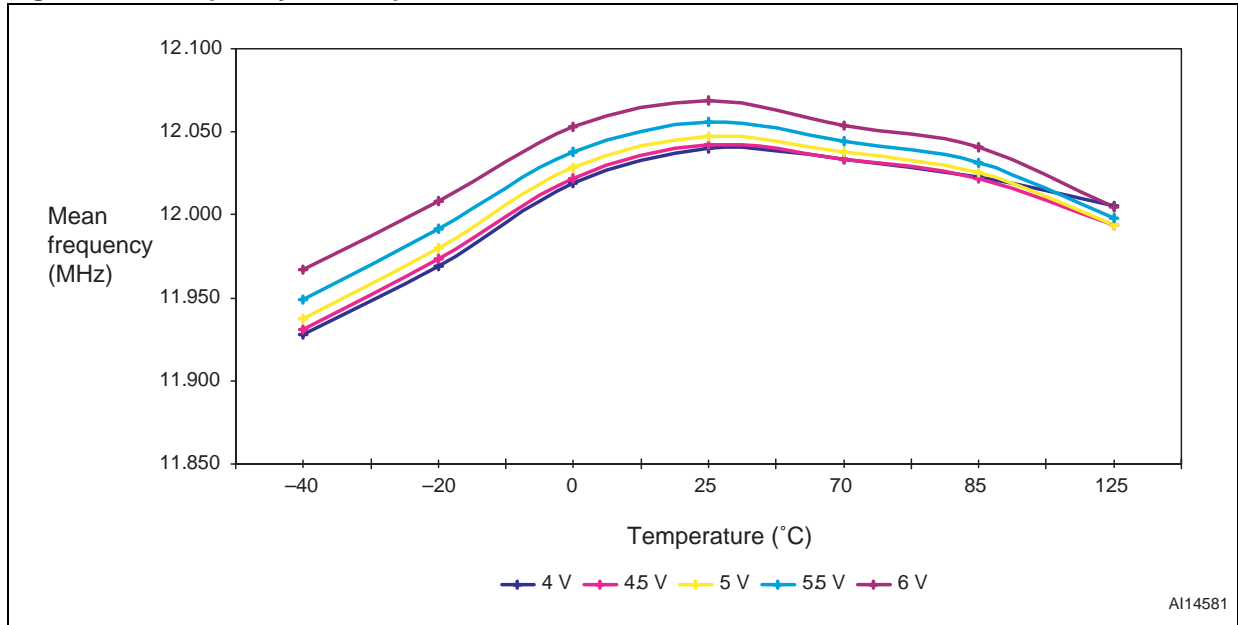
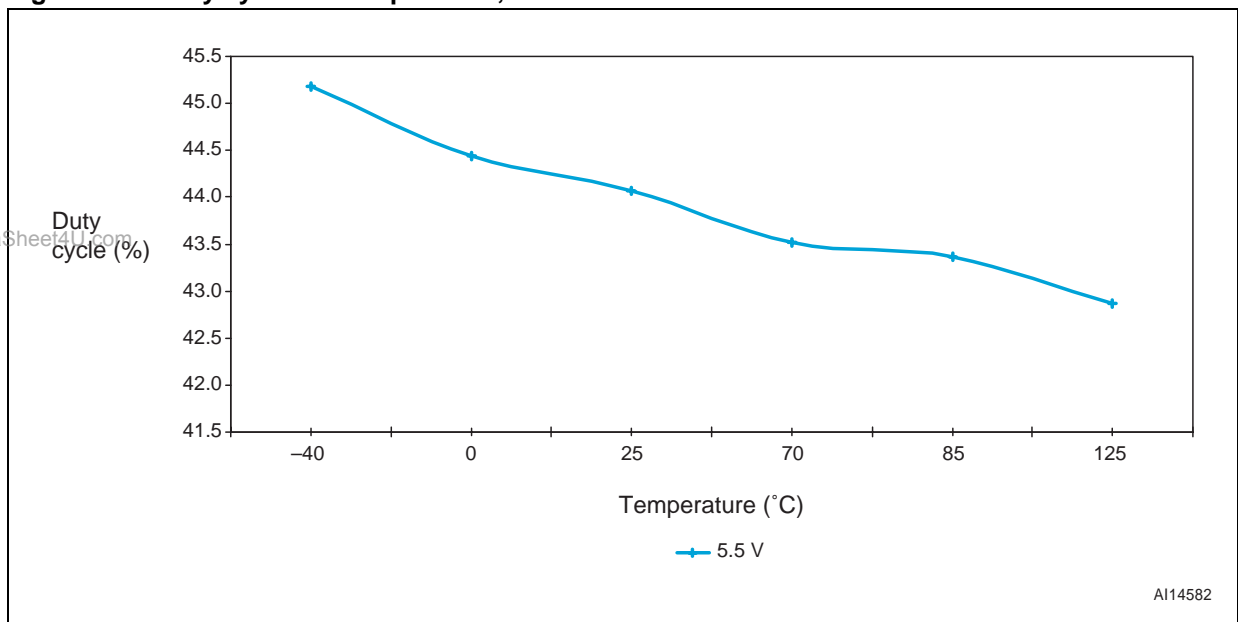**Figure 4.   Duty cycle vs. temperature, STCL1120**

Figure 5. **Active supply current vs. temperature, STCL1120**
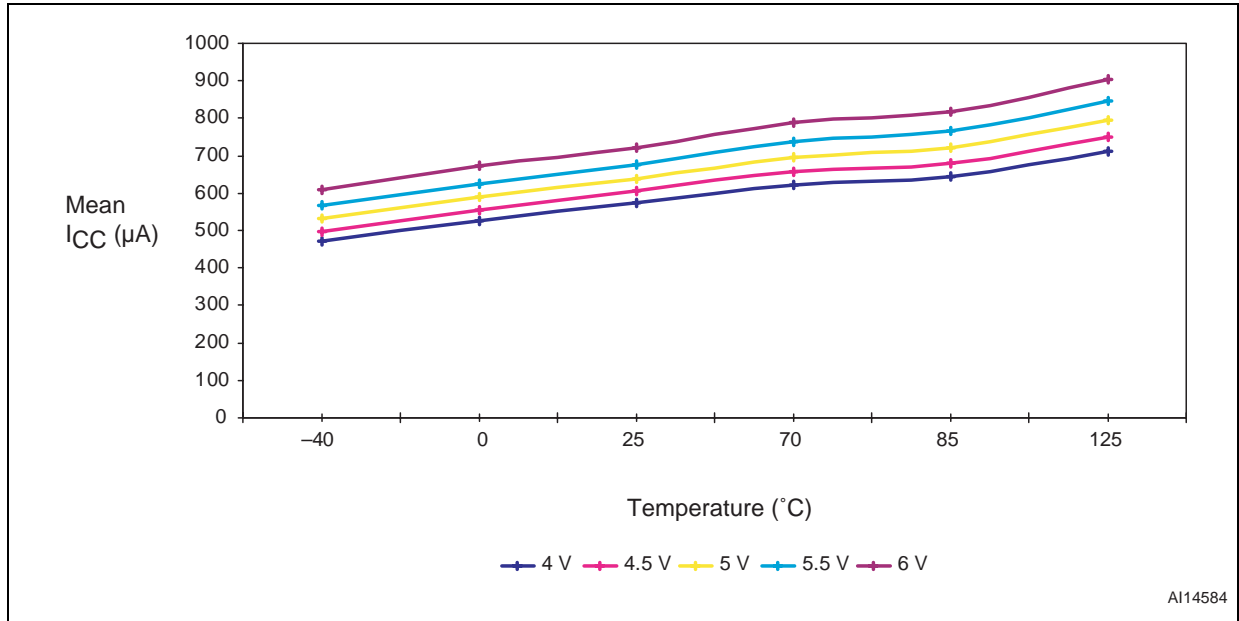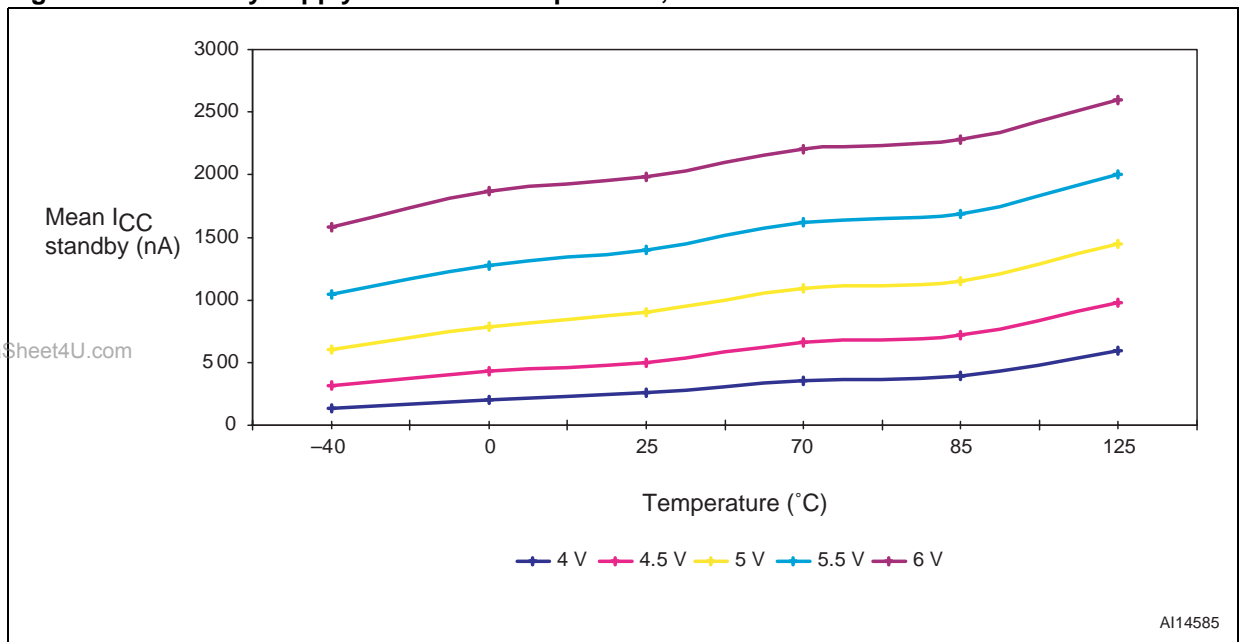

Figure 6. **Standby supply current vs. temperature, STCL1120**
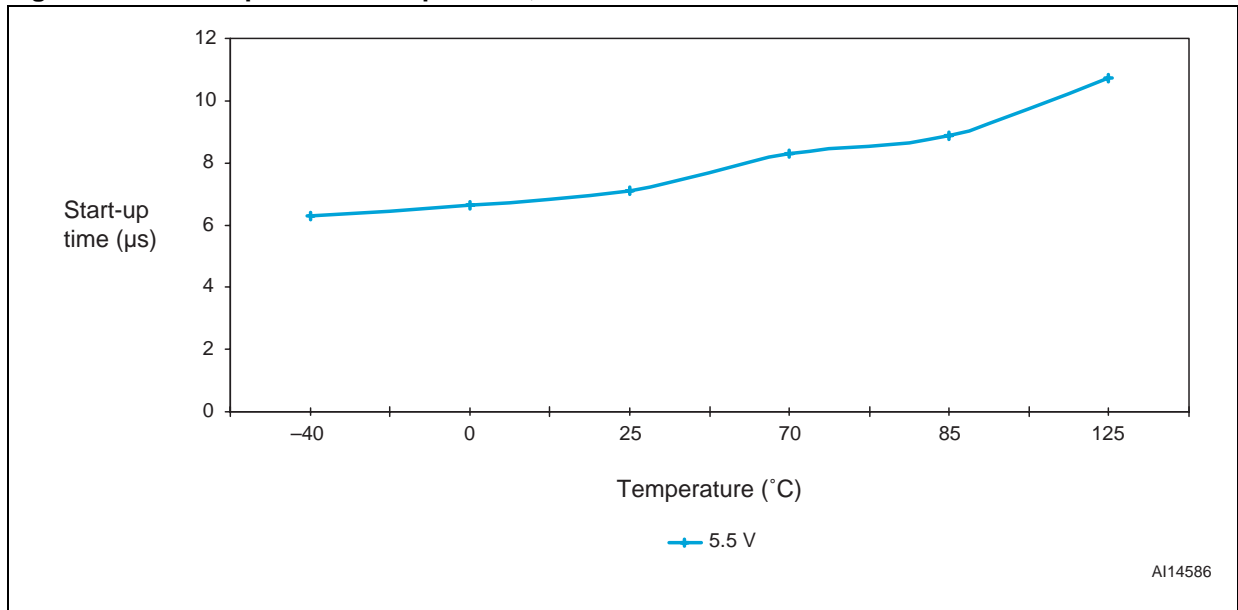
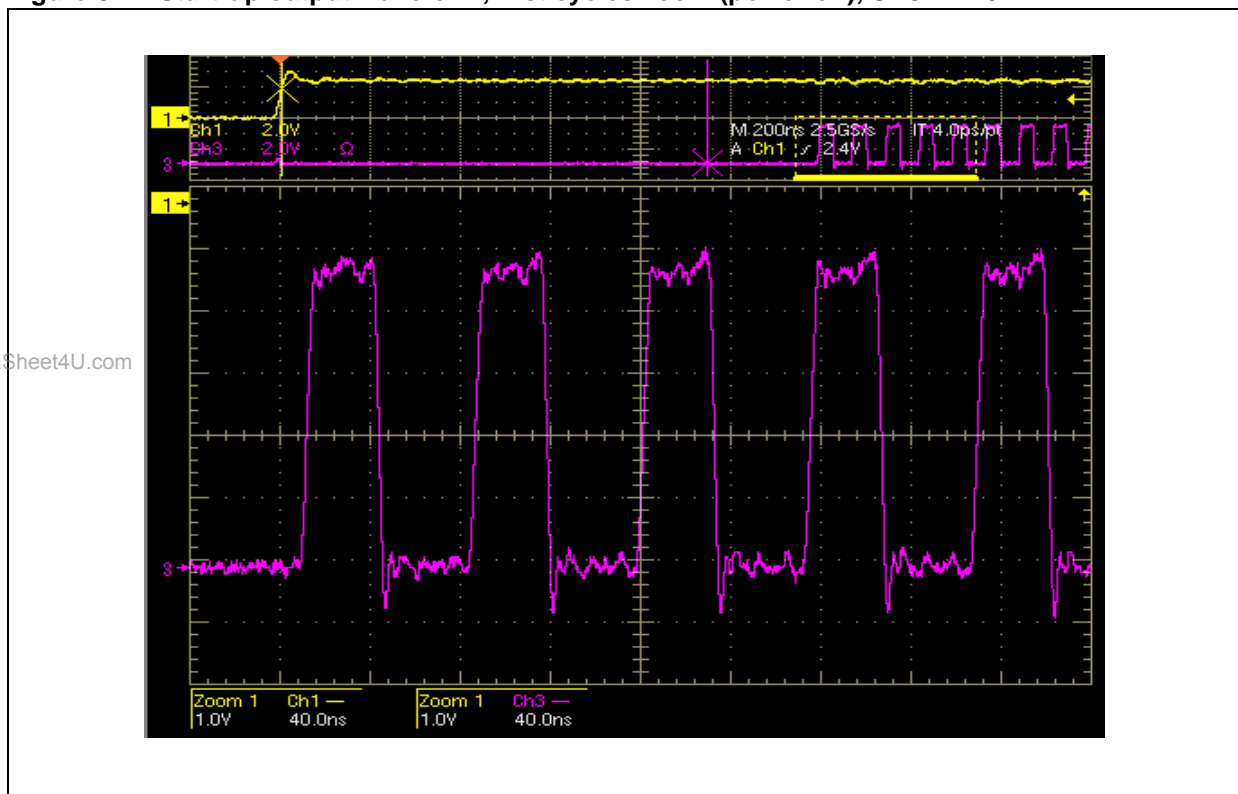**Figure 7.   Start-up time vs. temperature, STCL1120**

Figure 8.   Start-up output waveform, first cycles zoom (power-on), STCL1120

7　　Package details SOT23-5L

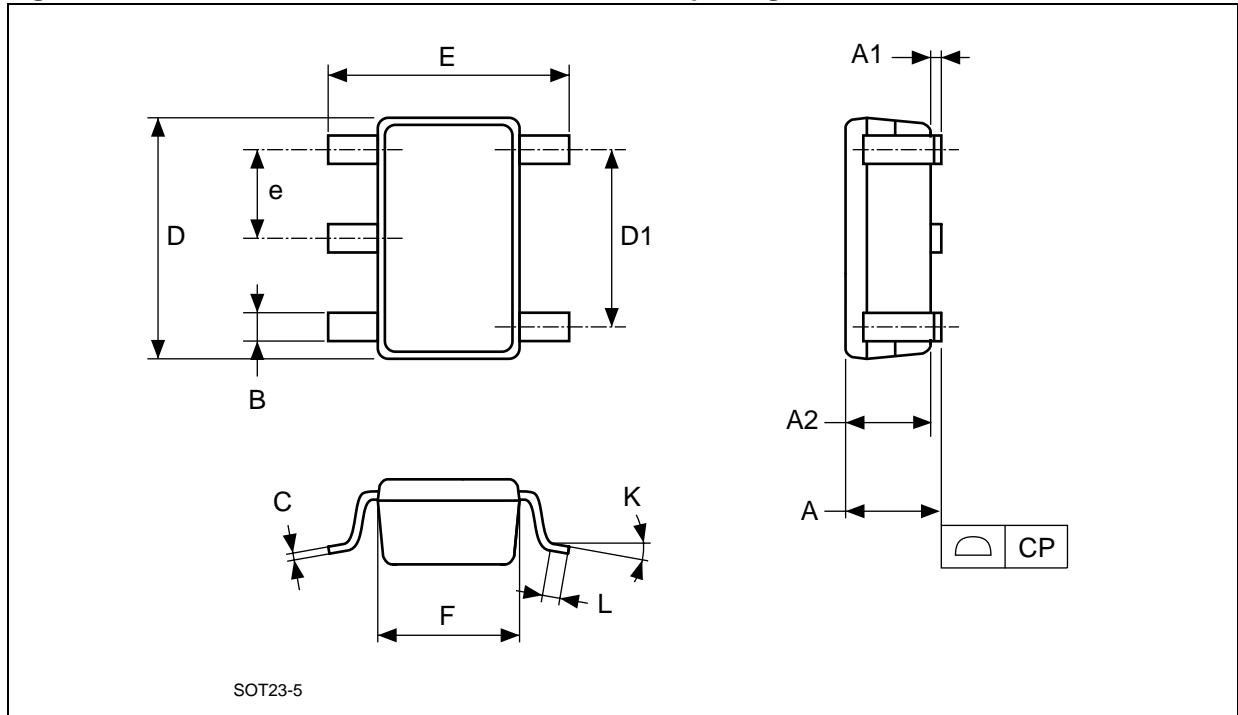**Figure 9.**　**SOT23-5L - 5-lead small outline transistor package outline**

SOT23-5

Table 4.　**SOT23-5L - 5-lead small outline transistor package mechanical data**

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	1.200	0.900	1.450	0.0472	0.0354	0.0571
A1			0.150			0.0059
A2	1.050	0.900	1.300	0.0413	0.0354	0.0512
B	0.400	0.350	0.500	0.0157	0.0138	0.0197
C	0.150	0.090	0.200	0.0059	0.0035	0.0079
D	2.900	2.800	3.000	0.1142	0.1102	0.1181
D1	1.900			0.0748		
E	2.800	2.600	3.000	0.1102	0.1024	0.1181
e	0.950			0.0374		
F	1.600	1.500	1.750	0.0630	0.0591	0.0689
K		0	10		0	10
L	0.350	0.100	0.600	0.0138	0.0039	0.0236

8   Part numbering

Table 5.   Ordering information scheme

| | STCL | 1 | 120 | Y | B | F | C | WY | 5 |

Device type (Root Part Number)

Product family

1 = Single frequency, fixed

Frequency

100 = 10.0 MHz

120 = 12.0 MHz

160 = 16.0 MHz

Operating voltage

Y = 4.5 to 5.5 V

Accuracy

B = ±1.5%

Chip enable

F = Single chip enable, active high, no pull

Disable mode

C = Additional 32 cycles, output low in disable, skip
      16 cycles at start-up, output low during that

Package

WY = SOT23-5L

Temperature range

5 = −20 to +85 °C

Note: *Contact local ST sales office for availability of other product options (chip enable active high*
               or low, with or without internal pull-up or pull-down, possibility of various disable modes,
               start-up procedures, output low or in high-impedance when disabled, etc.).

9 Revision history

Table 6.   Document revision history

Date	Revision	Changes
26-Mar-2007	0.1	Initial release.
04-May-2007	1	Parameters update in *Table 3*.
07-Jun-2007	1.0.1	Typing error corrected.
19-Feb-2008	2	Document reformatted, updated title, *Features*, *Description*, *Table 2*, *Table 3*, *Table 5*, *Figure 2* to *Figure 8*.

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