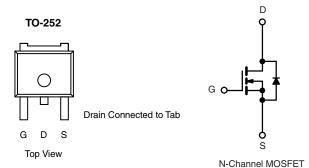


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Vishay Siliconix

# Automotive N-Channel 50 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	50		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.011		
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.015		
I <sub>D</sub> (A)	50		
Configuration	Single		



#### **FEATURES**

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC
- AEC-Q101 Qualifiedd



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD50N05-11L-GE3

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		$V_{DS}$	50	.,,		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V		
Continuous Drain Current	T <sub>C</sub> = 25 °C <sup>a</sup>	I <sub>D</sub>	50			
	T <sub>C</sub> = 125 °C		32			
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	50	Α		
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	200			
Single Pulse Avalanche Energy	L = 0.1 mH	I <sub>AS</sub>	45			
Single Pulse Avalanche Current	L=0.11IIH	E <sub>AS</sub>	101	mJ		
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	- P <sub>D</sub>	75	W		
	T <sub>C</sub> = 125 °C		25	] vv		
Operating Junction and Storage Temperature Range	,	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 175	°C		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	60	°C/W	
Junction-to-Case (Drain)	·		2.0	C/VV	

### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		50	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \mu A$		2.0	2.5	v
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$		-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 50 V	-	-	1.0	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 50 V, T <sub>J</sub> = 125 °C	-	-	50	μΑ
		$V_{GS} = 0 V$	V <sub>DS</sub> = 50 V, T <sub>J</sub> = 175 °C	-	-	250	1
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	$V_{DS} \ge 5 V$	50	-	-	Α
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 45 A	-	0.009	0.011	Ω
Drain-Source On-State Resistance <sup>a</sup>	В	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 45 A, T <sub>J</sub> = 125 °C	-	-	0.020	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 45 A, T <sub>J</sub> = 175 °C	=.	-	0.024	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 45 A	-	-	0.015	
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		-	58	-	S
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			-	1685	2106	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{GS} = 0 \text{ V}$ $V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$		345	430	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	]		=.	144	180	1
Total Gate Charge <sup>c</sup>	Qg			-	34.6	52	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$V_{DS} = 25 \text{ V}, I_D = 43 \text{ A}$	-	5.5	9	nC
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	9.1	14	
Gate Resistance	Rg	f = 1 MHz		1.3	2.6	3.9	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			=.	8.5	13	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD} = 25 \text{ V}, \text{ R}_L = 0.6 \Omega$ $I_D \cong 43 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$		=.	11.5	18	- ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	22.5	34	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	7.5	12	
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>						
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	200	Α
Forward Voltage	$V_{SD}$	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 V		-	0.95	1.5	V

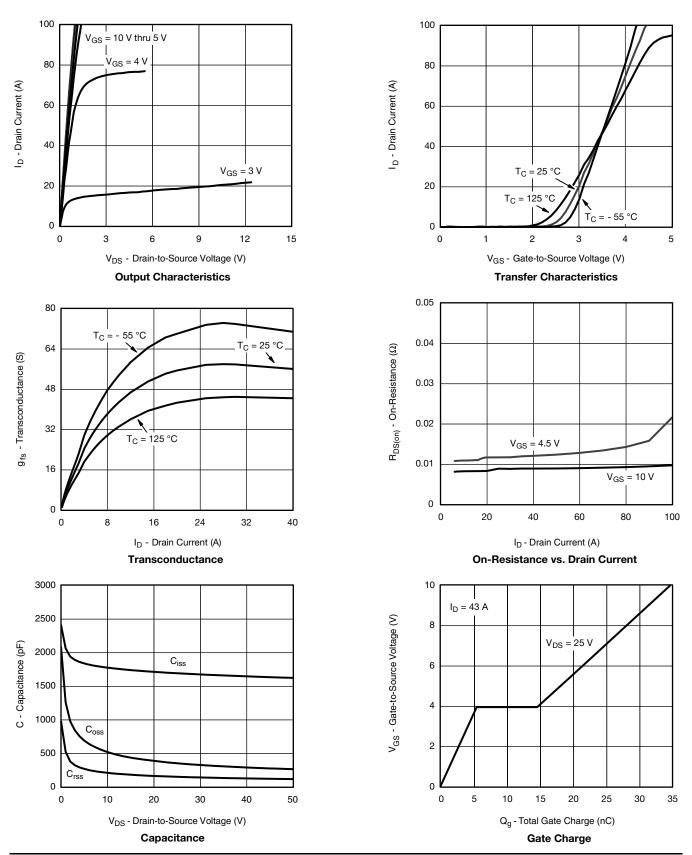
### Notes

- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

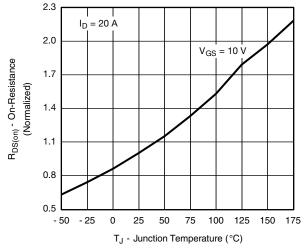


### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

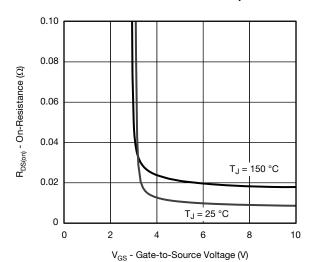




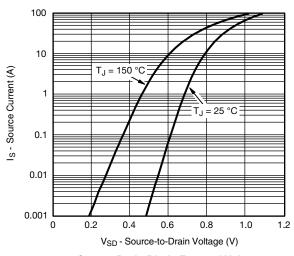
### **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



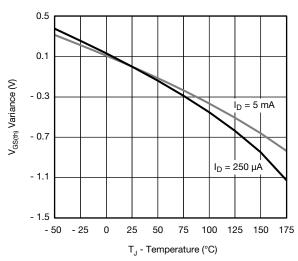
#### **On-Resistance vs. Junction Temperature**



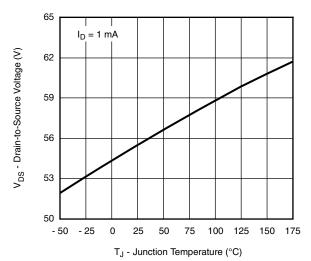
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage



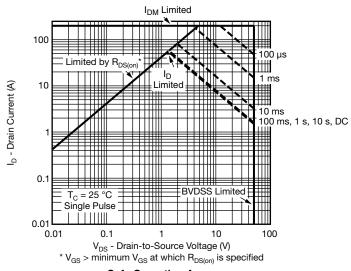
Threshold Voltage



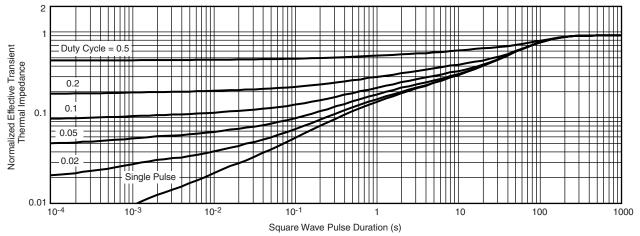
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** ( $T_A = 25$ °C, unless otherwise noted)



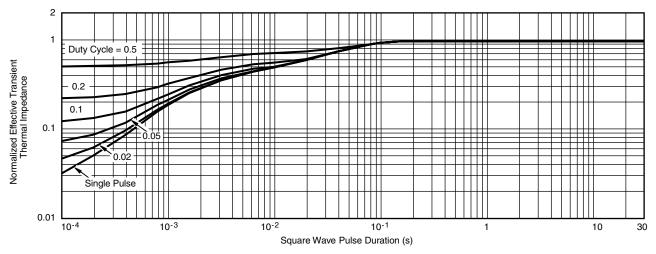
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

- The characteristics shown in the two graphs
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

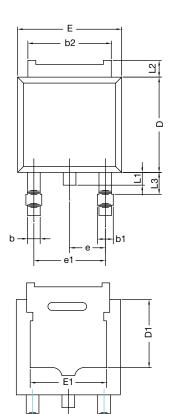
are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

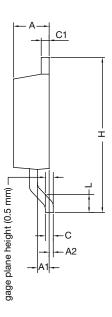
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### **TO-252AA CASE OUTLINE**





	MILLIN	IETERS	INCHES		
DIM.	MIN.	MAX.	MIN.	MAX.	
Α	2.21	2.38	0.087	0.094	
A1	0.89	1.14	0.035	0.045	
A2	0.030	0.127	0.001	0.005	
b	0.71	0.88	0.028	0.035	
b1	0.76	1.14	0.030	0.045	
b2	5.23	5.44	0.206	0.214	
С	0.46	0.58	0.018	0.023	
C1	0.46	0.58	0.018	0.023	
D	5.97	6.22	0.235	0.245	
D1	4.10	4.45	0.161	0.175	
Е	6.48	6.73	0.255	0.265	
E1	4.49	5.50	0.177	0.217	
е	2.28	BSC	0.090 BSC		
e1	4.57	BSC	0.180 BSC		
Η	9.65	10.41	0.380	0.410	
L	1.40	1.78	0.055	0.070	
L1	0.64	1.02	0.025	0.040	
L2	0.89	1.27	0.035	0.050	
L3	1.15	1.52	0.040	0.060	
ECN: T11-0110-Rev. L, 18-Apr-11 DWG: 5347					

#### Note

· Dimension L3 is for reference only.

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### **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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