# 3.3V CMOS 9-BIT BUS-INTERFACE FLIP-FLOP WITH 3-STATE OUTPUTS AND 5 VOLT TOLERANT I/O

**IDT74LVC823A**

## FEATURES:

- **0.5 MICRON CMOS Technology**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Vcc = 3.3V ± 0.3V, Normal Range**
- **Vcc = 2.7V to 3.6V, Extended Range**
- **CMOS power levels (0.4µ W typ. static)**
- **Rail-to-rail output swing for increased noise margin**
- **All inputs, outputs, and I/O are 5V tolerant**
- **Supports hot insertion**
- **Available in SSOP, QSOP, and TSSOP packages**

## DRIVE FEATURES:

- **High Output Drivers: ±24mA**
- **Reduced system switching noise**

## APPLICATIONS:

- **3.3V high speed systems**
- **3.3V and lower voltage computing systems**

## DESCRIPTION:

The LVC823A 9-bit bus-interface flip-flop is built using advanced dual metal CMOS technology. The LVC823A device is designed specifically for driving highly capacitive or relatively low-impedance loads. The device is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

With the clock-enable ($\overline{CLKEN}$) input low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high disables the clock buffer, latching the outputs. This device has noninverting data (D) inputs. Taking the clear ($\overline{CLR}$) input low causes the nine Q outputs to go low, independently of the clock.

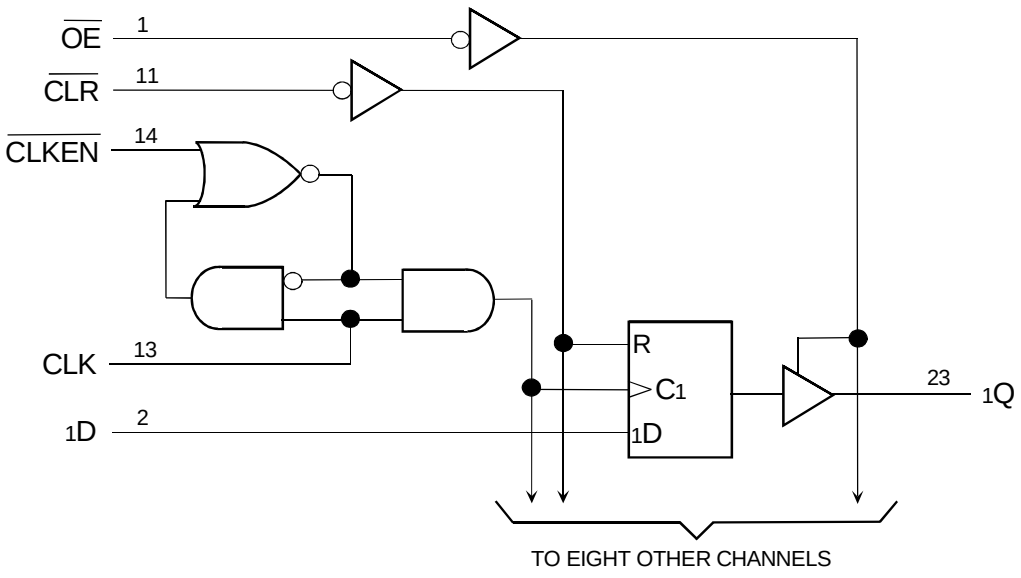
A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low logic levels) or a high-impedance state. $\overline{OE}$ does not affect internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

The LVC823A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

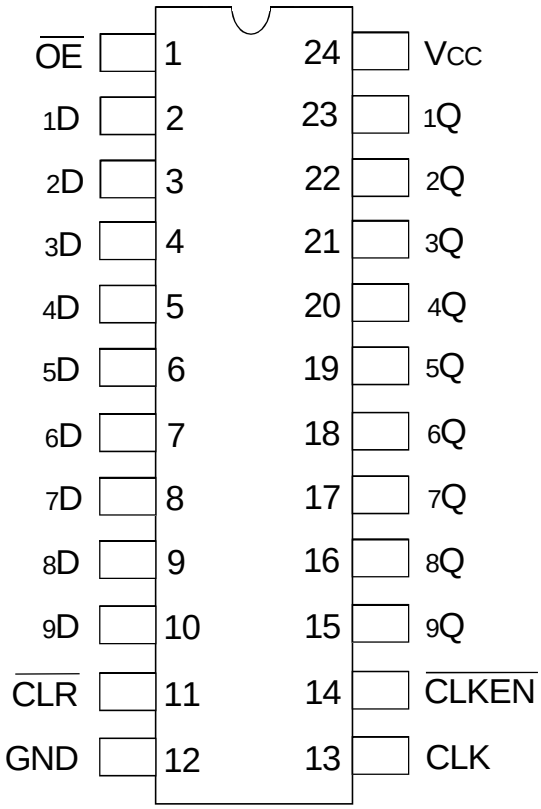
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to Vcc through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**SSOP/ QSOP/ TSSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +6.5 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –50 to +50 | mA |
| $I_{IK}$<br>$I_{OK}$ | Continuous Clamp Current,<br>$V_I < 0$ or $V_O < 0$ | –50 | mA |
| $I_{CC}$<br>$I_{SS}$ | Continuous Current through each<br>$V_{CC}$ or GND | ±100 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, F = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 5.5 | 8 | pF |
| $C_{I/O}$ | I/O Port Capacitance | $V_{IN}$ = 0V | 6.5 | 8 | pF |

**NOTE:**
1. As applicable to the device type.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input (Active LOW) |
| CLK | Clock Input |
| $\overline{CLKEN}$ | Clock Enable Input (Active LOW) |
| $\overline{CLR}$ | Clear Input (Active LOW) |
| xD | Data Inputs |
| xQ | Data Outputs |

## FUNCTION TABLE (EACH FLIP-FLOP)(1)

| Inputs | | | | | Outputs |
|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{CLKEN}$ | CLK | xD | xQ |
| L | L | X | X | X | L |
| L | H | L | ↑ | H | H |
| L | H | L | ↑ | L | L |
| L | H | H | X | X | Q(2) |
| H | X | X | X | X | Z |

**NOTES:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH transition
2. Output level before indicated steady-state input conditions were established.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: $T_A$ = –40°C to +85°C

| Symbol | Parameter | Test Conditions | | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | 1.7 | — | — | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2 | — | — | |
| $V_{IL}$ | Input LOW Voltage Level | $V_{CC}$ = 2.3V to 2.7V | | — | — | 0.7 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | — | — | 0.8 | |
| $I_{IH}$<br>$I_{IL}$ | Input Leakage Current | $V_{CC}$ = 3.6V | $V_I$ = 0 to 5.5V | — | — | ±5 | µA |
| $I_{OZH}$<br>$I_{OZL}$ | High Impedance Output Current (3-State Output pins) | $V_{CC}$ = 3.6V | $V_O$ = 0 to 5.5V | — | — | ±10 | µA |
| $I_{OFF}$ | Input/Output Power Off Leakage | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 5.5V | | — | — | ±50 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = 2.3V, $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $V_H$ | Input Hysteresis | $V_{CC}$ = 3.3V | | — | 100 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V | $V_{IN}$ = GND or $V_{CC}$ | — | — | 10 | µA |
| | | | $3.6 \leq V_{IN} \leq 5.5V$(2) | — | — | 10 | |
| $\Delta I_{CC}$ | Quiescent Power Supply Current Variation | One input at $V_{CC}$ - 0.6V, other inputs at $V_{CC}$ or GND | | — | — | 500 | µA |

**NOTES:**
1. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
2. This applies in the disabled state only.

## OUTPUT DRIVE CHARACTERISTICS

| Symbol | Parameter | Test Conditions(1) | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OH}$ = – 0.1mA | $V_{CC}$ – 0.2 | — | V |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 6mA | 2 | — | |
| | | $V_{CC}$ = 2.3V | $I_{OH}$ = – 12mA | 1.7 | — | |
| | | $V_{CC}$ = 2.7V | | 2.2 | — | |
| | | $V_{CC}$ = 3V | | 2.4 | — | |
| | | $V_{CC}$ = 3V | $I_{OH}$ = – 24mA | 2.2 | — | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.3V to 3.6V | $I_{OL}$ = 0.1mA | — | 0.2 | V |
| | | $V_{CC}$ = 2.3V | $I_{OL}$ = 6mA | — | 0.4 | |
| | | | $I_{OL}$ = 12mA | — | 0.7 | |
| | | $V_{CC}$ = 2.7V | $I_{OL}$ = 12mA | — | 0.4 | |
| | | $V_{CC}$ = 3V | $I_{OL}$ = 24mA | — | 0.55 | |

**NOTE:**
1. $V_{IH}$ and $V_{IL}$ must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate $V_{CC}$ range. $T_A$ = – 40°C to + 85°C.

## OPERATING CHARACTERISTICS, $V_{CC}$ = 3.3V ± 0.3V, $T_A$ = 25°C

| Symbol | Parameter | Test Conditions | Typical | Unit |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance per Flip-Flop Outputs enabled | $C_L$ = 0pF, f = 10Mhz | 59 | pF |
| $C_{PD}$ | Power Dissipation Capacitance per Flip-Flop Outputs disabled | | 46 | |

## SWITCHING CHARACTERISTICS(1)

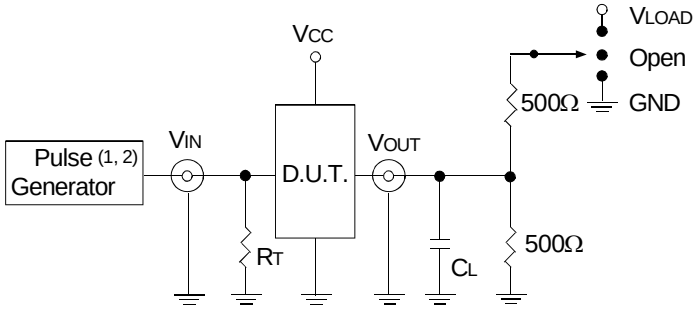
| Symbol | Parameter | Vcc = 2.7V | | Vcc = 3.3V ± 0.3V | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $f_{MAX}$ | | 150 | — | 150 | — | MHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to xQ | — | 8.9 | 1.4 | 8 | ns |
| $t_{PHL}$ | Propagation Delay<br>$\overline{CLR}$ to xQ | — | 8.8 | 2.5 | 7.9 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>$\overline{OE}$ to xQ | — | 8.3 | 1.6 | 7.2 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time<br>$\overline{OE}$ to xQ | — | 7.1 | 1.1 | 6 | ns |
| $t_W$ | Pulse Duration, $\overline{CLR}$ LOW | 3.3 | — | 3.3 | — | ns |
| $t_W$ | Pulse Duration, CLK HIGH or LOW | 3.3 | — | 3.3 | — | ns |
| $t_{SU}$ | Set-up Time, $\overline{CLR}$ inactive before CLK↑ | 1 | — | 1 | — | ns |
| $t_{SU}$ | Set-up Time, data before CLK↑ | 1.3 | — | 1.3 | — | ns |
| $t_{SU}$ | Set-up Time, $\overline{CLKEN}$ LOW before CLK↑ | 1.8 | — | 1.8 | — | ns |
| $t_H$ | Hold Time, data after CLK↑ | 2 | — | 2 | — | ns |
| $t_H$ | Hold Time, $\overline{CLKEN}$ LOW after CLK↑ | 1.3 | — | 1.3 | — | ns |
| $t_{SK(o)}$ | Output Skew(2) | — | — | — | 1 | ns |

**NOTES:**
1. See TEST CIRCUITS AND WAVEFORMS. $T_A$ = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

# TEST CIRCUITS AND WAVEFORMS

## TEST CONDITIONS

| Symbol | $V_{CC}^{(1)}$=3.3V±0.3V | $V_{CC}^{(1)}$=2.7V | $V_{CC}^{(2)}$=2.5V±0.2V | Unit |
|---|---|---|---|---|
| $V_{LOAD}$ | 6 | 6 | 2 x Vcc | V |
| $V_{IH}$ | 2.7 | 2.7 | Vcc | V |
| $V_T$ | 1.5 | 1.5 | Vcc / 2 | V |
| $V_{LZ}$ | 300 | 300 | 150 | mV |
| $V_{HZ}$ | 300 | 300 | 150 | mV |
| $C_L$ | 50 | 50 | 30 | pF |




LVC Link

***Test Circuit for All Outputs***

**DEFINITIONS:**

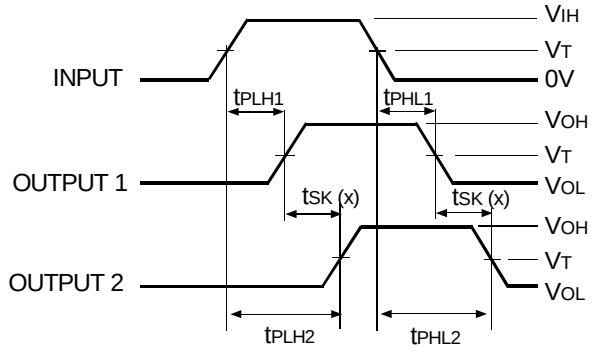
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

**NOTES:**

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; $t_F$ ≤ 2ns; $t_R$ ≤ 2ns.

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | $V_{LOAD}$ |
| Disable High<br>Enable High | GND |
| All Other Tests | Open |




$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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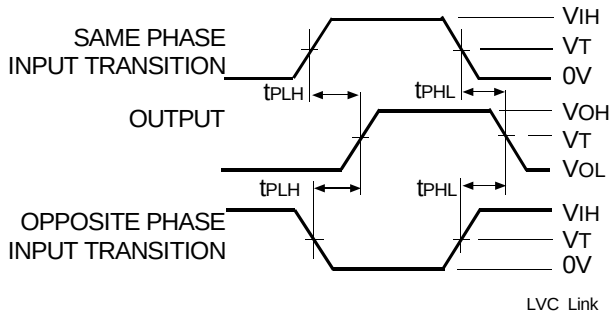
***Output Skew - $t_{SK(x)}$***

**NOTES:**

1. For $t_{SK}$(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For $t_{SK}$(b) OUTPUT1 and OUTPUT2 are in the same bank.

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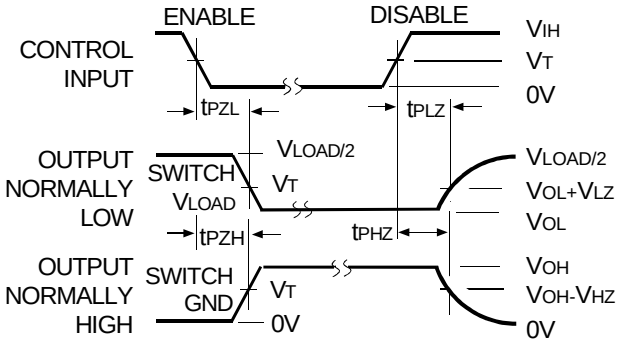
***Propagation Delay***

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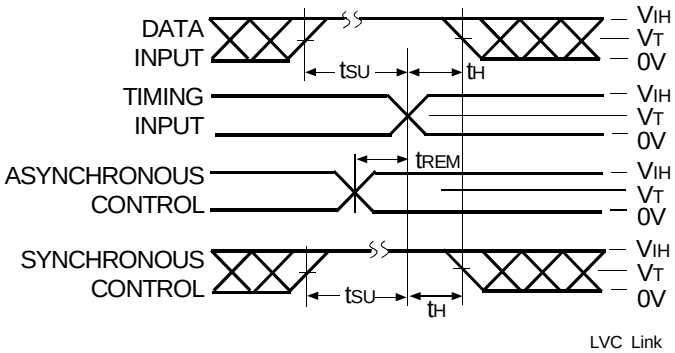
***Enable and Disable Times***

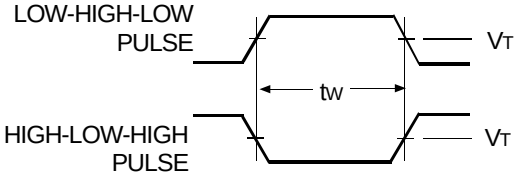
**NOTE:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.




LVC Link

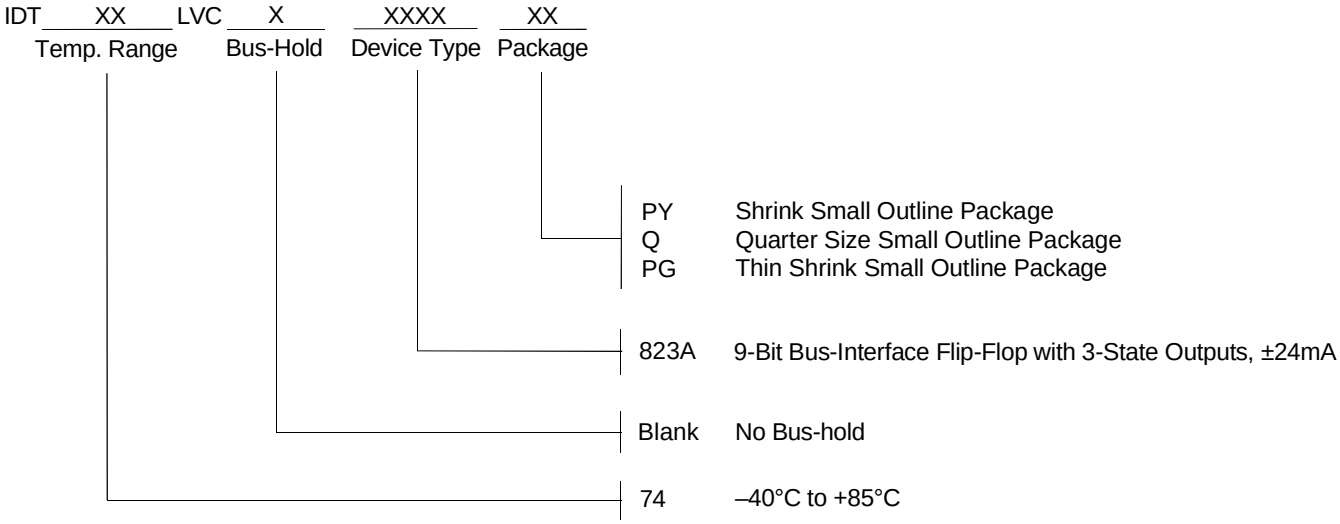
***Set-up, Hold, and Release Times***




LVC Link

***Pulse Width***

## ORDERING INFORMATION

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