

DESCRIPTION

The HYM591000A is a 1M x 9-bit Fast page mode CMOS DRAM module consisting of two HY514400 and one HY531000 in 20/26 pin SOJ on a 30 pin glass-epoxy printed circuit board. 0.22 μ F decoupling capacitor is mounted for each DRAM.

The HYM591000AM is a Tin-Lead plated socket type Single In-line Memory Module suitable for easy interchange and addition of 1M byte memory.

FEATURES

- Low power dissipation
Max. CMOS standby 16.5mW
Max. TTL standby 33.0mW
Max. operating

Speed	Power
70	1.46W
80	1.30W

- Single power supply of 5V $\pm$ 10%
- TTL compatible inputs and outputs
- Fast access time

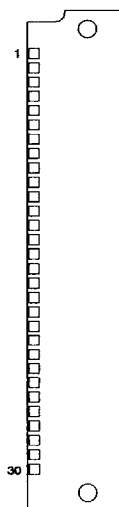
Speed	tRAC	tCAC	tPC
70	70ns	20ns	50ns
80	80ns	25ns	50ns

- Fast page mode operation
- CAS-before-RAS, RAS-only, Hidden refresh
- 1024 refresh cycles / 16ms

PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
PCAS	CAS for Parity
WE	Write Enable
A0-A9	Address Input
DQ0-DQ7	Data Input/Output
PD	Data In for Parity
PQ	Data Out for Parity
VCC	Power (+5V)
VSS	Ground

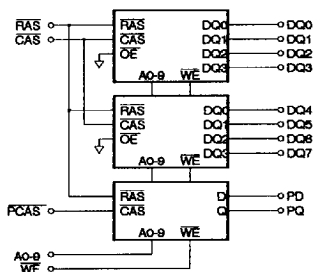
PIN CONNECTION



PIN NAME

#	NAME
1	VCC
2	CAS
3	DQ0
4	A0
5	A1
6	DQ1
7	A2
8	A3
9	VSS
10	DQ2
11	A4
12	A5
13	DQ3
14	A6
15	A7
16	DQ4
17	A8
18	A9
19	NC
20	DQ5
21	WE
22	VSS
23	DQ6
24	NC
25	DQ7
26	PQ
27	RAS
28	PCAS
29	PD
30	VCC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.94	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC + 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
I _I	Input Leakage Current (Any Input Pin)	VSS ≤ V _{IN} ≤ VCC + 1.0, All other pins not under test = VSS		-20	20	μA	
I _{LO}	Output Leakage Current (High Impedance State)	VSS ≤ V _{OUT} ≤ VCC, RAS & CAS at V _{IH}		-10	10	μA	
ICC1	VCC Supply Current, Operating	t _{RC} = t _{RC} (min.)	70 80	-	265 235	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at V _{IH} , other inputs ≥ VSS		-	6	mA	
ICC3	VCC Supply Current, RAS-only refresh	t _{RC} = t _{RC} (min.)	70 80	-	265 235	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	t _{PC} = t _{PC} (min.)	70 80	-	215 185	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC - 0.2V		-	3	mA	
ICC6	VCC Supply Current, CAS-before-RAS refresh	t _{RC} = t _{RC} (min.)	70 80	-	265 235	mA	1,3
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA		-	0.4	V	
V _{OH}	Output High Voltage	I _{OH} = -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS = V_{IL} and CAS = V_{IH}.

AC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM591000AM				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	130	-	150	-	ns	
2	tRPC	RAS to CAS Precharge Time	0	-	0	-	ns	
3	tPC	Fast Page Mode Cycle Time	50	-	50	-	ns	
4	tRHCP	RAS Hold Time from CAS Precharge	40	-	45	-	ns	
5	tRAC	Access Time from RAS	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	20	-	25	ns	4,9
7	tAA	Access Time from Column Address	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	45	-	45	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	20	-	25	-	ns	
16	tCSH	CAS Hold Time	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	20	10K	25	10K	ns	
18	tRCD	RAS to CAS Delay	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	55	-	60	-	ns	
27	tRAL	Column Address to RAS Lead Time	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	55	-	60	-	ns	
33	tWP	Write Command Pulse Width	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	20	-	25	-	ns	
35	tCWL	Write Command to CAS Lead Time	20	-	25	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	55	-	60	-	ns	
39	tREF	Refresh Period (1024 cycles)	-	16	-	16	ms	
40	tWCS	Write Command Set-up Time	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

(continued)

#	SYMBOL	PARAMETER	HYM591000AM				UNIT	NOTE
			-70		-80			
			MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	10	-	10	-	ns	
42	tCHR	CAS Hold Time (CBR Cycle)	30	-	30	-	ns	
43	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	ns	
44	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	ns	
45	tWRH	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	ns	

NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition time is measured between V_{IH} and V_{IL} and assumed to be 5ns for all inputs.
3. Refer to the HY514400 and HY531000 data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tr_{CH} or tr_{RH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. tw_{CS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $tw_{CS} \geq tw_{CS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $tr_{CD}(\text{max.})$ limit insures that $tr_{AC}(\text{max.})$ can be met. $tr_{CD}(\text{max.})$ is specified as a reference point only. If tr_{CD} is greater than the specified $tr_{CD}(\text{max.})$ limit, then access time is controlled by tr_{AC} .
10. Operation within the $tr_{AD}(\text{max.})$ limit insures that $tr_{AC}(\text{max.})$ can be met. $tr_{AD}(\text{max.})$ is specified as a reference point only. If tr_{AD} is greater than the specified $tr_{AD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

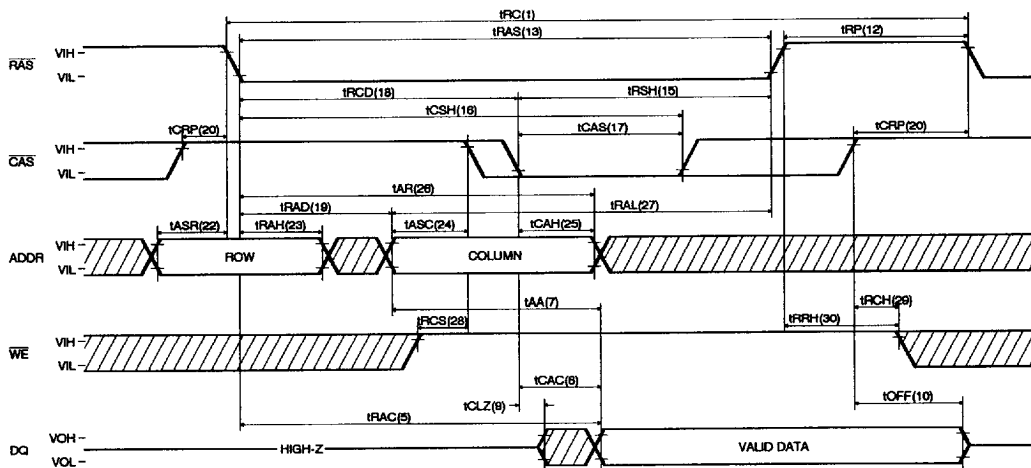
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $f = 1\text{MHz}$, unless otherwise noted.)

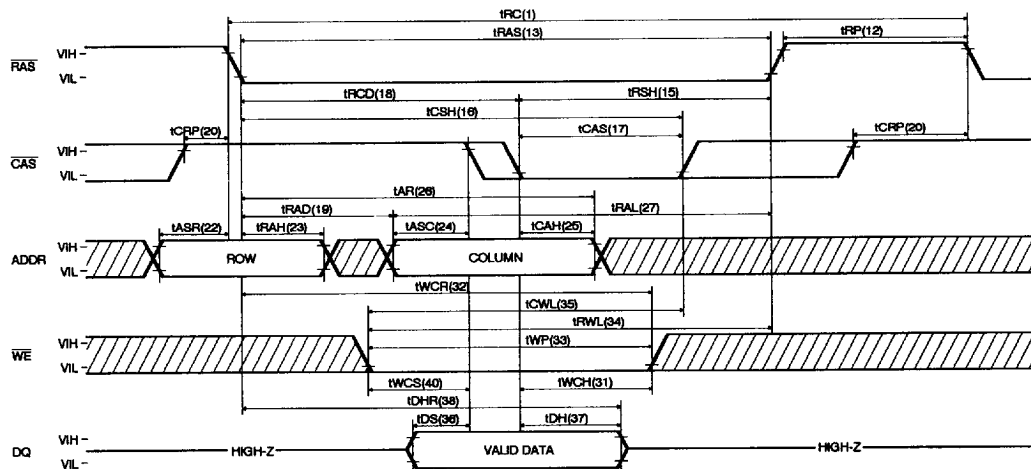
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9, WE, CAS, RAS)	-	25	pF
C_{IN2}	Input Capacitance (PD, PCAS)	-	10	pF
C_{DQ}	I/O Capacitance (DQ0-DQ7)	-	15	pF
C_{PQ}	Output Capacitance (PQ)	-	10	pF

TIMING DIAGRAM

READ CYCLE



EARLY WRITE CYCLE



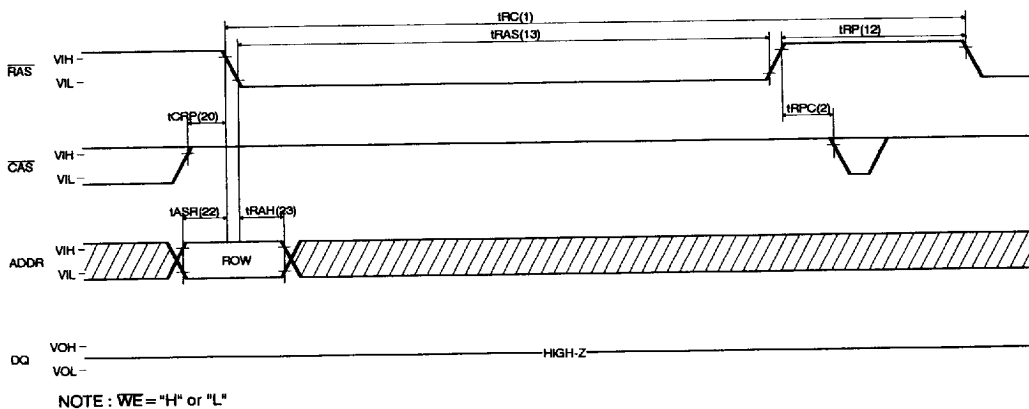
The timing diagram illustrates the relationship between several memory control and data signals over time. The signals shown are:

- RAS**: Row Address Strobe, active low.
- CAS**: Column Address Strobe, active low.
- ADDR**: Memory address bus, alternating between ROW and COLUMN phases.
- WE**: Write Enable, active low.
- DQ**: Data bus, showing VALID DATA periods.

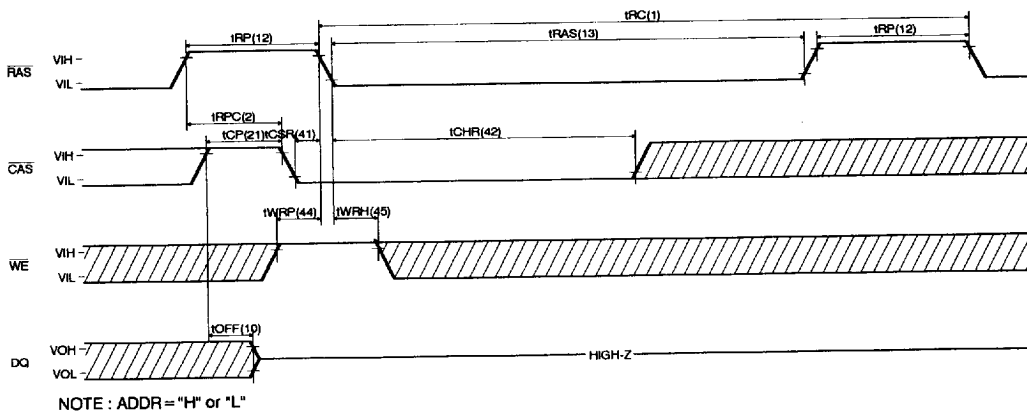
Key timing parameters labeled in the diagram include:

- $t_{RASP}(14)$: RAS pulse width.
- $t_{CRP}(20)$: RAS-to-CAS delay.
- $t_{CD}(19)$: CAS-to-DQ delay.
- $t_{CAS}(17)$: CAS pulse width.
- $t_{CP}(21)$: CAS-to-Data Delay.
- $t_{PC}(3)$: Precharge time.
- $t_{RHCP}(4)$: Refresh Hysteresis Control Pulse width.
- $t_{RS}(15)$: Refresh Strobe pulse width.
- $t_{ICAS}(17)$: Internal CAS delay.
- $t_{IRP}(12)$: Refresh Interval Period.
- $t_{RAD}(19)$: Read Access Delay.
- $t_{IAH}(23)$: Initial Access Hold time.
- $t_{ASC}(24)$: Access Setup time.
- $t_{CAH}(25)$: Column Access Hold time.
- $t_{IASC}(24)$: Internal Access Setup time.
- $t_{ICAH}(25)$: Internal Column Access Hold time.
- $t_{IAL}(27)$: Internal Access Latency.
- $t_{WCS}(40)$: Write Cycle Setup time.
- $t_{ICWL}(35)$: Internal Column Word Line delay.
- $t_{IWCH}(31)$: Internal Write Column Hit delay.
- $t_{IWP}(33)$: Internal Write Pulse width.
- $t_{WCR}(32)$: Write Cycle Recovery time.
- $t_{DHR}(36)$: Data Hold after Refresh time.
- $t_{DS}(30)$: Data Setup time.
- $t_{IDH}(37)$: Internal Data Hold time.
- $t_{IRWL}(34)$: Internal Refresh Word Line delay.

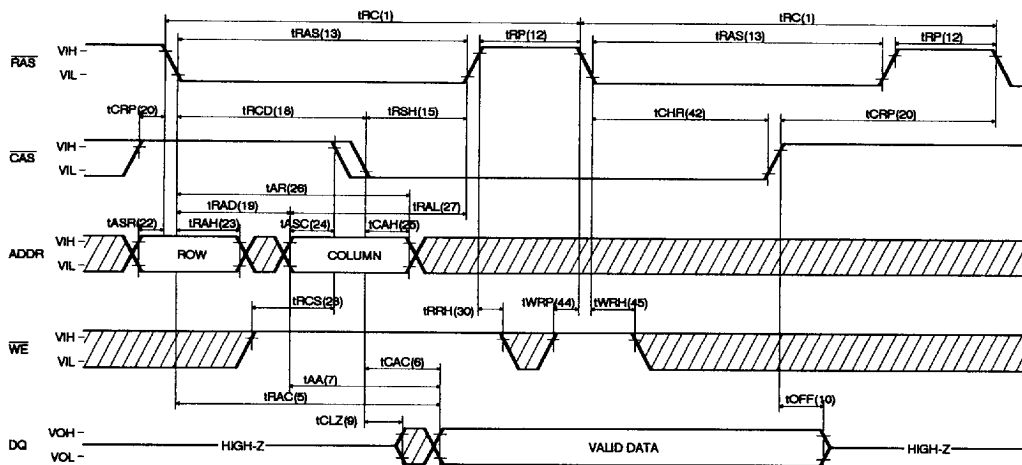
RAS-ONLY REFRESH CYCLE



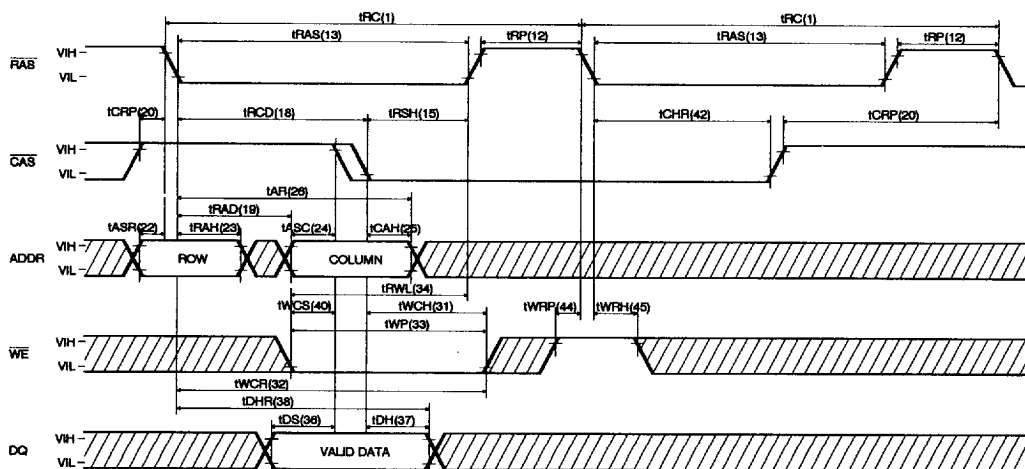
CAS-BEFORE-RAS REFRESH CYCLE



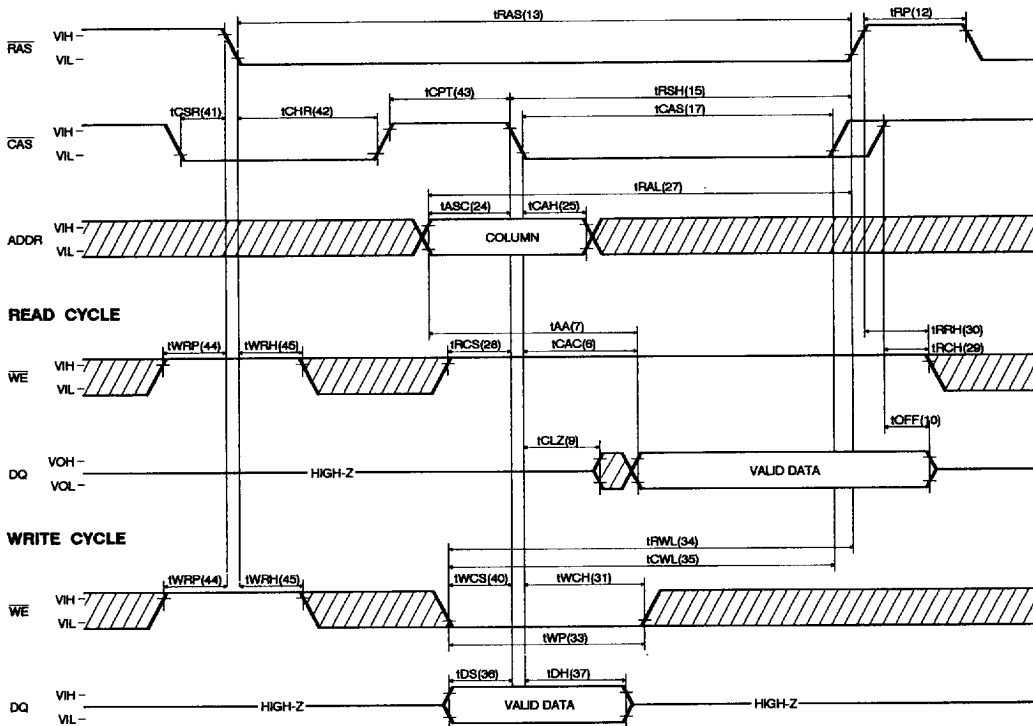
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



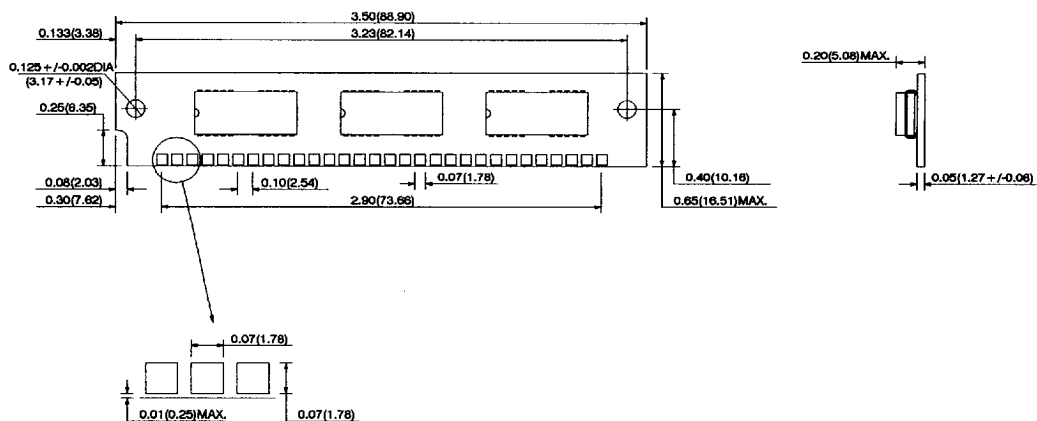
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

30 pin Single In-line Memory Module (M ; Tin-Lead plated)

UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM591000AM	70/80		SIMM	Tin-Lead