

BGF125

SIM Card Interface Filter and ESD Protection

Small Signal Discretes



Never stop thinking

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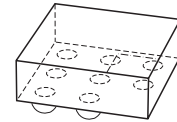
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BGF125

Features

- ESD protection circuit and interface filter for SIM cards
- Reduced line capacitance of 12 pF maximum
- ESD protection according to IEC61000-4-2 for ±15 kV contact discharge on external IOs
- Wafer level package with SnAgCu solder balls
- 400 µm solder ball pitch
- RoHS and WEEE compliant package



WLP-8-10-N-3D



Description

BGF125 is an ESD protection and filtering circuit for SIM card interfaces. All external IOs are protected against ESD pulses of ±15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green lead-free and halogen-free package with a size of only 1.15 mm x 1.15 mm and a total height of 0.6 mm

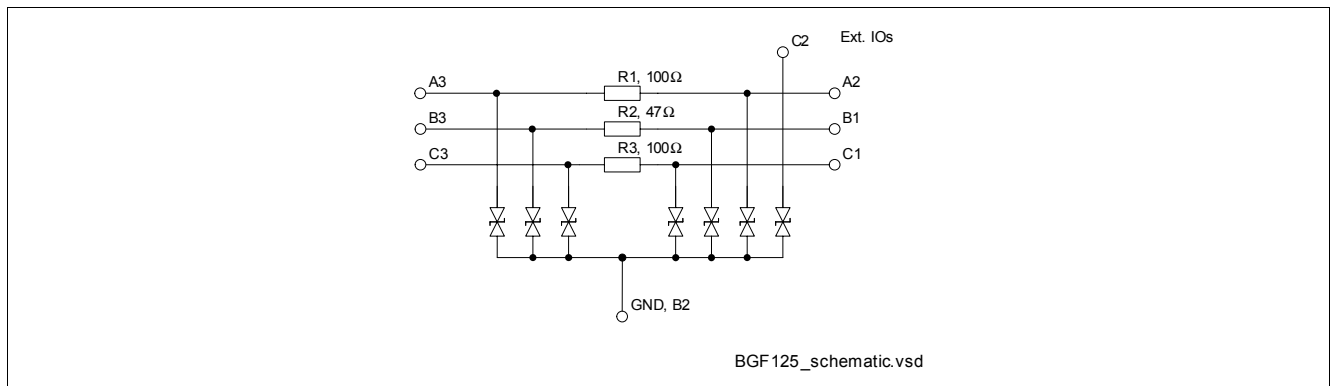


Figure 1 Schematic

Type	Package	Marking	Chip
BGF125	WLP-8-10	25	N0745

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	0	–	5	V	–
Operating temperature range	T_{OP}	-40	–	+85	°C	–
Storage temperature range	T_{STG}	-65	–	+150	°C	–
Summed up input power for all pins	P_{in}	–	–	60	mW	$T_S < 70\text{ °C}$

Electrostatic Discharge According to IEC61000-4-2

Contact discharge at internal pins A3, B3, C3	V_{ESD}	-2	–	2	kV	–
Contact discharge at external pins A2, B1, C1, C2	V_{ESD}	-15	–	15	kV	–

Table 2 Electrical Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistors R_1, R_3	$R_{1,3}$	80	100	120	Ω	–
Resistor R_2	R_2	37.6	47	56.4	Ω	–
Leakage current of ESD protection diodes	I_L	–	1	100	nA	$V = 3\text{ V}$
		–	2	200	nA	$V = 5\text{ V}$
Breakdown voltage of ESD diodes ²⁾	$V_{(BR)}$	–	18.5	–	V	$I_{(BR)} = 1\text{ mA}$
		–	-12.5	–	V	$I_{(BR)} = -1\text{ mA}$
Line capacitance Capacitance of all lines to GND	C_T	8	10	12	pF	$V = 0\text{ V}$

1) at $T_A = 25\text{ }^\circ\text{C}$

2) after snap-back

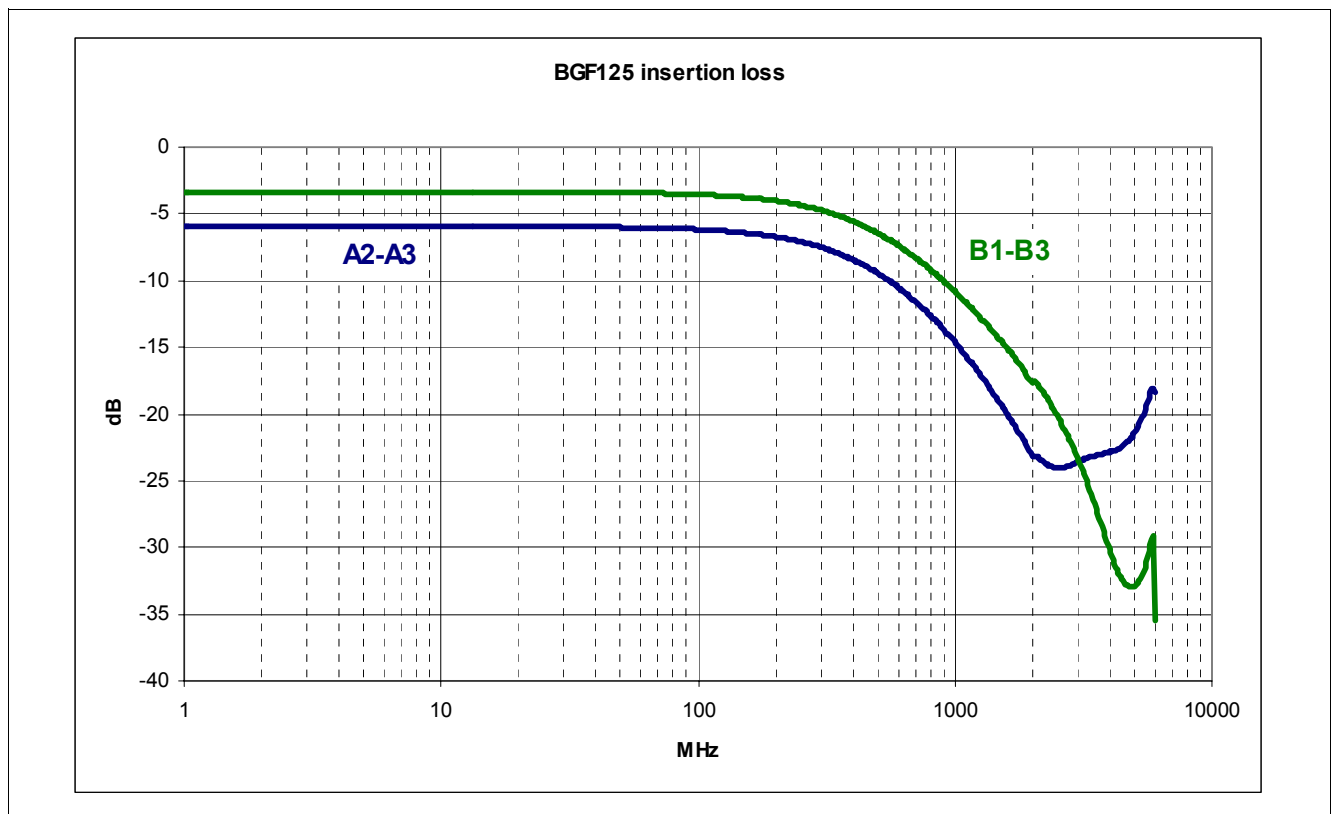


Figure 2 Insertion Loss, $Z_S = Z_L = 50\ \Omega$

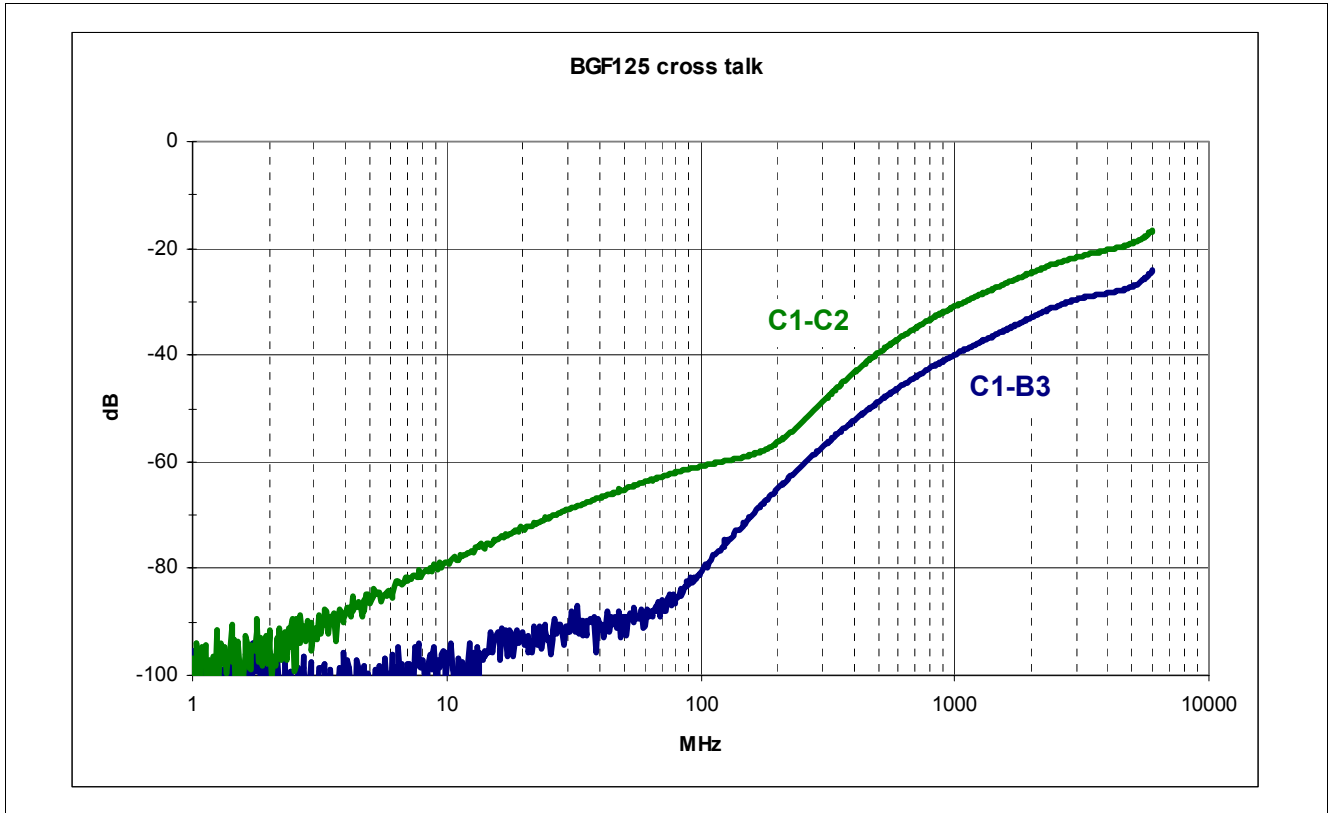


Figure 3 Typical Cross Talk, $Z_s = Z_L = 50 \Omega$

Package Outlines

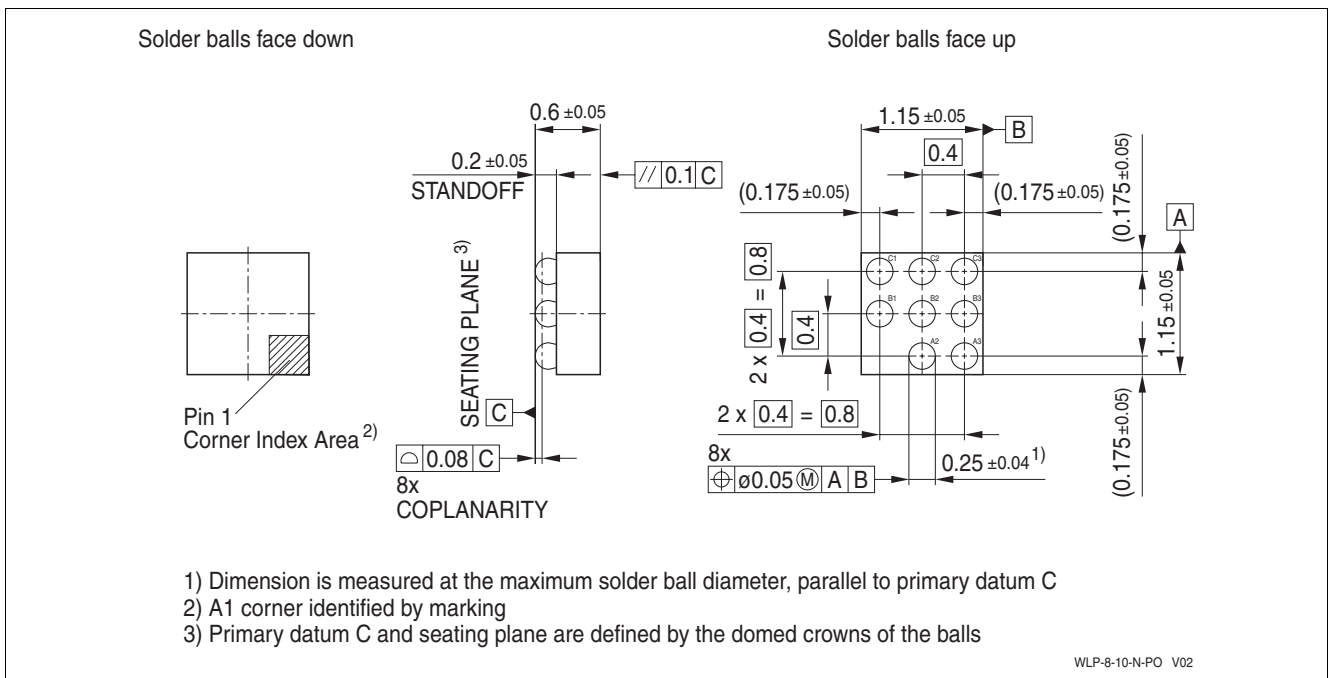


Figure 4 WLP-8-10 (Wafer Level Package)

Footprint

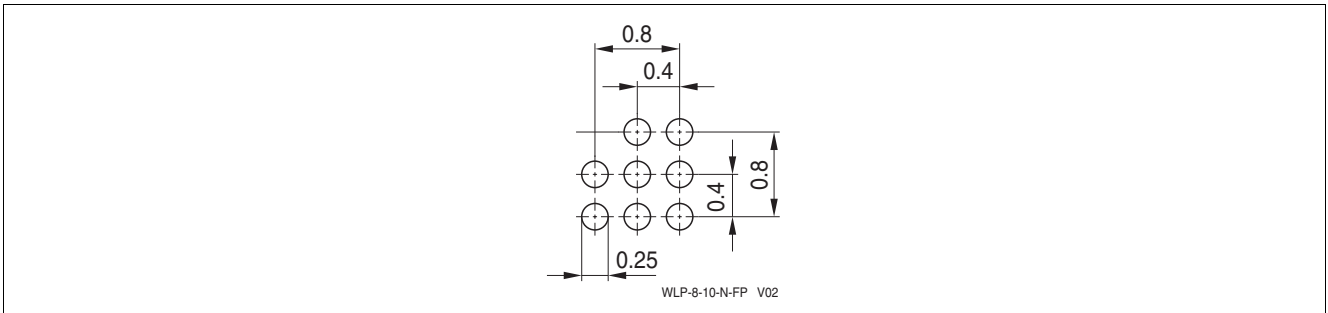


Figure 5 Recommended PCB pad design for reflow soldering

Tape

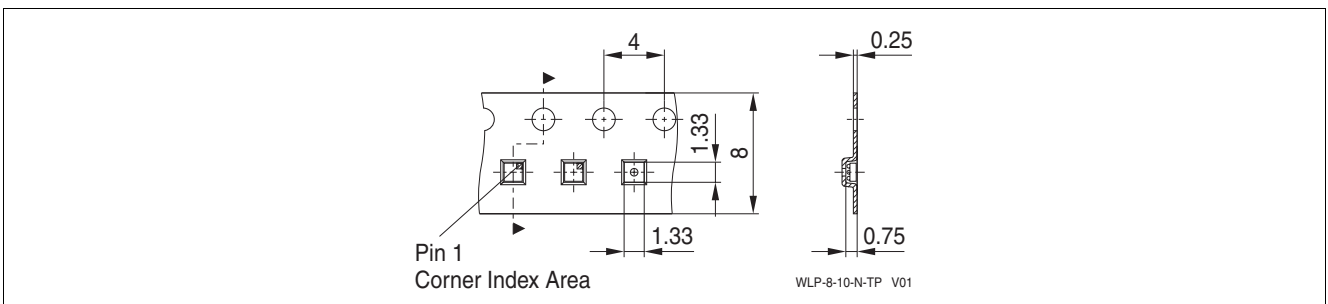


Figure 6 Tape for BGF125 / WLP-8-10

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