Ordering number : ENA1755A

SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

P-Channel Silicon MOSFET

ATP113 — General-Purpose Switching Device Applications

Features

- ON-resistance $R_{DS}(on)1$=22.5mΩ(typ.)
- 4V drive
- Protection diode in
- Input Capacitance Ciss=2400pF(typ.)
- Halogen free compliance

Specifications

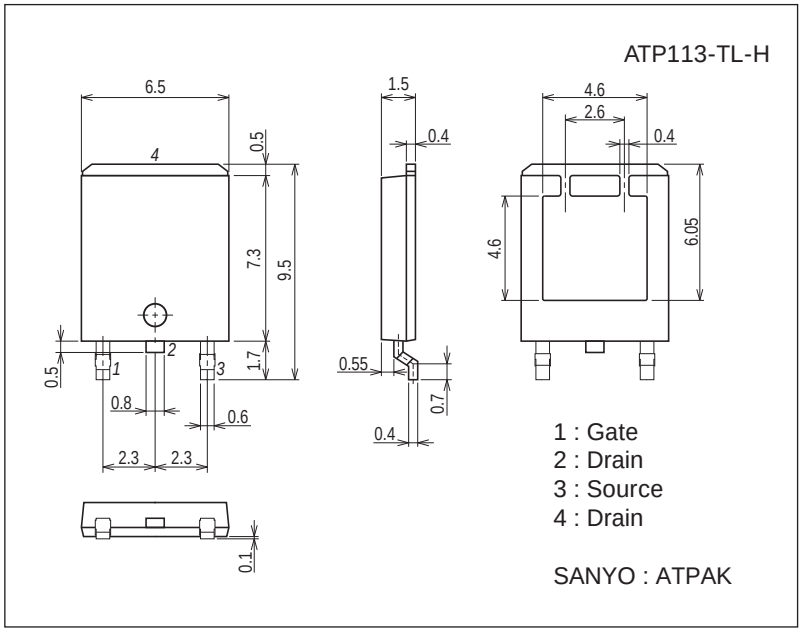
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		−60	V
Gate-to-Source Voltage	V_{GSS}		±20	V
Drain Current (DC)	I_D		−35	A
Drain Current (PW≤10μs)	I_{DP}	PW≤10μs, duty cycle≤1%	−105	A
Allowable Power Dissipation	P_D	Tc=25°C	50	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C
Avalanche Energy (Single Pulse) *1	E_{AS}		95	mJ
Avalanche Current *2	I_{AV}		−18	A

Note :*1 V_{DD}=−10V, L=500μH, I_{AV}=−18A
*2 L≤500μH, Single pulse

Package Dimensions

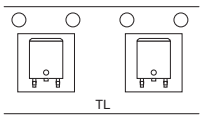
unit : mm (typ)
7057-001



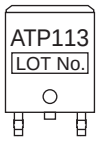
Product & Package Information

- Package : ATPAK
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

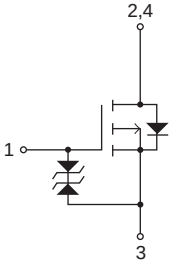
Packing Type: TL



Marking



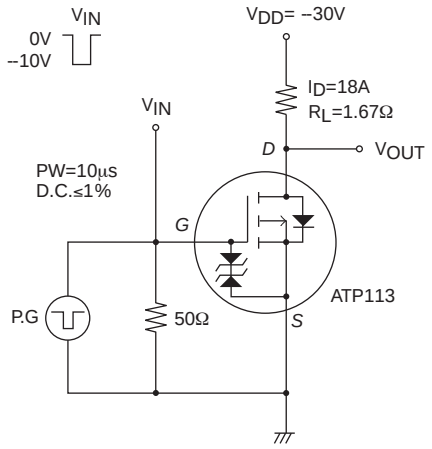
Electrical Connection



Electrical Characteristics at Ta=25°C

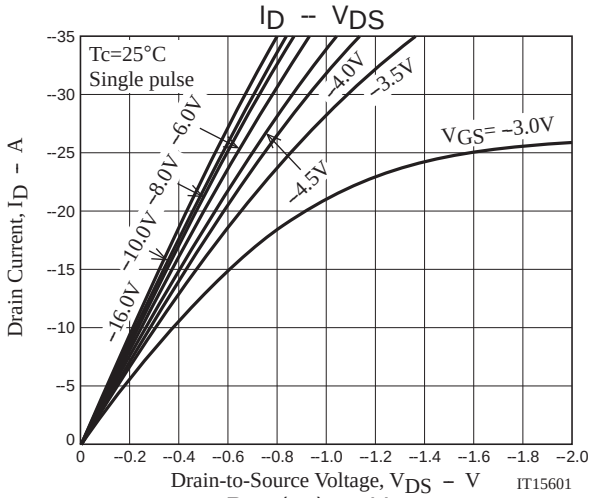
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=−1mA, V_{GS}=0V	−60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=−60V, V_{GS}=0V			−1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=−10V, I_D=−1mA	−1.2		−2.6	V
Forward Transfer Admittance	| yfs |	V_{DS}=−10V, I_D=−18A		37		S
Static Drain-to-Source On-State Resistance	R_{DS}(on)1	I_D=−18A, V_{GS}=−10V		22.5	29.5	mΩ
	R_{DS}(on)2	I_D=−9A, V_{GS}=−4.5V		27	38	mΩ
	R_{DS}(on)3	I_D=−5A, V_{GS}=−4V		29	44	mΩ
Input Capacitance	Ciss	V_{DS}=−20V, f=1MHz		2400		pF
Output Capacitance	Coss			250		pF
Reverse Transfer Capacitance	Crss			195		pF
Turn-ON Delay Time	t_d(on)	See specified Test Circuit.		15		ns
Rise Time	t_r			125		ns
Turn-OFF Delay Time	t_d(off)			250		ns
Fall Time	t_f			200		ns
Total Gate Charge	Qg	V_{DS}=−30V, V_{GS}=−10V, I_D=−35A		55		nC
Gate-to-Source Charge	Qgs			7.5		nC
Gate-to-Drain “Miller” Charge	Qgd			12		nC
Diode Forward Voltage	V_{SD}	I_S=−35A, V_{GS}=0V		−0.98	−1.5	V

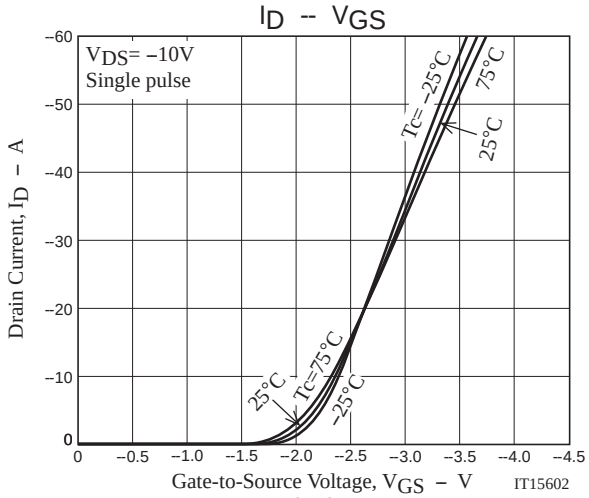
Switching Time Test Circuit

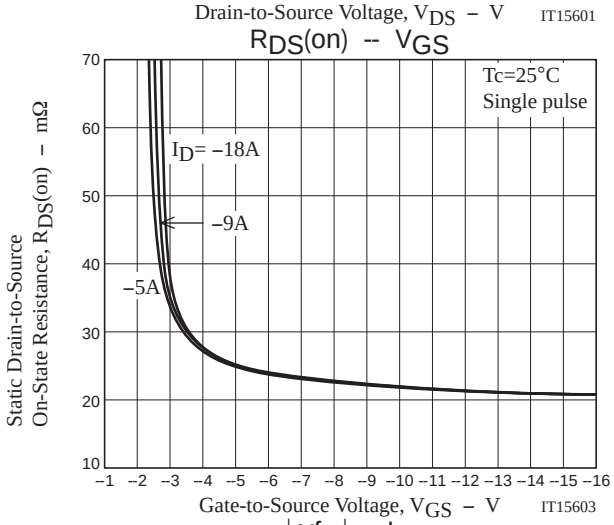


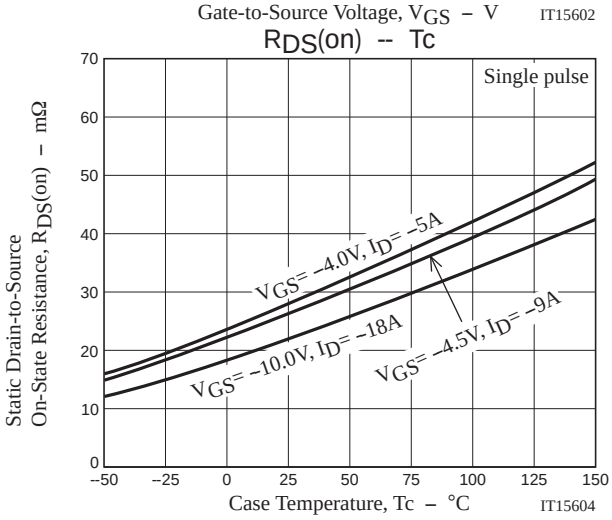
Ordering Information

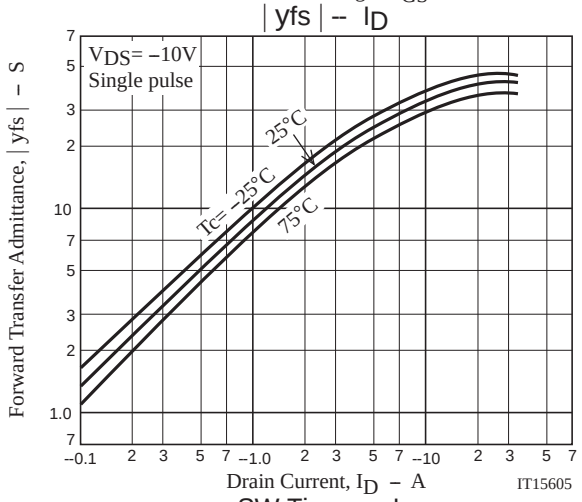
Device	Package	Shipping	memo
ATP113-TL-H	ATPAK	3,000pcs./reel	Pb Free and Halogen Free

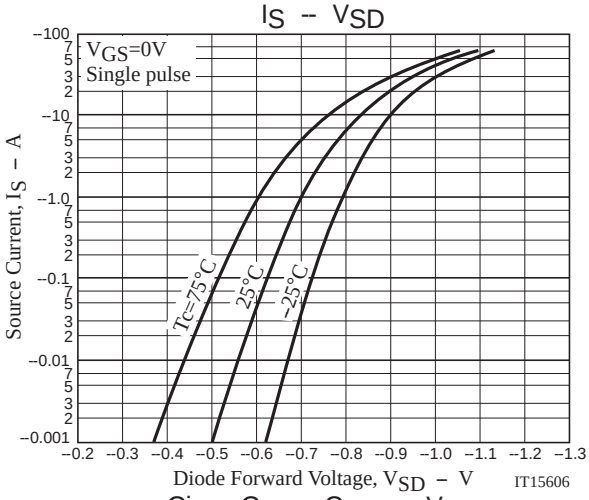

ID -- VDS
Tc=25°C
Single pulse
VGS= –3.0V
–3.5V
–4.0V
–4.5V
–6.0V
–8.0V
–10.0V
–16.0V
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT15601

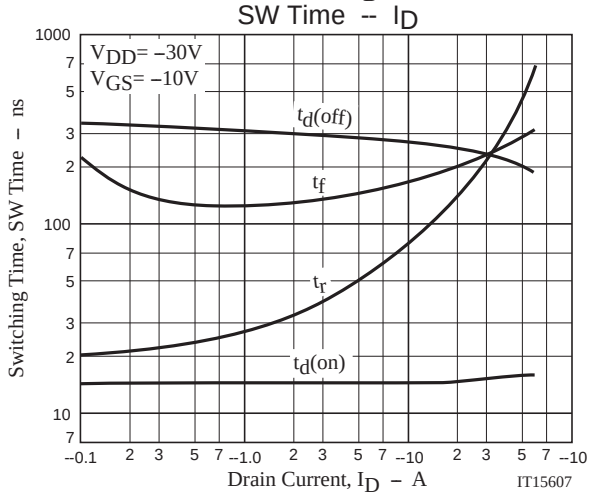

ID -- VGS
VDS= –10V
Single pulse
Tc= –25°C
75°C
25°C
Drain Current, ID – A
Gate-to-Source Voltage, VGS – V
IT15602

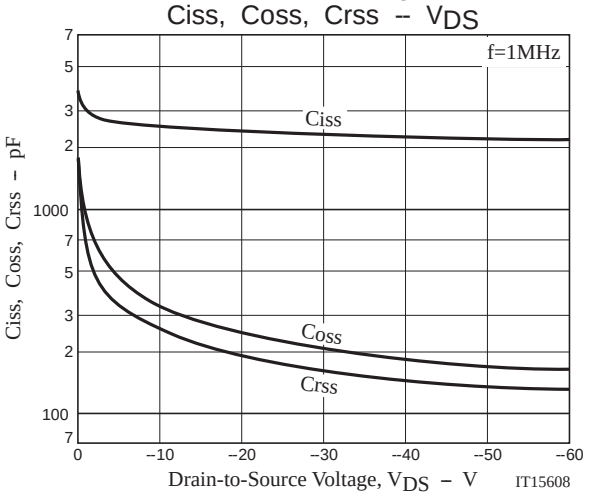

RDS(on) -- VGS
Tc=25°C
Single pulse
ID= –18A
–9A
–5A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage, VGS – V
IT15603

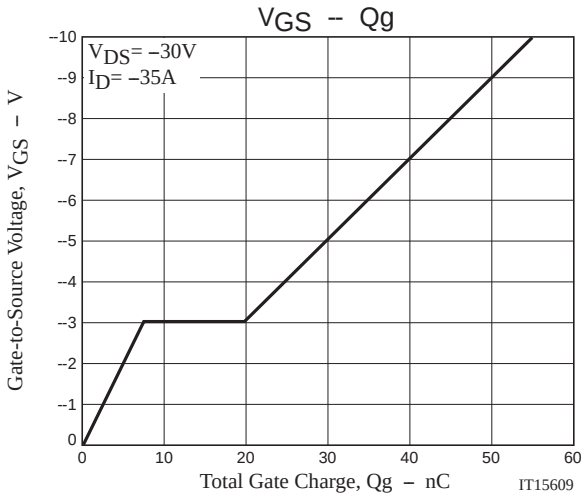

RDS(on) -- Tc
Single pulse
VGS= –4.0V, ID= –5A
VGS= –10.0V, ID= –18A
VGS= –4.5V, ID= –9A
Static Drain-to-Source On-State Resistance, RDS(on) – mΩ
Case Temperature, Tc – °C
IT15604

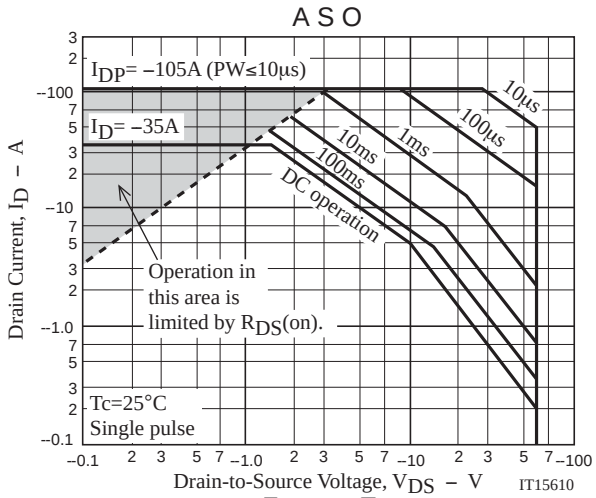

| yfs | -- ID
VDS= –10V
Single pulse
25°C
Tc= –25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current, ID – A
IT15605

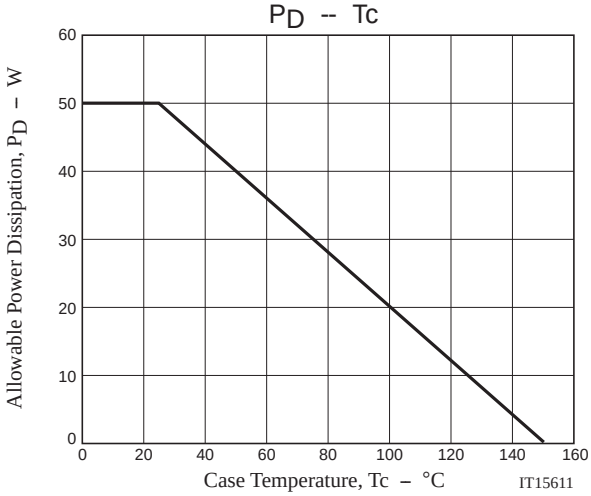

IS -- VSD
VGS=0V
Single pulse
Tc=75°C
25°C
–25°C
Source Current, IS – A
Diode Forward Voltage, VSD – V
IT15606

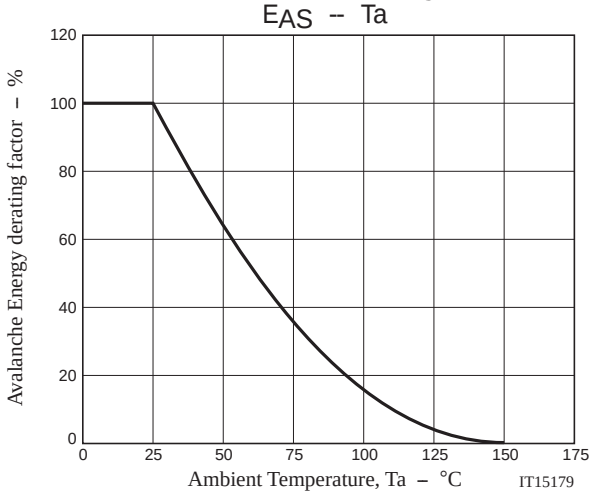

SW Time -- ID
VDD= –30V
VGS= –10V
td(off)
tf
tr
td(on)
Switching Time, SW Time – ns
Drain Current, ID – A
IT15607


Ciss, Coss, Crss -- VDS
f=1MHz
Ciss
Coss
Crss
Ciss, Coss, Crss – pF
Drain-to-Source Voltage, VDS – V
IT15608


VGS – Qg
VDS= –30V
ID= –35A
Gate-to-Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT15609


A S O
IDP= –105A (PW≤10μs)
ID= –35A
10μs
100μs
1ms
10ms
100ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current, ID – A
Drain-to-Source Voltage, VDS – V
IT15610


PD – Tc
Allowable Power Dissipation, PD – W
Case Temperature, Tc – °C
IT15611


EAS – Ta
Avalanche Energy derating factor – %
Ambient Temperature, Ta – °C
IT15179

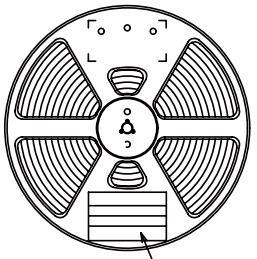
Taping Specification

ATP113-TL-H

1. Packing Format (TL)

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	INNER BOX SD-C-18	OUTER BOX SD-A-18
ATPAK	ATP	3,000	3,000	15,000	1 reels contained Dimensions:mm (external) 340×340×28	5 inner boxes contained Dimensions:mm (external) 355×355×165

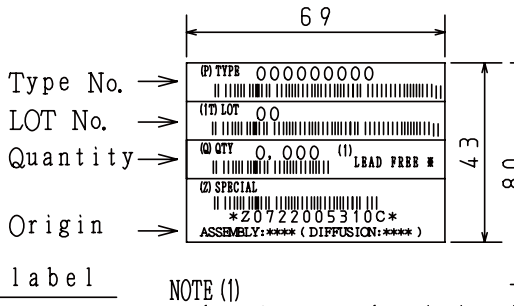
Packing method



Reel label

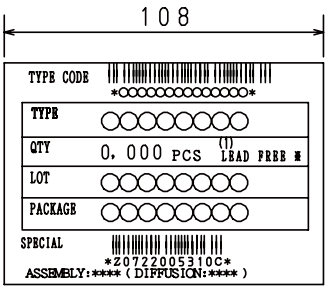
Reel label, Inner box label

(unit:mm)



Outer box label

It is a label at the time of factory shipments. The form of a label may change in physical distribution process.



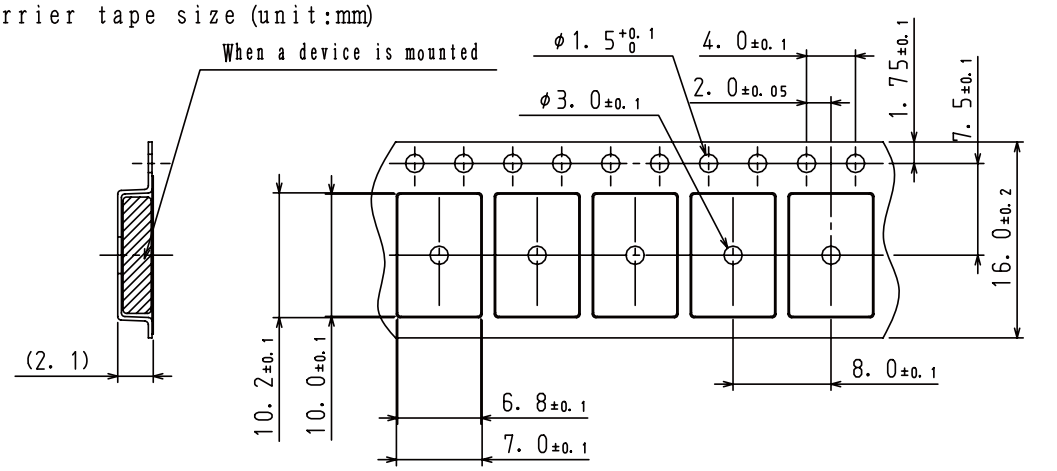
NOTE (1)

The LEAD FREE ※ description shows that the surface treatment of the terminal is lead free.

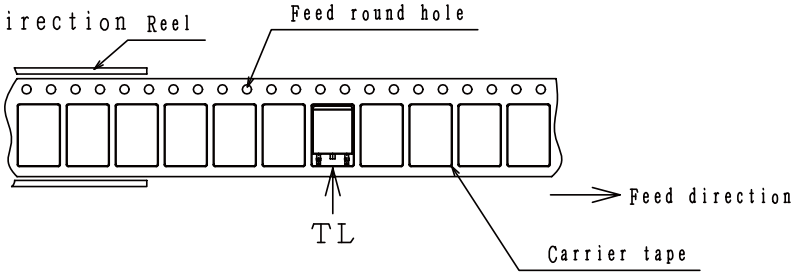
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



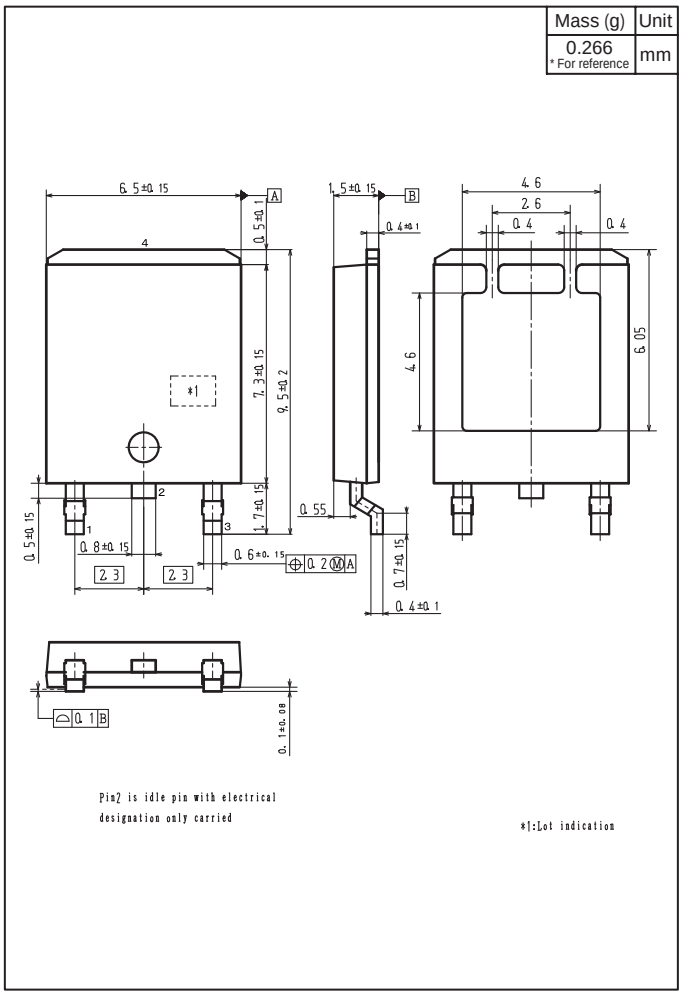
2-2. Device placement direction



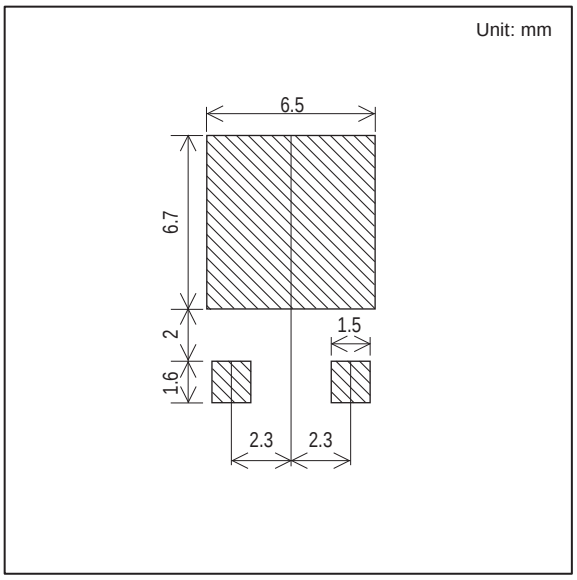
The one erectrode terminals on feed hole side····TL

Outline Drawing

ATP113-TL-H



Land Pattern Example



Note on usage : Since the ATP113 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

This catalog provides information as of June, 2012. Specifications and information herein are subject to change without notice.