

AOD400

N-Channel Enhancement Mode Field Effect Transistor

General Description

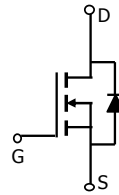
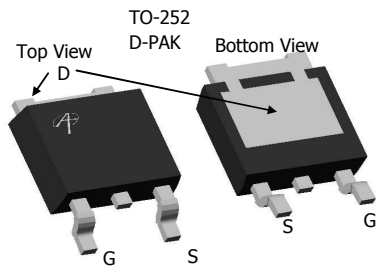
The AOD400 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

- RoHS Compliant
- Halogen Free*

Features

- V_{DS} (V) = 30V
- I_D = 10 A (V_{GS} = 10V)
- $R_{DS(ON)} < 30 \text{ m}\Omega$ (V_{GS} = 10V)
- $R_{DS(ON)} < 36 \text{ m}\Omega$ (V_{GS} = 4.5V)
- $R_{DS(ON)} < 52 \text{ m}\Omega$ (V_{GS} = 2.5V)

100% Rg Tested!



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|---|-------------------------|------------|------------------|
| Drain-Source Voltage | V_{DS} | 30 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | V |
| Continuous Drain Current ^G | $T_C=25^\circ\text{C}$ | 10 | A |
| | $T_C=100^\circ\text{C}$ | 10 | |
| Pulsed Drain Current ^C | I_{DM} | 40 | |
| Avalanche Current ^C | I_{AR} | 10 | A |
| Repetitive avalanche energy $L=0.1\text{mH}$ ^C | E_{AR} | 30 | mJ |
| Power Dissipation ^B | $T_C=25^\circ\text{C}$ | 20 | W |
| | $T_C=100^\circ\text{C}$ | 10 | |
| Power Dissipation ^A | $T_A=25^\circ\text{C}$ | 2.1 | W |
| | $T_A=70^\circ\text{C}$ | 1.3 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 175 | $^\circ\text{C}$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 17.4 | 30 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 50 | |
| Maximum Junction-to-Case ^B | $R_{\theta JC}$ | 4 | 7.5 | $^\circ\text{C/W}$ |

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|---|-----|----------|----------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =24V, V _{GS} =0V T _J =55°C | | 0.002 | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±12V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 0.7 | 1.1 | 1.5 | V |
| I _{D(ON)} | On state drain current | V _{GS} =4.5V, V _{DS} =5V | 40 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =10A T _J =125°C | | 25 35 | 30 42 | mΩ |
| | | V _{GS} =4.5V, I _D =10A | | 28.5 | 36 | mΩ |
| | | V _{GS} =2.5V, I _D =3.5A | | 40.5 | 52 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =10A | | 21 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.77 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 3 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | | 857 | 1030 | pF |
| C _{oss} | Output Capacitance | | | 97 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 71 | | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | | 1.2 | 3.6 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _g | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =10A | | 9.7 | 12 | nC |
| Q _{gs} | Gate Source Charge | | | 1.63 | | nC |
| Q _{gd} | Gate Drain Charge | | | 3.1 | | nC |
| t _{D(on)} | Turn-On Delay Time | V _{GS} =10V, V _{DS} =15V, R _L =1.5Ω, R _{GEN} =6Ω | | 3.5 | | ns |
| t _r | Turn-On Rise Time | | | 3.7 | | ns |
| t _{D(off)} | Turn-Off Delay Time | | | 25 | | ns |
| t _f | Turn-Off Fall Time | | | 4 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =10A, dI/dt=100A/μs | | 20 | 24 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =10A, dI/dt=100A/μs | | 13 | | nC |

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.

D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep 1ST 2008).

Rev 1 : Sep. 2008

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

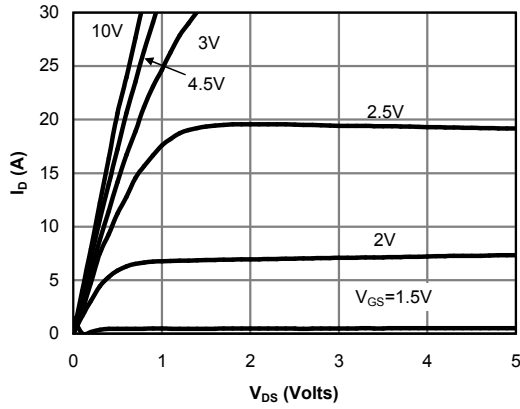


Fig 1: On-Region Characteristics

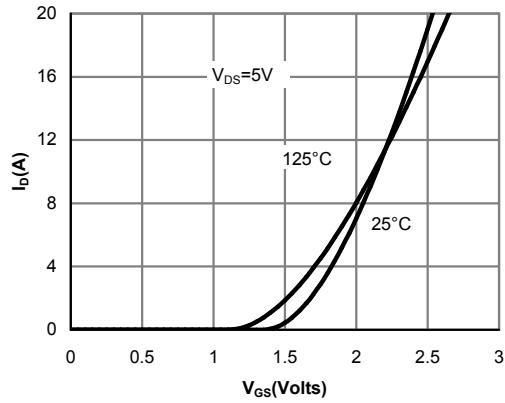


Figure 2: Transfer Characteristics

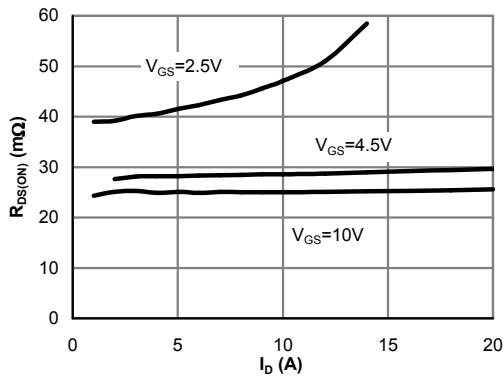


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

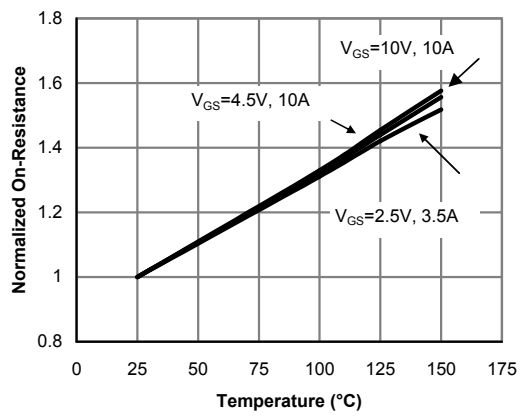


Figure 4: On-Resistance vs. Junction Temperature

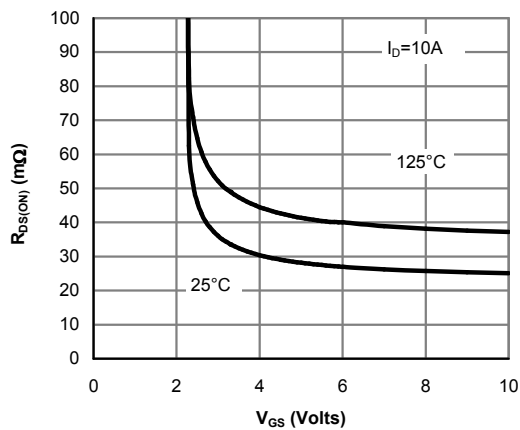


Figure 5: On-Resistance vs. Gate-Source Voltage

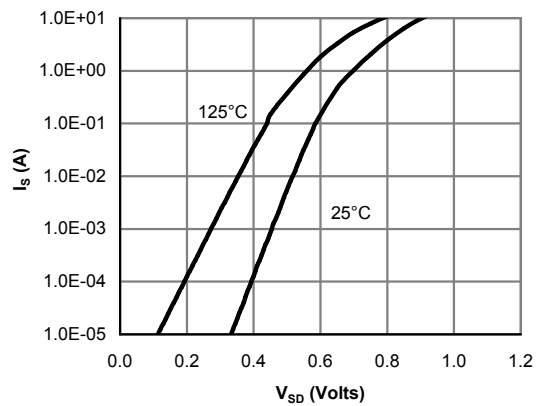


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

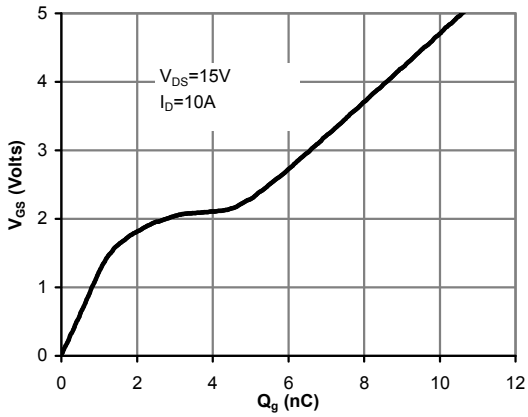


Figure 7: Gate-Charge Characteristics

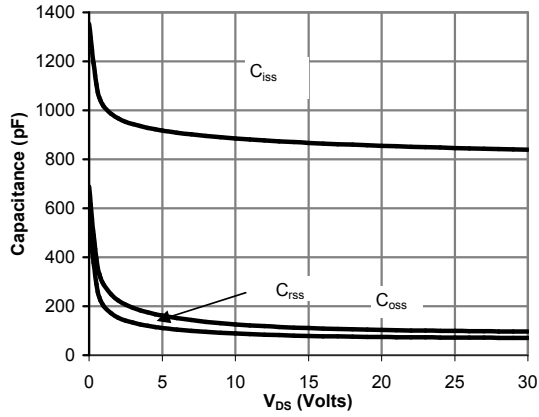


Figure 8: Capacitance Characteristics

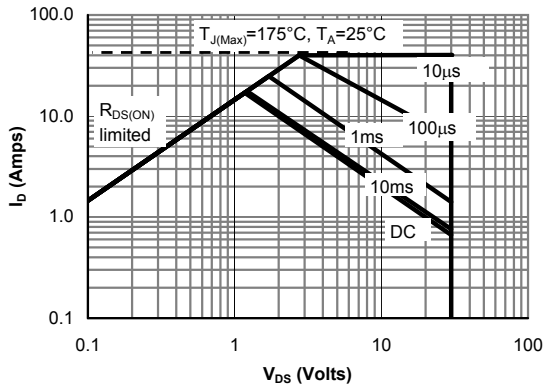


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

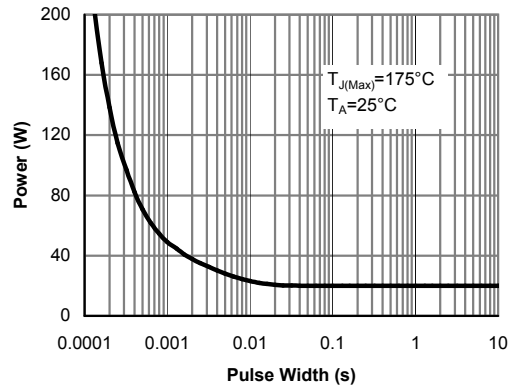


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

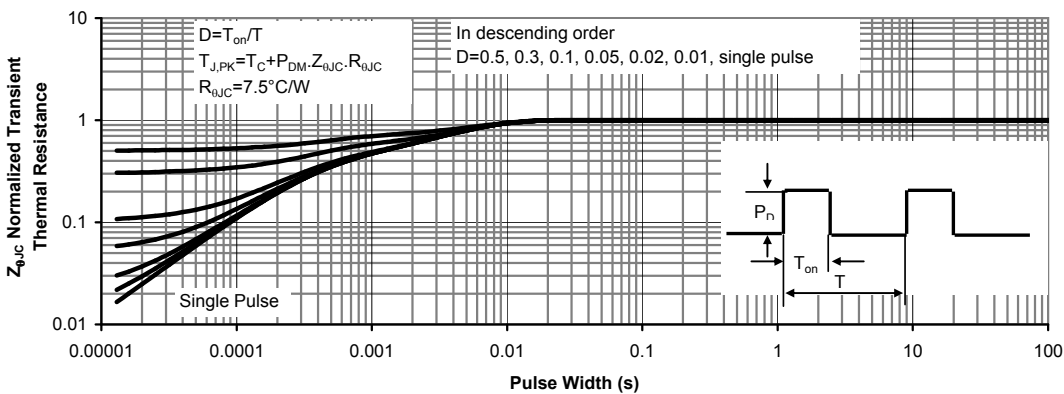


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

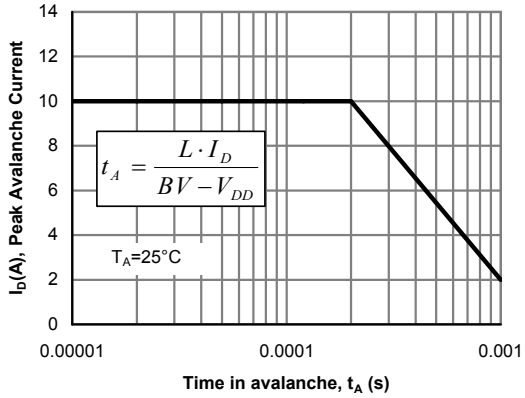


Figure 12: Single Pulse Avalanche capability

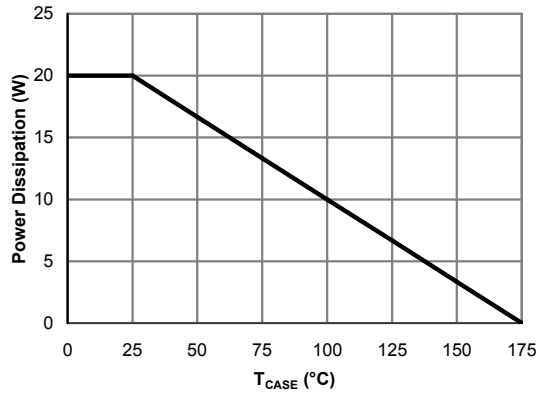


Figure 13: Power De-rating (Note B)

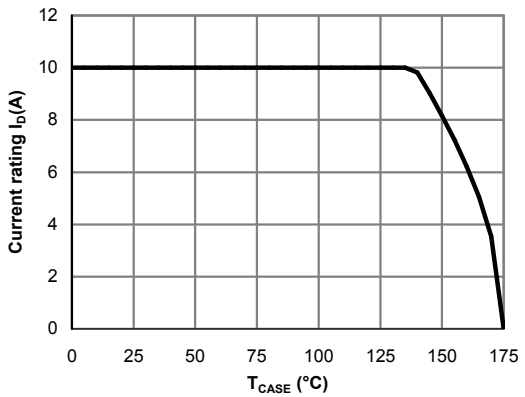


Figure 14: Current De-rating (Note B)

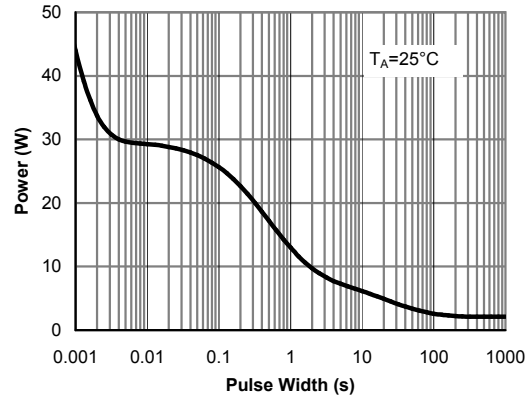


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

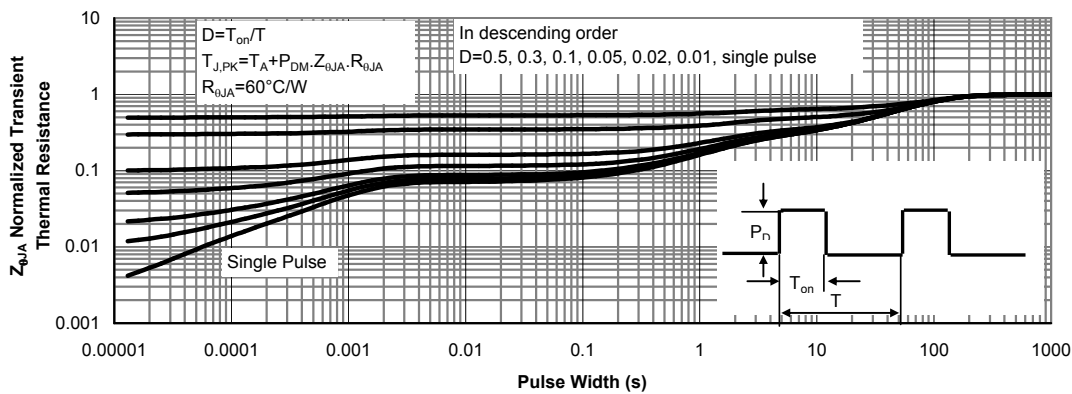
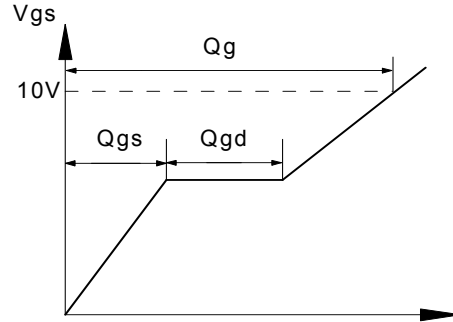
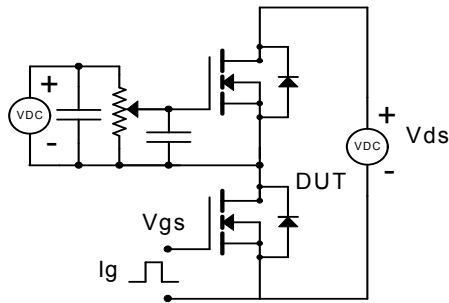
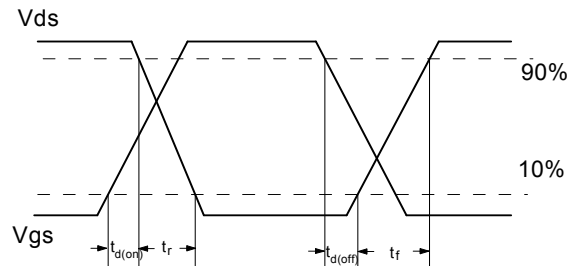
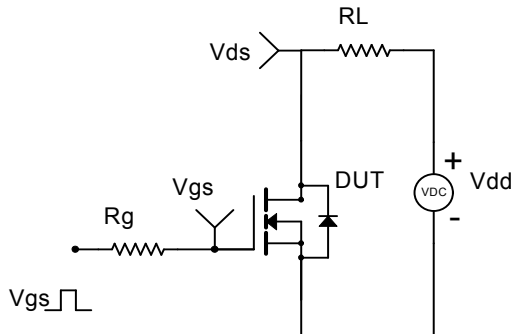


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

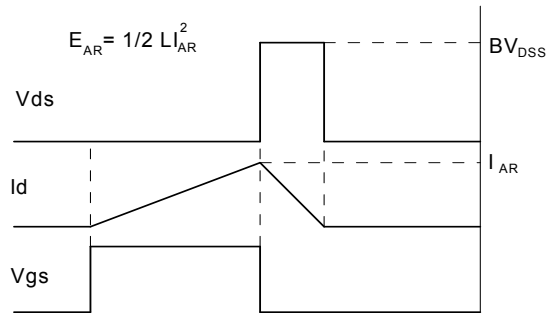
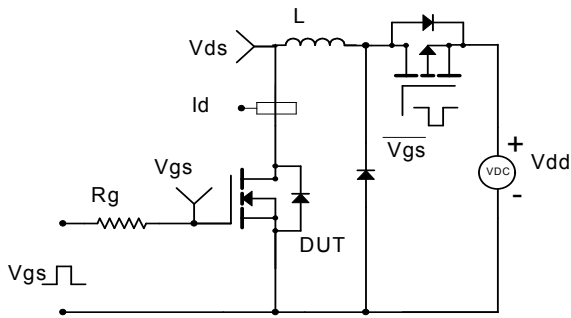
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

