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AMENDENT HISTORY

Version	Date	Description
Ver 1.0	Nov. 6, 2008	First issue
Ver 1.1	Nov. 17, 2008	Revise CVDD & VDDIO order of “Motor Application”
Ver 1.2	Jan. 6, 2009	Just revise version following with 4/8/12 IO body
Ver 1.3	Feb. 13, 2009	1. Revise Rosc=220K Ohm in Application Circuit part
Ver 1.4	May 6, 2009	1. Revise frequency guarantee range in electrical characteristics according IC Test flow
Ver 1.5	June 23, 2009	No modification, just revise version following with updating SNC26500 IO numbers.
Ver 1.6	July 23, 2009	Revise system clock with 2.05MHz (typical).
Ver 1.7	October 14, 2009	1. Revise PWM output spec condition with BUOx=1/2 VDD (peak value), instead of 1KHz sine wave

1. INTRODUCTION

SNC26250 is a one-channel voice synthesizer IC with PWM direct drive circuit. It built in a 4-bit tiny controller with one 4-bit input port and two 4-bit I/O ports. By programming through the tiny controller in SNC26250, user's varied applications including voice section combination, key trigger arrangement, output control, and other logic functions can be easily implemented.

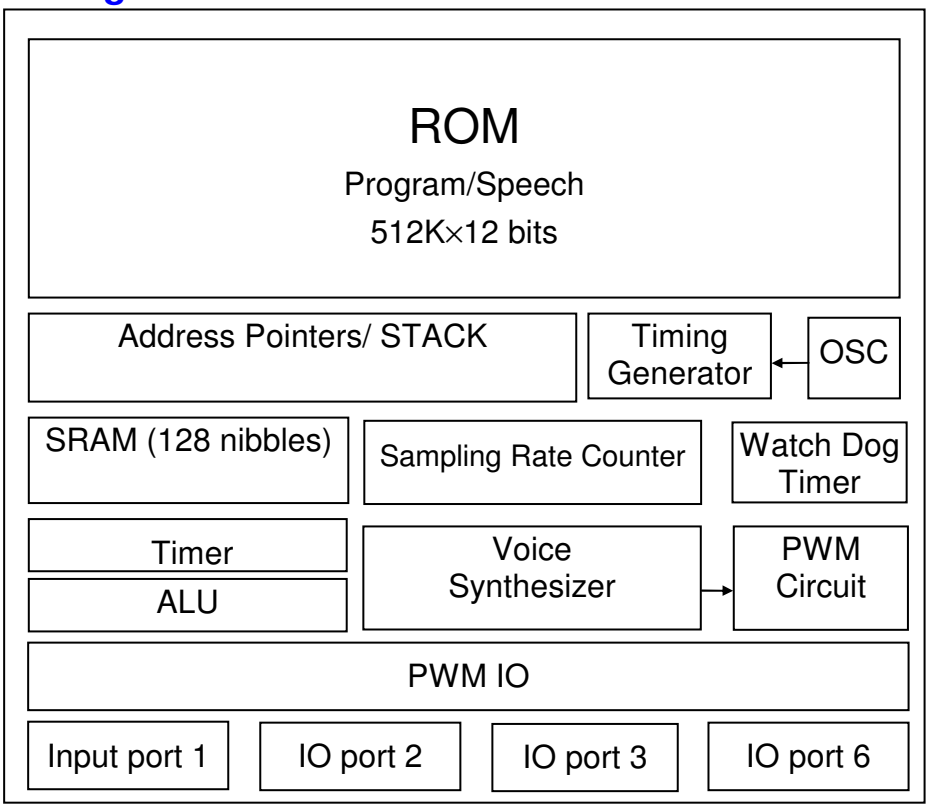
2. FEATURES

- Single power supply 2.4V – 5.5V
- 250 seconds voice capacity are provided (@6KHZ sample rate)
- Built in a 4-bit tiny controller
- I/O Port
  - One 4-bit Input port P1is provided.
  - Three 4-bit I/O ports P2, P3 and P6 are provided.
  - The driving/sink current of P2 & P3 is up to 8mA/16mA
  - The IO pins P2.3 can be modulated with 38.5Khz carry signal to implement IR function.
  - PWM output for IO (P2.0~P2.3, P3.0~P3.3)
- 128*4 bits RAM are provided
- Maximum 64k program ROM is provided
- 512K*12 shared ROM for voice data and program
- Readable ROM code data
- Voice Synthesizer:
  - Single channel speech output.
  - Support 4-bits SONiX-ASDPCM and 8-bit PCM algorithm
- Adaptive playing speed from 2.5k-20kHz is provided
- Built in an PWM circuit output, can directly connected to Speaker for sound output.
- System clock: 2MHz
- Event Mark function supported
- Low Power Detect.
- Watch Dog Timer Supported

3. PIN ASSIGNMENT

Symbol	I/O	Function Description
P10~P13	I	Input port 1
P20~P23	I/O	I/O port 2: IO
P30~P33	I/O	I/O port 3: IO
P60~P63	I/O	I/O port 6: IO
Rosc	I	Oscillation component connection pin
BUO1	O	PWM output 1
BUO2	O	PWM output 2
RST	I	RST=1→ Reset Chip (Active H)
CVDD	I	Positive power supply for CPU
CGND	I	Negative power supply for CPU
VDDIO	I	Positive power supply for I/O
GNDIO	I	Negative power supply for I/O
Test	I	Test pin

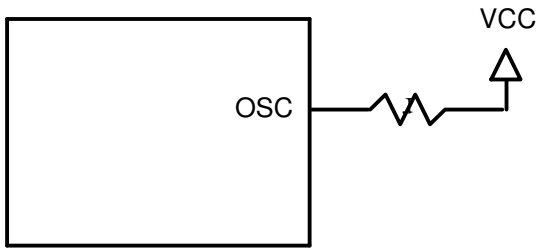
4. Block Diagram



5. FUNCTION DESCRIPTIONS

5.1 Oscillator

SNC26250 accepts RC type oscillator for system clock. The typical circuit diagram for oscillator is listed as follows.



RC Oscillator

5.2 ROM

SNC26250 contains a substantial 512K words (12-bit) internal ROM, which is shared by program and resource data. Program, voice and data are shared within this same 512K words ROM.

5.3 RAM

SNC26250 contains 128 nibble RAM (128 x 4-bits). The 128 nibble RAM is divided into two pages (page 0, 64 nibbles ; page1, 16 nibbles RAM). In our programming structure, users can use the instructions, PAGE n (n=0 or 1) to switch and indicate the RAM page. Besides, users can use direct mode, M0 ~ M63 in the data transfer type instructions, to access first 64 nibbles of page0 and the last 64 nibbles of page1.

5.4 Power Down Mode

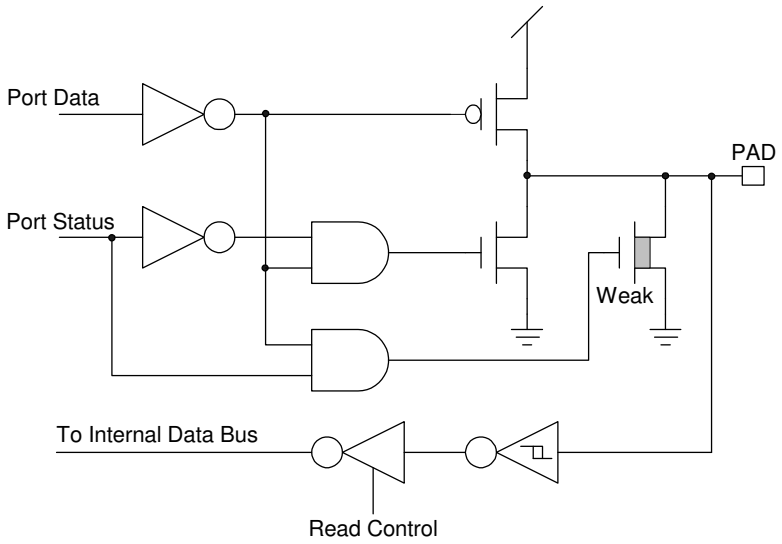
"End" instruction makes the IC entering into Stop Mode will stop the system clock for power savings (<3uA @VDD=3V and <6uA @VDD=4.5V.) Any valid data transition (L→H or H→L) occurring on any IO pin can be used to start the system clock and return to normal operating mode.

5.5 Sampling Rate Counter

The unique sampling rate counter is designed in voice channel to be able to play diverse voices at different sample playing rates. The playing rate can be adaptively set up among from the wide ranges of 2.5KHz to 20KHz. This architecture yields a high-quality voice synthesis that sounds very close to its original source when played through the same amplifier and speaker circuitry.

5.6 I/O Ports

There are one 4-bit input port P1 and two 4-bit I/O ports P2 and P3. Any I/O can be individually programmed as either input pull low or output. Any valid data transition (H→ L|L→H) of P1, P2 and P3 can reactivate the chip when it is in power-down stage.



I/O Port Configuration

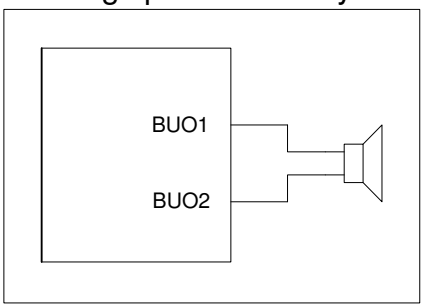
Note:

(1) ***Weak N-MOS can serve as pull-low resistor.***

(2) ***The driving/sink current of P2 & P3 is up to 8mA/16mA***

5.7 PWM Output

An PWM circuit is built-in SNC26250. The maximum resolution of PWM is 8 bits. Two huge output stage circuits are designed in SNC26250. With this advanced circuit, the chip is capable of driving speaker directly without external transistors.



PWM Output

5.8 Watch Dog Timer

SNC26250 built an internal WDT (Watch Dog Timer). This Watchdog timer would issue resets signal to this chip if it is not cleared before reaching terminal count (128 ms). The watchdog timer is enabled at reset and cannot be disabled.

5.9 IR Function

P23 can be modulated with 38.5KHz square wave before sent out to P23 pin. The IR signal can be achieved by this modulated signal.

5.10 PWM IO control

SNC26250 has support 8 PWM IO (P20~P23, P30~P33). Each I/O has 8 bit independent duty register, and the 8 bit register are compare with 8 bits counter. If set use PWM IO function and internal counter start at 000H, the mapping I/O will set High. The 8 bits counter increment if the same duty register, that will reset the mapping IO pin.

6. ABSOLUTE MAXIMUM RATING

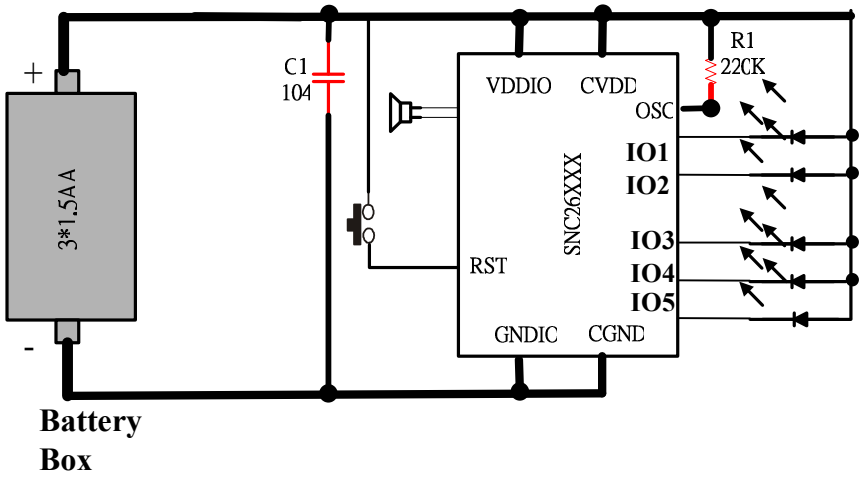
Items	Symbol	Min	Max	Unit.
Supply Voltage	V_{DD}-V	-0.3	6.0	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}	0	55.0	°C
Storage Temperature	T_{STG}	-55.0	125.0	°C

7. ELECTRICAL CHARACTERISTICS

Item	Sym.	Min.	Typ.	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	5.5	V	
Standby current	I_{SBY}	-	-	3.0 6.0	*u*A	V_{DD}=3V, no load V_{DD}=4.5V, no load
Operating Current	I_{OPR}	-	300	-	*u*A	V_{DD}=3V, no load
Input current of P1, P2, P3 & P6	I_{IH}	-	3.0	-	*u*A	V_{DD}=3V,V_{IN}=3V
Drive current of P6	I_{OD}	3	4	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink current of P6	I_{OS}	4	6	-	*m*A	V_{DD}=3V,V_O=2.4V
Drive current of P2, P3	I_{OD}	6	8	-	*m*A	V_{DD}=3V,V_O=2.4V
Sink current of P2, P3	I_{OS}	10	16	-	*m*A	V_{DD}=3V,V_O=2.4V
PWM current	I_{PWM}	-	240	-	*m*A	VDD=3V, BUOx=1.5V
PWM current	I_{PWM}	-	310	-	*m*A	VDD=4.5V, BUOx=2.25V
Oscillation Freq.	F_{OSC}	1.98	2.05	2.12	MHz	V_{DD}=3V, Temp.=25°C @Rosc = 220 Kohm Min : -3% Max : +3%

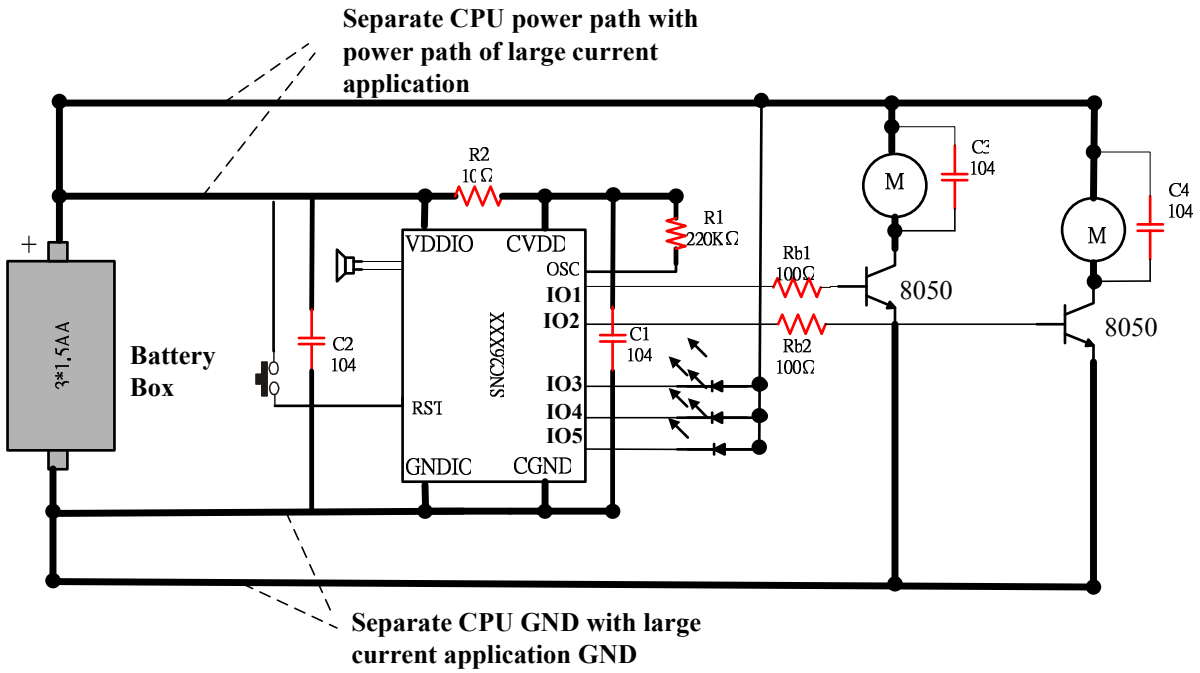
8. APPLICATION Circuit

8.1 General application



It is suggested to add a capacitor (C1), 104, between VDD with GND to keep power stable with general application. And this capacitor is strongly suggested to be as close to the chip as possible.

8.2 Motor application



There are some suggestions about PCB layout when user use SNC26000 series IC with motor applications.

(1) The capacitor C1 (104) C2 (104)is strongly suggested to be as close to the chip as possible.
(2) It had better let OSC components (R) get close to IC chip.

(3) OSC components had better get far away large current applications.

(4) Separate IC power path with large current application power path to avoid affect IC working by power drop from large current application.

(5) R2 (10Ω)separate VDDIO and CVDD.

(6) Let power cable thicker, especially for large current application.

(7) C3 and C4 (104) are connected at the positive point and negative point of the motor.

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