MC14024B

7-Stage Ripple Counter

The MC14024B is a 7–stage ripple counter with short propagation delays and high maximum clock rates. The Reset input has standard noise immunity, however the Clock input has increased noise immunity due to Hysteresis. The output of each counter stage is buffered.

- Diode Protection on All Inputs
- Output Transitions Occur on the Falling Edge of the Clock Pulse
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Pin–for–Pin Replacement for CD4024B

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	− 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	− 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

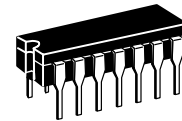* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
   Plastic "P and D/DW" Packages: − 7.0 mW/°C From 65°C To 125°C
   Ceramic "L" Packages: − 12 mW/°C From 100°C To 125°C
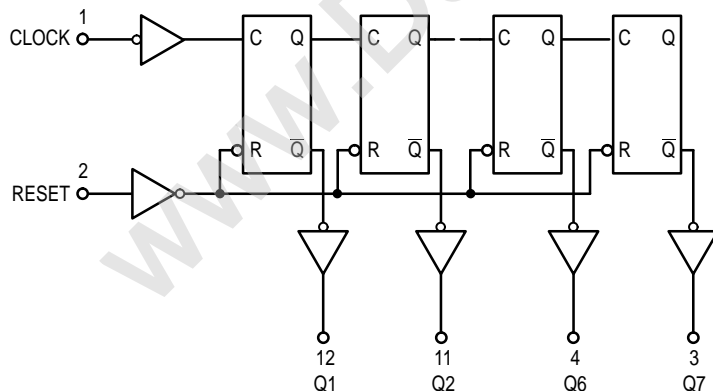
L SUFFIX
CERAMIC
CASE 632
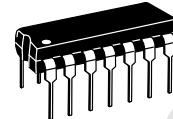
P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

T_A = − 55° to 125°C for all packages.

PIN ASSIGNMENT

CLOCK	1 ●		14	V_{DD}
RESET	2		13	NC
Q7	3		12	Q1
Q6	4		11	Q2
Q5	5		10	NC
Q4	6		9	Q3
V_{SS}	7		8	NC
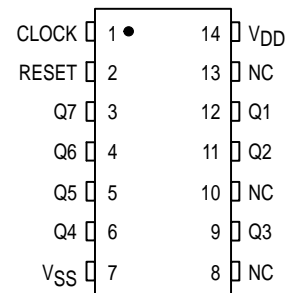
V_{DD} = PIN 14
V_{SS} = PIN 7
NC = NO CONNECTION

LOGIC DIAGRAM

Q3 = PIN 9
Q4 = PIN 6
Q5 = PIN 5

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
V_{in} = 0 or V_{DD} "1" Level	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
(V_O = 0.5 or 4.5 Vdc) "1" Level (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	− 3.0 − 0.64 − 1.6 − 4.2	— — — —	− 2.4 − 0.51 − 1.3 − 3.4	− 4.2 − 0.88 − 2.25 − 8.8	— — — —	− 1.7 − 0.36 − 0.9 − 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15		I_T = (0.31 μA/kHz) f + I_{DD} I_T = (0.60 μA/kHz) f + I_{DD} I_T = (1.89 μA/kHz) f + I_{DD}					μAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit

Output Rise and Fall Time
  t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns
  t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns
  t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns
	t_{TLH},
	t_{THL}
		5.0
		10
		15
			—
			—
			—
				100
				50
				40
					200
					100
					80
						ns

Propagation Delay Time
 Clock to Q1
  t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 295 ns
  t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 117 ns
  t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 85 ns
 Clock to Q7
  t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 915 ns
  t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 367 ns
  t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 275 ns
 Reset to Q_n
  t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns
  t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 217 ns
  t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 155 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
		
		5.0
		10
		15
		
		5.0
		10
		15
			—
			—
			—
			
			—
			—
			—
			
			—
			—
			—
				380
				150
				110
				
				1000
				400
				300
				
				500
				250
				180
					600
					230
					175
					
					2000
					750
					565
					
					800
					400
					300
						ns

Clock Pulse Width	t_{WH}	5.0 10 15	500 165 125	200 60 40	— — —	ns
Reset Pulse Width	t_{WH}	5.0 10 15	600 350 260	375 200 150	— — —	ns
Reset Removal Time	t_{rem}	5.0 10 15	625 190 145	250 75 50	— — —	ns
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	— — —	— — —	1.0 8.0 200	s ms µs
Input Pulse Frequency	f_{cl}	5.0 10 15	— — —	2.5 8.0 12	1.0 3.0 4.0	MHz

* The formulas given are for the typical characteristics only at 25°C.
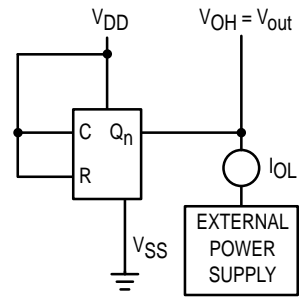#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
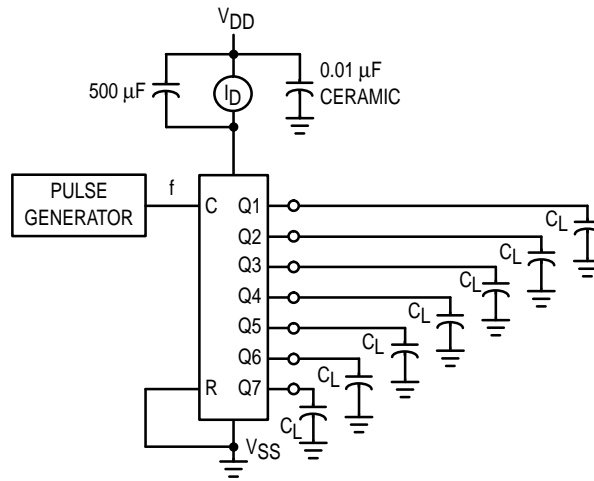
TRUTH TABLE

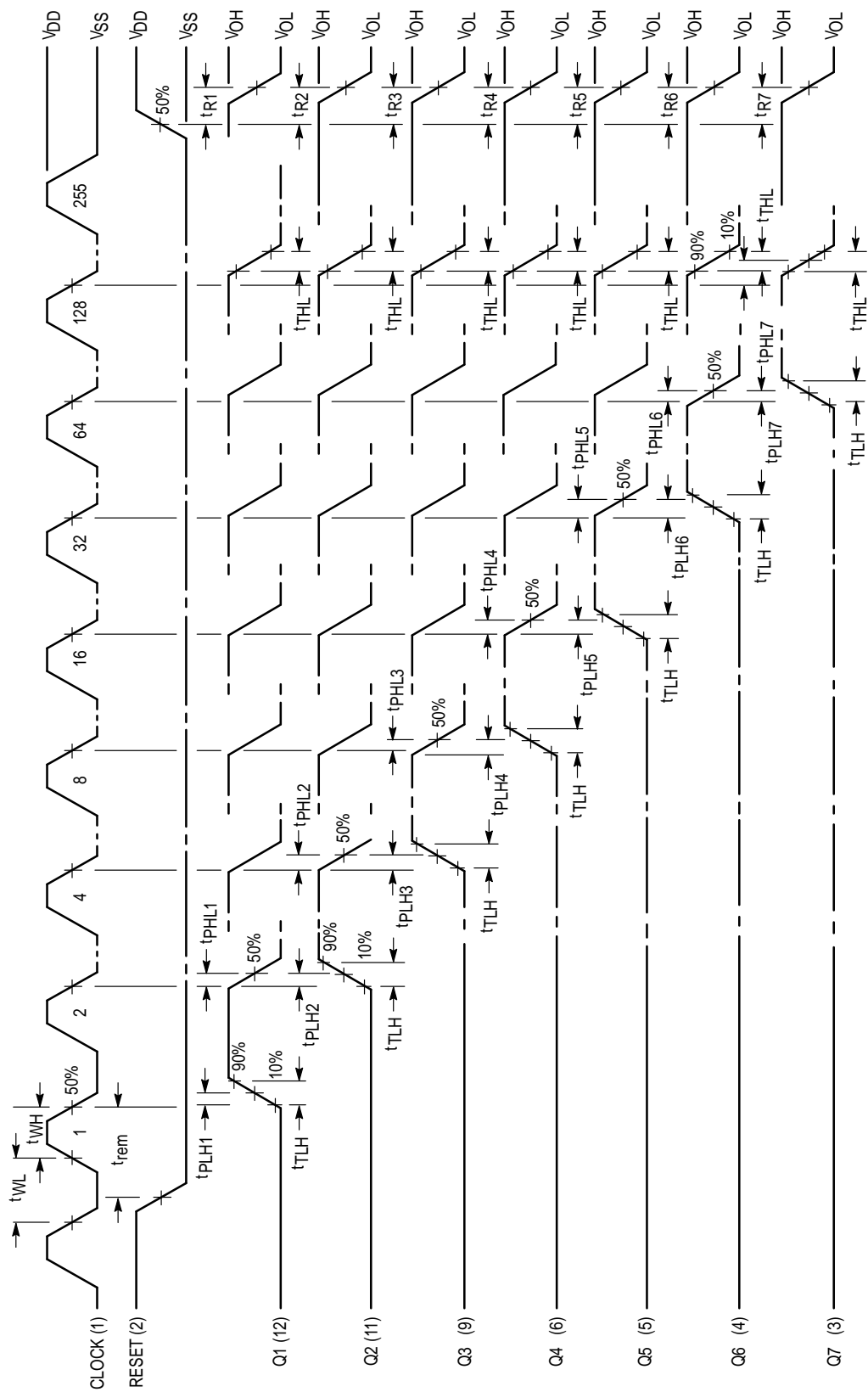| Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
⌐	0	No Change
⌐	1	All Outputs Low
⌐_	0	Advance One Count
⌐_	1	All Outputs Low
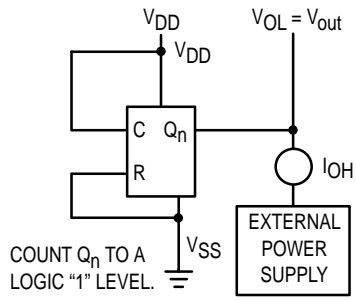
**Figure 1. Typical Output Source
Characteristics Test Circuit**

**Figure 2. Typical Output Sink
Characteristics Test Circuit**

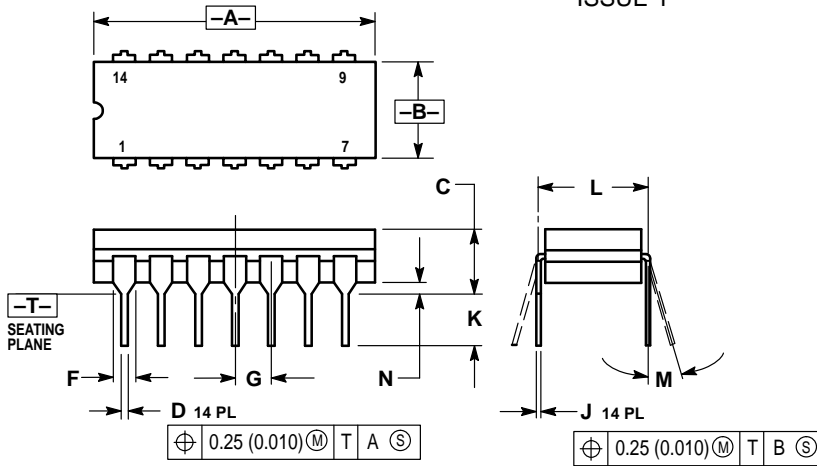**Figure 3. Power Dissipation Test Circuit**

Figure 4. Functional Waveforms

OUTLINE DIMENSIONS

L SUFFIX
CERAMIC DIP PACKAGE
CASE 632–08
ISSUE Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 646–06
ISSUE L
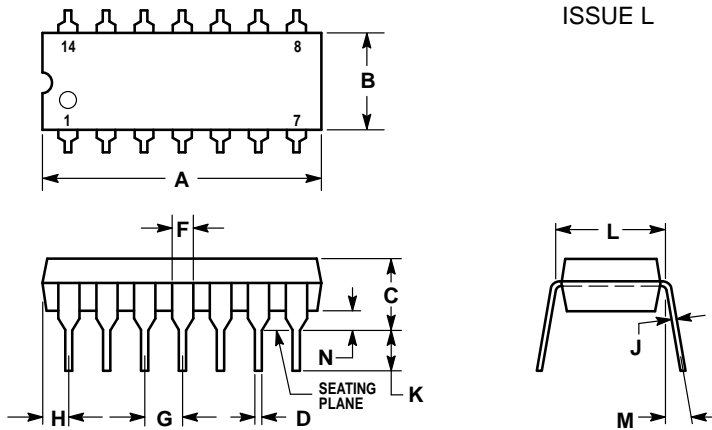
NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751A–03
ISSUE F
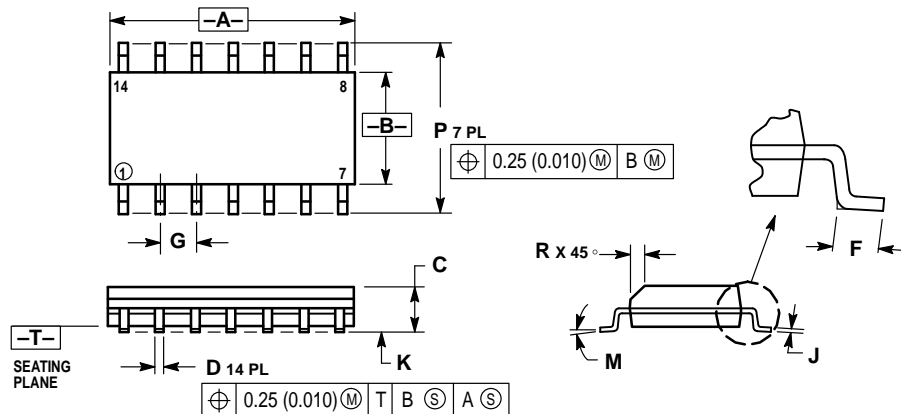
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

⊕ 0.25 (0.010) Ⓜ B Ⓜ

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

MOTOROLA

◊

MC14024B/D