# AK4421A

## 192kHz 24-Bit Stereo ΔΣ DAC with 2Vrms Output

## GENERAL DESCRIPTION

The AK4421A is 3.3V 24-bit stereo DAC with an integrated 2Vrms output buffer. A charge pump in the buffer develops an internal negative power supply rail that enables a ground-referenced 2Vrms output. Using AKM's multi bit modulator architecture, the AK4421A delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4421A integrates a combination of switched-capacitor and continuous-time filters, increasing performance for systems with excessive clock jitter. The 24-bit word length and 192kHz sampling rate make this part ideal for a wide range of consumer audio applications, such as portable A/V players, set-top boxes, and digital televisions. The AK4421A is offered in a space saving 16pin TSSOP package.

## FEATURES

☐ **Sampling Rate Ranging from 8kHz to 192kHz**
☐ **128 times Oversampling (Normal Speed Mode)**
☐ **64 times Oversampling (Double Speed Mode)**
☐ **32 times Oversampling (Quad Speed Mode)**
☐ **24-Bit 8 times FIR Digital Filter**
☐ **Switched-Capacitor Filter with High Tolerance to Clock Jitter**
☐ **Single Ended 2Vrms Output Buffer**
☐ **Soft mute**
☐ **I/F format: 24-Bit MSB justified or I$^2$S**
☐ **Master clock: 512fs, 768fs or 1152fs (Normal Speed Mode)**
             **256fs or 384fs (Double Speed Mode)**
             **128fs or 192fs (Quad Speed Mode)**
☐ **THD+N: -92dB**
☐ **Dynamic Range: 102dB**
☐ **Automatic Power-on Reset Circuit**
☐ **Power supply: +3.0 ~ +3.6V**
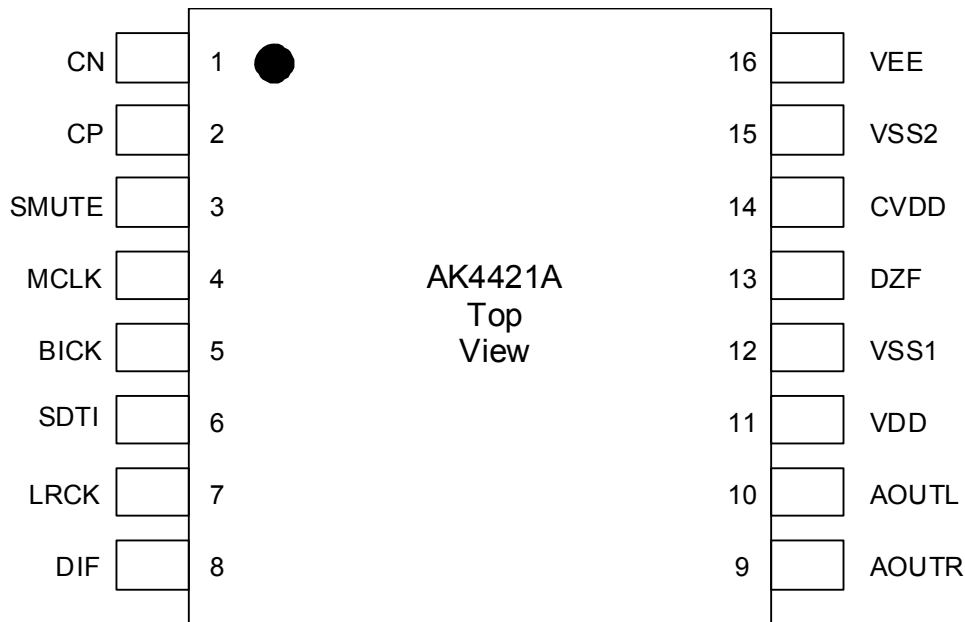☐ **Ta = -20 to 85°C**
☐ **Small Package: 16pin TSSOP (6.4mm x 5.0mm)**
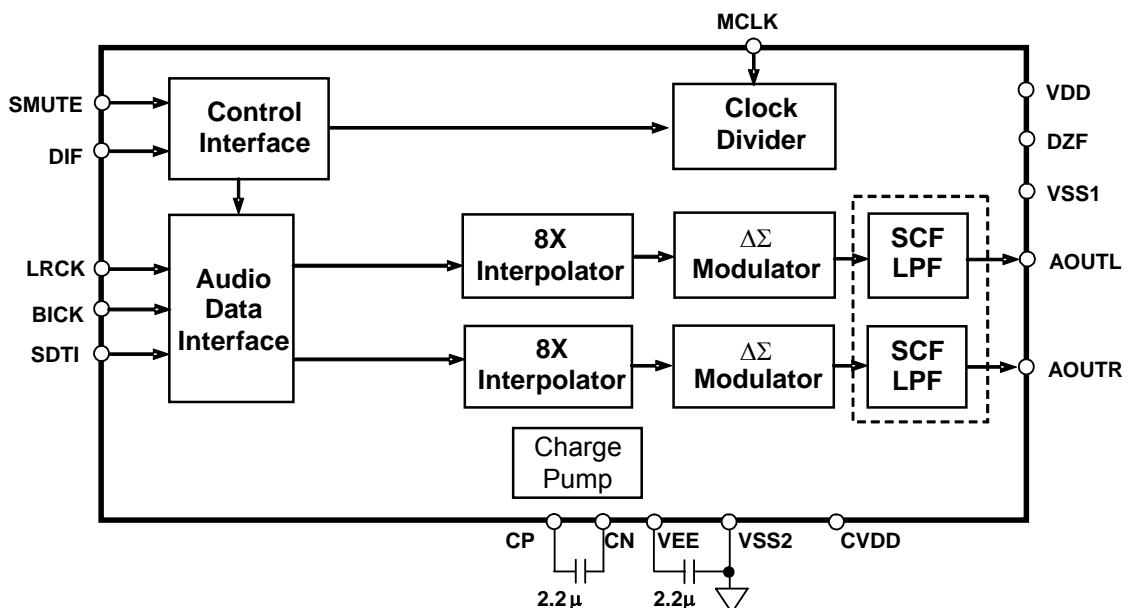
■ **Ordering Guide**

AK4421AET        -20 ~ +85°C              16pin TSSOP (0.65mm pitch)
AKD4421A          Evaluation Board for AK4421A

■ **Pin Layout**

```
CN    | 1  ●                        16 |  VEE
CP    | 2                           15 |  VSS2
SMUTE | 3                           14 |  CVDD
MCLK  | 4                           13 |  DZF
BICK  | 5        AK4421A            12 |  VSS1
SDTI  | 6         Top               11 |  VDD
LRCK  | 7         View              10 |  AOUTL
DIF   | 8                            9 |  AOUTR
```

■ **Compatibility with AK4420, AK4421, AK4424, AK4423 and AK4421A**

| | | AK4420 | AK4424 | AK4421 | AK4421A | AK4423 |
|---|---|---|---|---|---|---|
| Power Supply | | +4.5 ~ +5.5V | +4.5 ~ +5.5V | +3.0 ~ +3.6V | +3.0 ~ +3.6V | +3.0 ~ +3.6V |
| Digital de-emphasis | | - | X | - | - | X |
| I/F format | | 24-bit MSB/I²S | I²S | 24-bit MSB/I²S | 24-bit MSB/I²S | I²S |
| Pin out | Pin#3 | SMUTE | DEM | SMUTE | SMUTE | SMUTE |
| | Pin#8 | DIF | SMUTE | DIF | DIF | DEM |
| THD+N | | -92dB | -92dB | -92dB (-3dBFS) | -92dB | -92dB |
| DR | | 105dB | 105dB | 102dB | 102dB | 102dB |
| Operating Temperature | | ET: -20 ~ +85°C VT: -40 ~ +85°C | ET: -20 ~ +85°C | ET: -20 ~ +85°C | ET: -20 ~ +85°C | ET: -20 ~ +85°C |

-: Not available
X: Available

## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | CN | I | Negative Charge Pump Capacitor Terminal Pin<br>    Connect to CP with a 2.2µF low ESR (Equivalent Series Resistance) capacitor over temperature.  When this capacitor is polarized, the positive polarity pin should be connected to the CP pin.  Non-polarized capacitors can also be used. |
| 2 | CP | I | Positive Charge Pump Capacitor Terminal Pin<br>    Connect to CN with a 2.2µF low ESR (Equivalent Series Resistance) capacitor over temperature.  When this capacitor is polarized, the positive polarity pin should be connected to the CP pin.  Non-polarized capacitors can also be used. |
| 3 | SMUTE | I | Soft Mute Enable Pin  (Internal pull down: 100kΩ)<br>    "H": Enable, "L": Disable |
| 4 | MCLK | I | Master Clock Input Pin |
| 5 | BICK | I | Audio Serial Data Clock Pin |
| 6 | SDTI | I | Audio Serial Data Input Pin |
| 7 | LRCK | I | L/R Clock Pin |
| 8 | DIF | I | Audio Data Interface Format Pin (Internal pull up: 100kΩ)<br>    "L": 24-bit MSB Justified, "H": I2S |
| 9 | AOUTR | O | Right channel Analog Output Pin<br>    When power down, outputs VSS voltage (0V, typ). |
| 10 | AOUTL | O | Left channel Analog Output Pin<br>    When power down, outputs VSS voltage (0V, typ). |
| 11 | VDD | - | DAC Power Supply Pin, 3.0V~3.6V |
| 12 | VSS1 | - | Ground Pin 1 |
| 13 | DZF | O | Zero Input Detect Pin |
| 14 | CVDD | - | Charge Pump Power Supply Pin, 3.0V~3.6V |
| 15 | VSS2 | - | Ground Pin 2 |
| 16 | VEE | O | Negative Voltage Output Pin<br>    Connect to VSS2 with a 2.2µF low ESR capacitor over temperature. When this capacitor is polarized, the positive polarity pin should be connected to the VSS2 pin.  Non-polarized capacitors can also be used. |

Note: All input pins except for the SMUTE and DIF pins should not be left floating.

## ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2=0V; Note 1)

| Parameter | Symbol | min | max | Units |
|---|---|---|---|---|
| Power Supply | VDD | -0.3 | +6.0 | V |
| | CVDD | -0.3 | +6.0 | V |
| Input Current (Note 3) | IIN | - | ±10 | mA |
| Input Voltage | VIND | -0.3 | VDD+0.3 | V |
| Ambient Operating Temperature | Ta | -20 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 1. All voltages with respect to ground.
Note 2. VSS1, VSS2 connect to the same analog ground.
Note 3. SMUTE, MCLK, BICK, SDTI, LRCK and DIF pins.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
　　　　　Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=0V; Note 1)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supply | VDD | +3.0 | +3.3 | +3.6 | V |
| | CVDD | | VDD | | |

Note 4. CVDD should be equal to VDD.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

| ANALOG CHARACTERISTICS |
|---|

(Ta = 25°C; VDD=CVDD = +3.3V; fs = 44.1 kHz; BICK = 64fs; Signal Frequency = 1 kHz;
24bit Input Data; Measurement frequency = 20Hz ~ 20kHz; $R_L \geq 10k\Omega$, unless otherwise specified)

| Parameter | | min | typ | max | Units |
|---|---|---|---|---|---|
| Resolution | | | | 24 | Bits |
| THD+N | fs=44.1kHz, BW=20kHz | | -92 | -84 | dB |
| | fs=96kHz, BW=40kHz | | -92 | - | dB |
| | fs=192kHz, BW=40kHz | | -92 | - | dB |
| Dynamic Range (-60dBFS with A-weighted, Note 6) | | 96 | 102 | | dB |
| S/N (A-weighted, Note 7) | | 96 | 102 | | dB |
| Interchannel Isolation (1kHz) | | 90 | 100 | | dB |
| Interchannel Gain Mismatch | | | 0.2 | 0.5 | dB |
| **DC Accuracy** | | | | | |
| DC Offset  (at output pin) | | -40 | 0 | 40 | mV |
| Gain Drift | | | 100 | - | ppm/°C |
| Output Voltage (Note 8) | | 1.85 | 2.0 | 2.15 | Vrms |
| Load Capacitance (Note 9) | | | | 25 | pF |
| Load Resistance | | 10 | | | kΩ |
| **Power Supplies** | | | | | |
| Power Supply Current: (Note 10) | | | | | |
| Normal Operation (fs≤96kHz) | | | 14 | 21 | mA |
| Normal Operation (fs=192kHz) | | | 16 | 24 | mA |
| Power-Down Mode (Note 11) | | | 10 | 100 | μA |

Note 5. Measured by Audio Precision (System Two). Refer to the evaluation board manual.
Note 6. 98dB for 16-bit input data
Note 7. S/N does not depend on input data size.
Note 8. Full-scale voltage (0dB). Output voltage is proportional to the voltage of VDD:
     AOUT (typ.@0dB) = 2Vrms × VDD/3.3.
Note 9. In case of driving capacitive load, inset a resistor between the output pin and the capacitive load.
Note 10. The current into VDD and CVDD.
Note 11. All digital inputs including clock pins (MCLK, BICK and LRCK) are fixed to VSS or VDD. (The SMUTE and DIF pins are not included)

## FILTER CHARACTERISTICS

(Ta = 25°C; VDD=CVDD = +3.0 ~ +3.6V; fs = 44.1 kHz)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Digital filter** | | | | | |
| Passband ±0.05dB (Note 12) | PB | 0 | | 20.0 | kHz |
| −6.0dB | | - | 22.05 | - | kHz |
| Stopband (Note 12) | SB | 24.1 | - | - | kHz |
| Passband Ripple | PR | - | - | ± 0.02 | dB |
| Stopband Attenuation | SA | 54 | - | - | dB |
| Group Delay (Note 13) | GD | - | 19.3 | - | 1/fs |
| **Digital Filter + LPF** | | | | | |
| Frequency Response | | | | | |
| fs=44.1kHz, 20.0kHz | FR | - | ± 0.05 | - | dB |
| fs=96kHz,   40.0kHz | FR | - | ± 0.05 | - | dB |
| fs=192kHz,  80.0kHz | FR | - | ± 0.05 | - | dB |

Note 12. The passband and stopband frequencies scale with fs (system sampling rate).
        For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.
Note 13. Calculated delay time caused by the digital filter. This time is measured from setting the 16/24bit data
        of both channels to input register to the output of the analog signal.

## DC CHARACTERISTICS

(Ta = 25°C; VDD=CVDD = +3.0 ~ +3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| High-Level Input Voltage | VIH | 70%VDD | - | - | V |
| Low-Level Input Voltage | VIL | - | - | 30%VDD | V |
| High-Level Output Voltage    (Iout = -80uA) | VOH | VDD-0.4 | - | - | V |
| Low-Level Output Voltage    (Iout =  80uA) | VOL | - | - | 0.4 | V |
| Input Leakage Current  (Note 14) | Iin | - | - | ± 10 | μA |

Note 14. The SMUTE and DIF pins are not included. The SMUTE pin has an internal pull-down resistor (typ.100kΩ).
        The DIF pin has an internal pull-up resistor (typ.100kΩ).

**SWITCHING CHARACTERISTICS**

(Ta = 25°C; VDD=CVDD = +3.0 ~ +3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Master Clock Frequency** | fCLK | 4.096 | | 36.864 | MHz |
| Duty Cycle | dCLK | 40 | | 60 | % |
| **LRCK Frequency** | | | | | |
| Normal Speed Mode | fsn | 8 | | 48 | kHz |
| Double Speed Mode | fsd | 32 | | 96 | kHz |
| Quad Speed Mode | fsq | 120 | | 192 | kHz |
| Duty Cycle | Duty | 45 | | 55 | % |
| **Audio Interface Timing** | | | | | |
| BICK Period | | | | | |
| Normal Speed Mode | tBCK | 1/128fsn | | | ns |
| Double Speed Mode | tBCK | 1/64fsd | | | ns |
| Quad Speed Mode | tBCK | 1/64fsq | | | ns |
| BICK Pulse Width Low | tBCKL | 30 | | | ns |
| Pulse Width High | tBCKH | 30 | | | ns |
| BICK "↑" to LRCK Edge (Note 15) | tBLR | 20 | | | ns |
| LRCK Edge to BICK "↑" (Note 15) | tLRB | 20 | | | ns |
| SDTI Hold Time | tSDH | 20 | | | ns |
| SDTI Setup Time | tSDS | 20 | | | ns |

Note 15. BICK rising edge must not occur at the same time as LRCK edge.

■ **Timing Diagram**
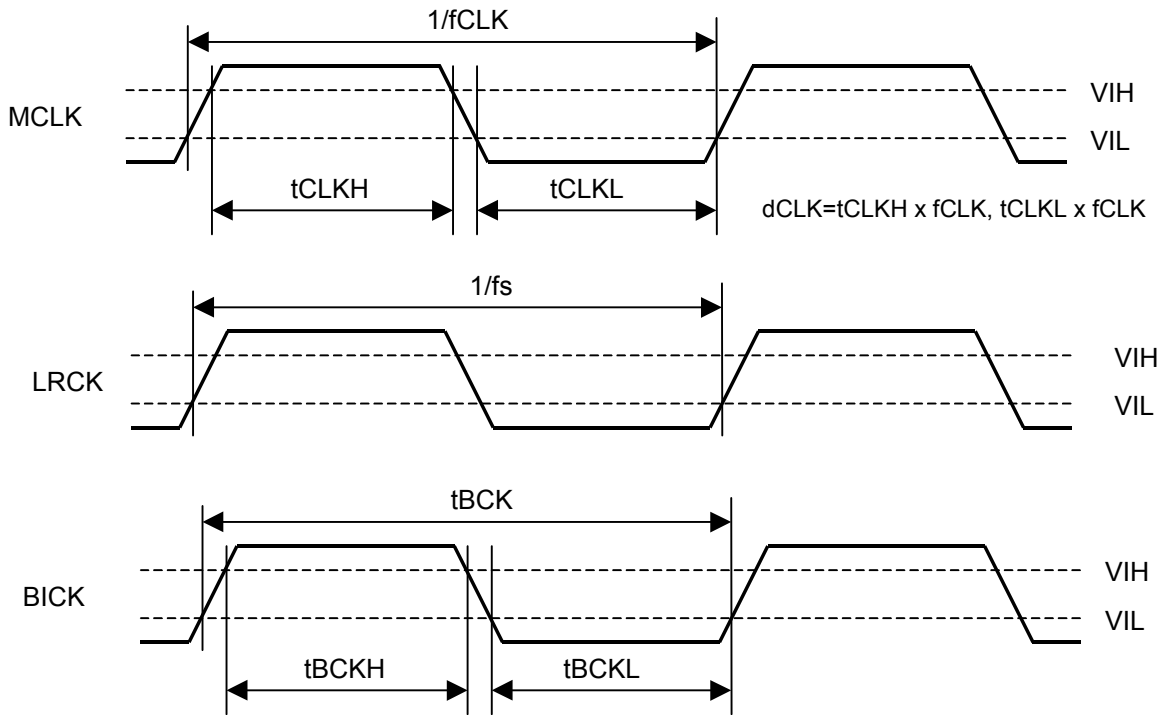


Figure 1. Clock Timing
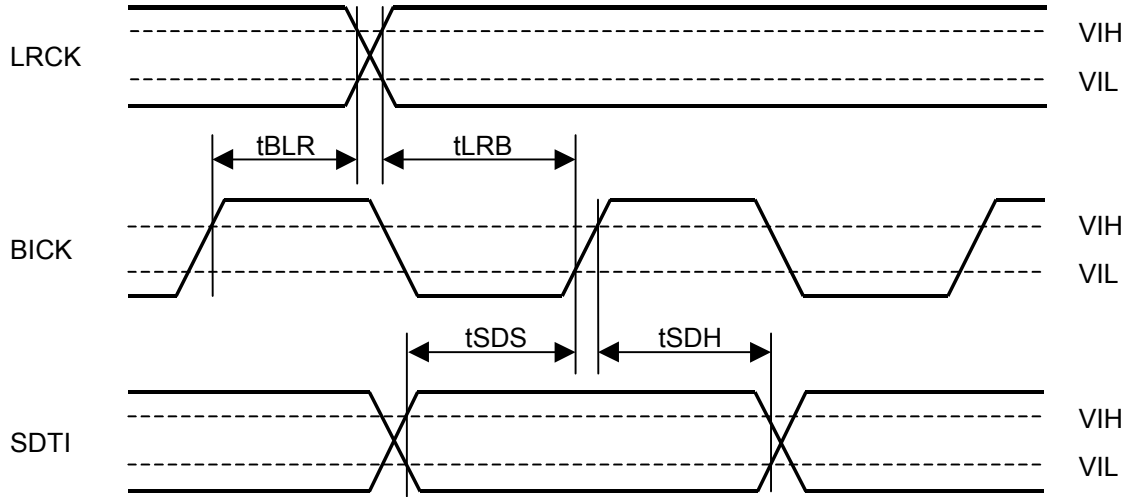


Figure 2. Serial Interface Timing

# OPERATION OVERVIEW

## ■ System Clock

The external clocks required to operate the AK4421A are MCLK, LRCK, and BICK. The master clock (MCLK) should be synchronized with LRCK, but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. Sampling speed and MCLK frequency are detected automatically, and then the internal master clock is set to the appropriate frequency (Table 1).

The AK4421A is automatically placed in power saving mode when MCLK, LRCK and BICK stop during normal operation mode, and the analog output goes to 0V(typ). When MCLK, LRCK and BICK are input again, the AK4421A is powered up. After exiting reset following power-up, the AK4421A is not fully operational until MCLK, LRCK and BICK are input.

| LRCK | MCLK (MHz) | | | | | | | Sampling |
|------|-------|-------|---------|---------|---------|---------|---------|----------|
| fs | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | 1152fs | Speed |
| 32.0kHz | - | - | - | - | 16.3840 | 24.5760 | 36.8640 | Normal |
| 44.1kHz | - | - | - | - | 22.5792 | 33.8688 | - | |
| 48.0kHz | - | - | - | - | 24.5760 | 36.8640 | - | |
| 32.0kHz | | | 8.192 | 12.288 | | | | Double |
| 44.1kHz | | | 11.2896 | 16.9344 | | | | |
| 48.0kHz | | | 12.288 | 18.432 | | | | |
| 88.2kHz | - | - | 22.5792 | 33.8688 | - | - | - | |
| 96.0kHz | - | - | 24.5760 | 36.8640 | - | - | - | |
| 176.4kHz | 22.5792 | 33.8688 | - | - | - | - | - | Quad |
| 192.0kHz | 24.5760 | 36.8640 | - | - | - | - | - | |

Table 1. System Clock Example

When MCLK= 256fs/384fs, the Auto Setting Mode supports sampling rate of 32kHz~96kHz (Table 1). But, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs (Table 2).

| MCLK | DR,S/N |
|------|--------|
| 256fs/384fs | 99dB |
| 512fs/768fs | 102dB |

Table 2. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

## ■ Audio Serial Interface Format

The audio data is shifted in via the SDTI pin using the BICK and LRCK inputs. The DIF pin can select between two serial data modes as shown in Table 3. In all modes the serial data is MSB-first, two's complement format and it is latched on the rising edge of BICK. In one cycle of LRCK, eight "H" pulses or more must not be input to the DIF pin.

| Mode | DIF | SDTI Format | BICK | Figure |
|------|-----|-------------|------|--------|
| 0 | L | 24bit MSB justified | ≥48fs | Figure 3 |
| 1 | H | 24bit I$^2$S | ≥48fs | Figure 4 |

Table 3. Audio Data Formats
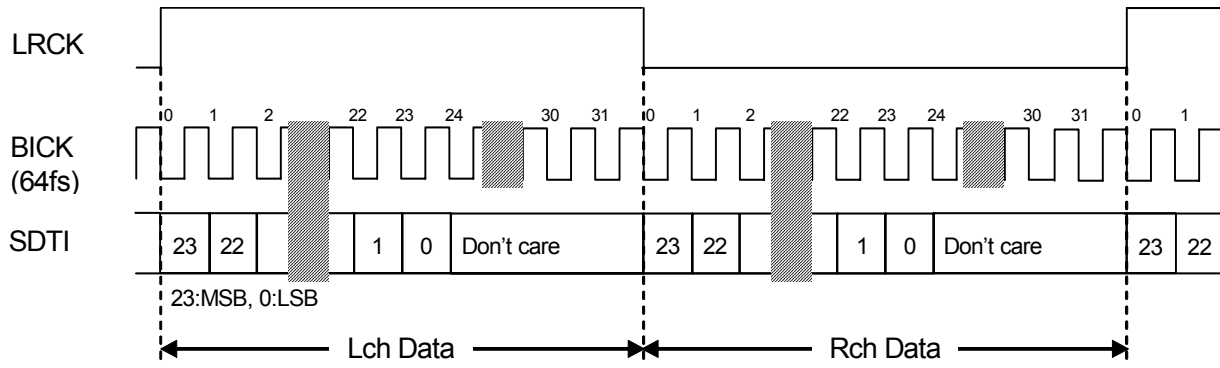
Figure 3. Mode 0 Timing
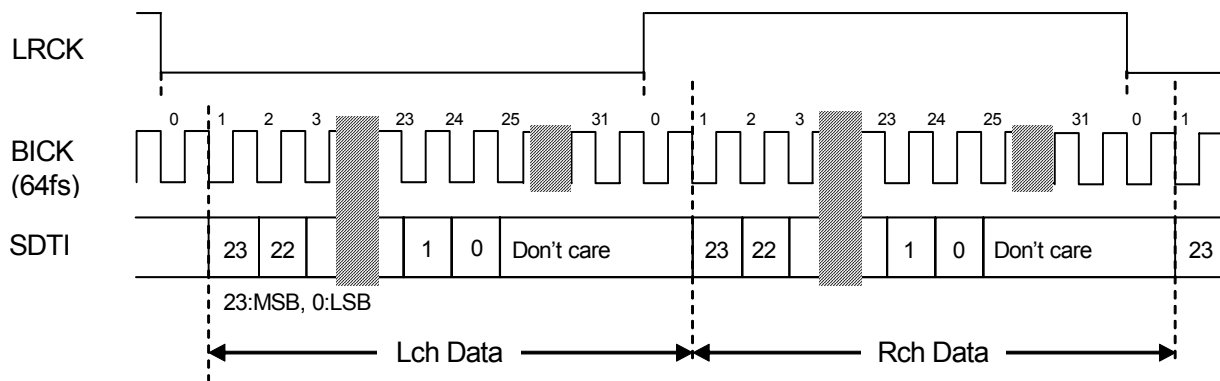


Figure 4. Mode 1 Timing

## ■ Zero Detect Function

When the input data for both channels are continuously zero for 8192 LRCK cycles, the DZF pin goes to "H". The DZF pin immediately returns to "L" if the input data for both channels are not zero.

## ■ Analog Output Block

The internal negative power supply generation circuit (Figure 5) provides a negative power supply for the internal 2Vrms amplifier. It allows the AK4421A to output an audio signal centered at VSS (0V, typ) as shown in Figure 6. The negative power generation circuit (Figure 5) needs 2.2uF capacitors (Ca, Cb) with low ESR (Equivalent Series Resistance). If this capacitor is polarized, the positive polarity pin should be connected to the CP and VSS2 pins. This circuit operates by clocks generated from MCLK. When MCLK stops, the AK4421A is placed in reset mode automatically and the analog outputs settle to VSS (0V, typ).
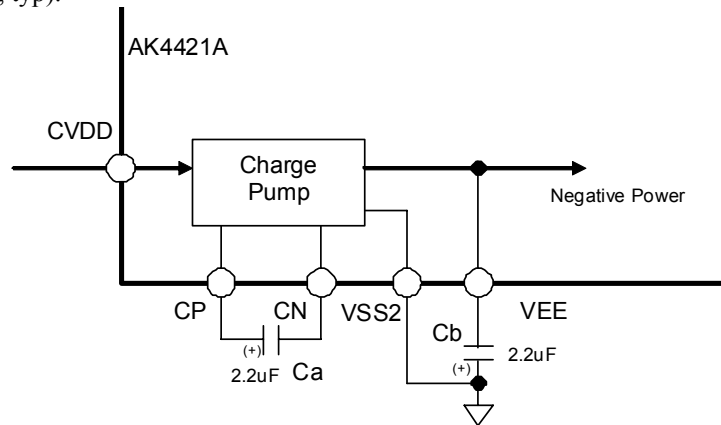
Figure 5. Negative Power Generation Circuit
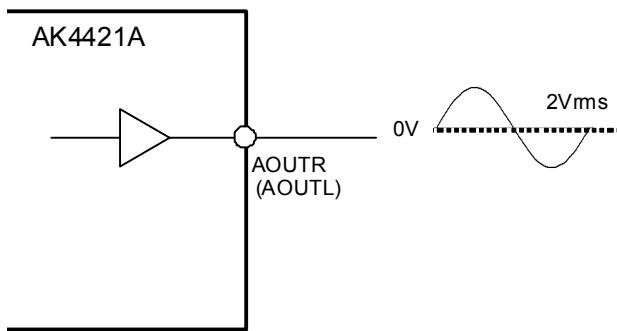
Figure 6. Audio Signal Output

## ■ Soft Mute Operation

Soft mute operation is performed in the digital domain. When the SMUTE pin is set "H", the output signal is attenuated to $-\infty$ in 1024 LRCK cycles. When the SMUTE pin is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB in 1024 LRCK cycles. If the soft mute is cancelled within the 1024 LRCK cycles after starting this operation, the attenuation is discontinued and it is returned to 0dB by the same cycle. Soft mute is effective for changing the signal source without stopping the signal transmission.
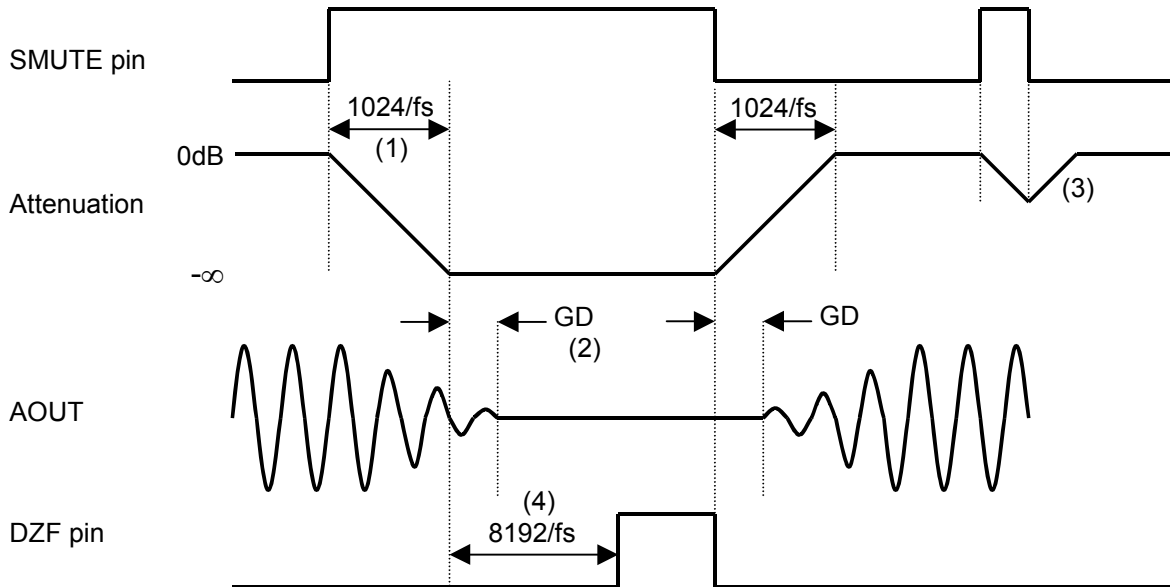


Notes:
    (1) The time for input data attenuation to $-\infty$ is :
        Normal Speed Mode: 1024 LRCK cycles (1024/fs).
        Double Speed Mode: 2048 LRCK cycles (2048/fs).
        Quad Speed Mode  : 4096 LRCK cycles (4096/fs).
    (2) The analog output corresponding to a specific digital input has a group delay, GD.
    (3) If soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to ATT level in the same cycle.
    (4) When the input data for both channels are continuously zero for 8192 LRCK cycles, the DZF pin goes to "H". The DZF pin immediately returns to "L" if the input data are not zero.

Figure 7. Soft Mute and Zero Detect Function

## ■ System Reset

The AK4421A is in power down mode upon power-up. The MLCK should be input after the power supplies are ramped up. The AK4421A is in power-down mode until LRCK are input.
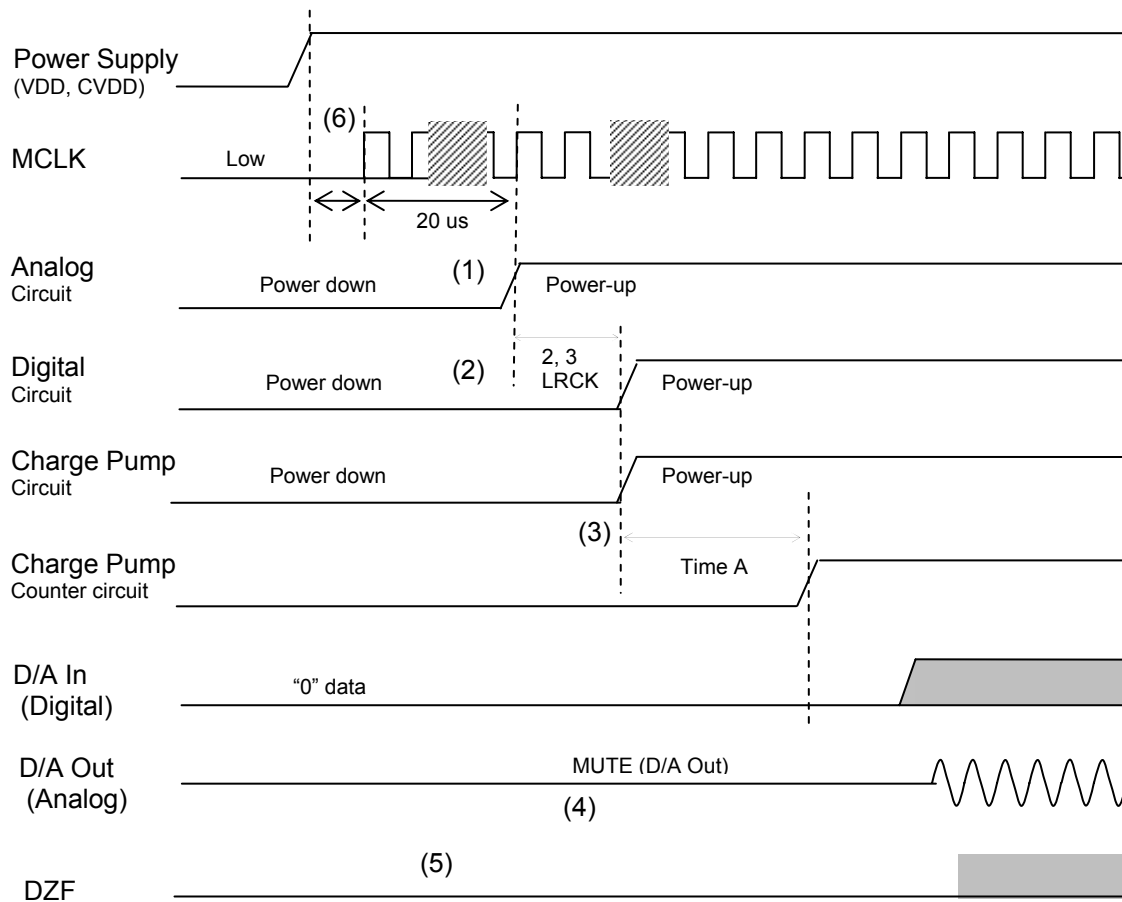


Notes:
(1) Approximately 20us after a MCLK input is detected, the internal analog circuit is powered-up.
(2) The digital circuit is powered-up after 2 or 3 LRCK cycles following the detection of MCLK.
(3) The charge pump counter starts after the charge pump circuit is powered-up. The DAC outputs a valid analog signal after Time A.
    Time A = 1024/ (fs x 16): Normal speed mode
    Time A = 1024/ (fs x 8): Double speed mode
    Time A = 1024/ (fs x 4): Quadruple speed mode
(4) No audible click noise occurs under normal conditions.
(5) The DZF pin is "L" in the power-down mode.
(6) The power supply must be powered-up when the MCLK pin is "L". MCLK must be input after 20us when the power supply voltage achieves 80% of VDD. If not, click noise may occur at a different time from this figure.

Figure 8. System Reset Diagram

## ■ Reset Function

When the MCLK or LRCK stops, the AK4421A is placed in reset mode and its analog outputs are set to VSS (0V, typ). When the MCLK and LRCK are restarted, the AK4421A returns to normal operation mode.
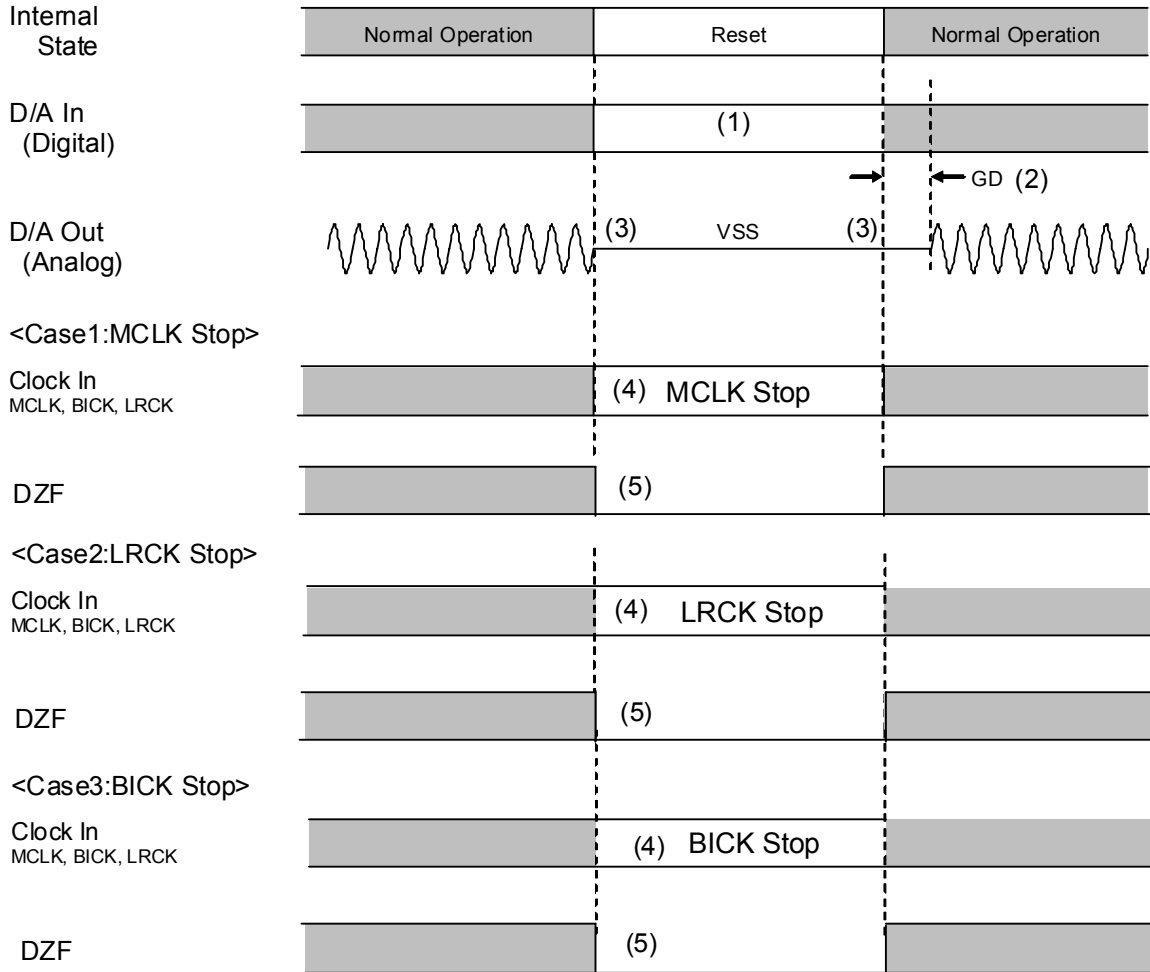


Notes:
 (1) Digital data can be stopped. The click noise after MCLK, LRCK and BICK are input again can be reduced by inputting the "0" data during this period.
 (2) The analog output corresponding to a specific digital input has group delay (GD).
 (3) No audible click noise occurs under normal conditions.
 (4) Clocks (MCLK, BICK, LRCK) can be stopped in the reset mode (MCLK, LRCK or BICK is stopped).
 (5) The DZF pin is set to "L" in the reset mode.

Figure 9. Reset Timing Example

AsahiKASEI                                                              [AK4421A]

**SYSTEM DESIGN**

Figure 10 shows the system connection diagram. An evaluation board (AKD4421A) is available for fast evaluation as well as suggestions for peripheral circuitry.
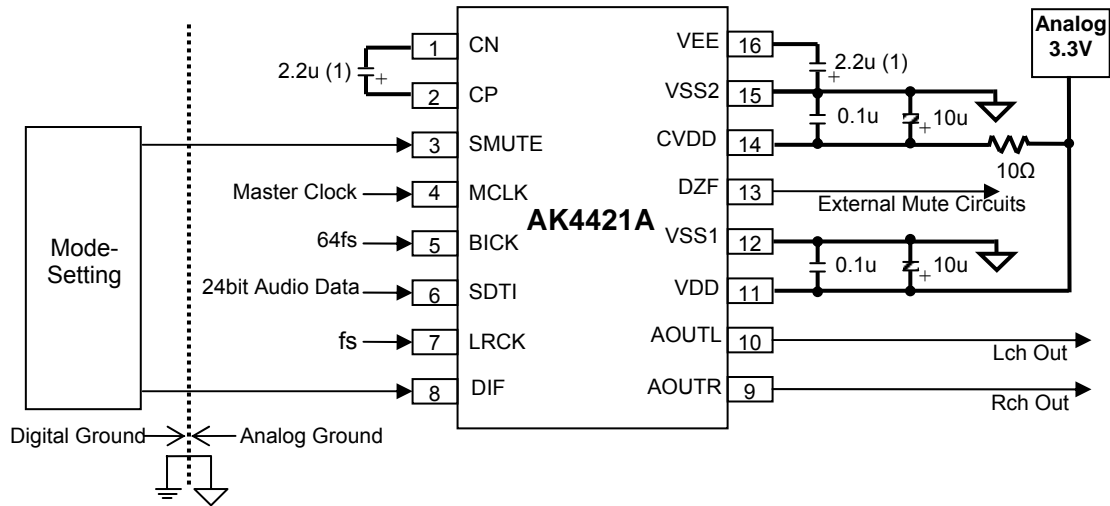


Note:
Use low ESR (Equivalent Series Resistance) capacitors. When using polarized capacitors, the positive polarity pin should be connected to the CP and VSS2 pin.
VSS1 and VSS2 should be separated from digital system ground.
Digital input pins should not be allowed to float.

Figure 10. Typical Connection Diagram

MS1086-E-01                                                              2009/09
- 15 -

## 1. Grounding and Power Supply Decoupling

VDD, CVDD and VSS are supplied from the analog supply and should be separated from the system digital supply. Decoupling capacitors, especially 0.1μF ceramic capacitors for high frequency bypass, should be placed as near to VDD and CVDD as possible. The differential voltage between VDD and VSS pins set the analog output range. **The power-up sequence between VDD and CVDD is not critical.**

## 2. Analog Outputs

The analog outputs are single-ended and centered around the VSS (ground) voltage. The output signal range is typically 2.0Vrms (typ @VDD=3.3V). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Using a 1st-order LPF (Figure 11) can reduce noise beyond the audio passband.

The output voltage is  positive full scale for 7FFFFFH (@24-bit data) and  negative full scale for 800000H (@24-bit data). The ideal output is 0V (VSS) for 000000H (@24bit). The DC offset is ±40mV or less.
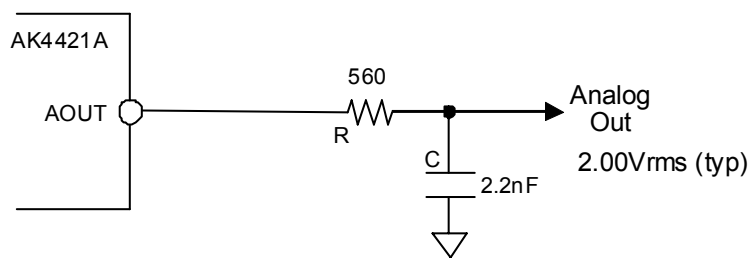


(fc = 129kHz, gain = -0.4dB @ 40kHz, gain = -1.4dB @ 80kHz)

Figure 11. External 1st order LPF Circuit Example

**PACKAGE**

# 16pin TSSOP (Unit: mm)

*5.0±0.1

16                    9

*4.4±0.1

1                     8

$\oplus$ | 0.13 | M

0.22±0.1          0.65

1.1 (max)

A

6.4±0.2

0.17±0.05

**Detail A**

Seating Plane

$\square$ | 0.10

0.1±0.1

0.5±0.2

0-10°
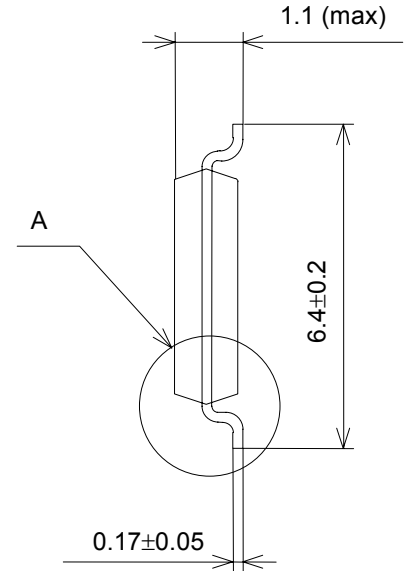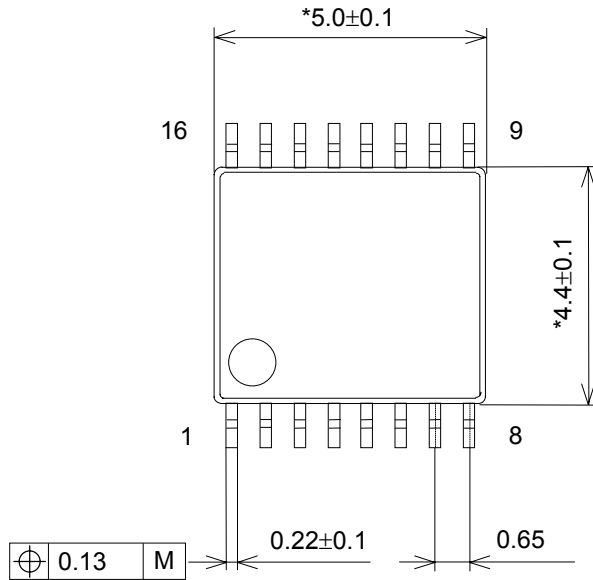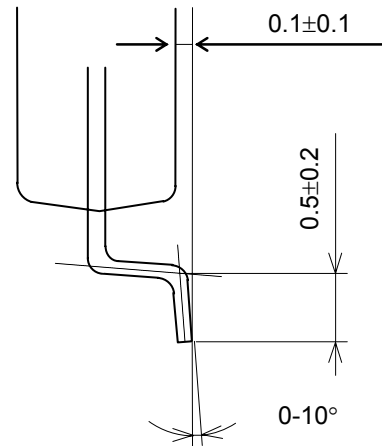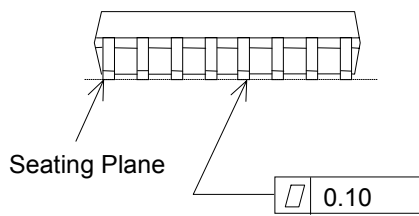
NOTE: Dimension "*" does not include mold flash.

## ■ Package & Lead frame material

Package molding compound:     Epoxy, Halogen (bromine and chlorine) free
Lead frame material:          Cu
Lead frame surface treatment: Solder (Pb free) plate

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**MARKING**
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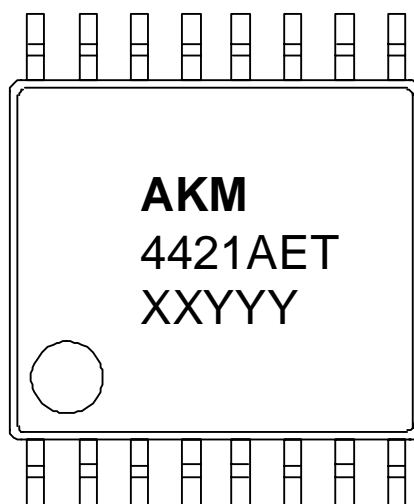


1) Pin #1 indication
2) Date Code : XXYYY (5 digits)
    XX:     Lot#
    YYY:   Date Code
3) Marketing Code : 4421AET
4) Asahi Kasei Logo

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**REVISION HISTORY**
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| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 09/07/03 | 00 | First Edition | | |
| 09/09/17 | 01 | Error Correction | 2 | Compatibility table was changed. Pin #8, AK4421A: DEM → DIF  Pin #8, AK4423: DIF → DEM |
| | | | 4 | Note 3 was changed. DEM was deleted. |