

FEATURES

- *Guaranteed Reset Assertion at $V_{CC} = 1V$*
- 1.5mA Maximum Supply Current
- SO-8 Packaging
- 4.65V Precision Voltage Monitor
- Power OK/Reset Time Delay: 200ms
- Minimum External Component Count
- Performance Specified Over Temperature
- Superior Upgrade for MAX699

APPLICATIONS

- Critical μP Power Monitoring
- Intelligent Instruments
- Computers and Controllers
- Automotive Systems

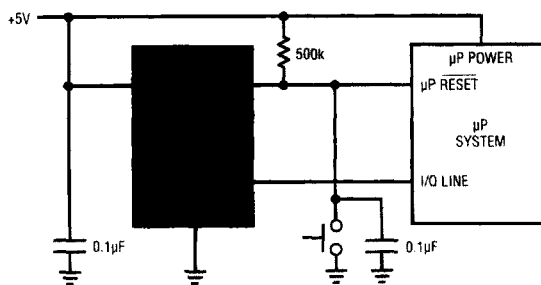
DESCRIPTION

The LTC699 provides power supply monitoring for microprocessor-based systems. The features include microprocessor reset and watchdog timing. Precise internal voltage reference and comparator circuit monitor the power supply line. When an out-of-tolerance condition occurs, the **RESET** output is forced to active low. In addition, the **RESET** output is guaranteed to remain logic low even with V_{CC} as low as 1V.

An internal watchdog timer is also available, which forces the **RESET** output to active low when the watchdog input is not toggled prior to the time-out period of 1.6 seconds.

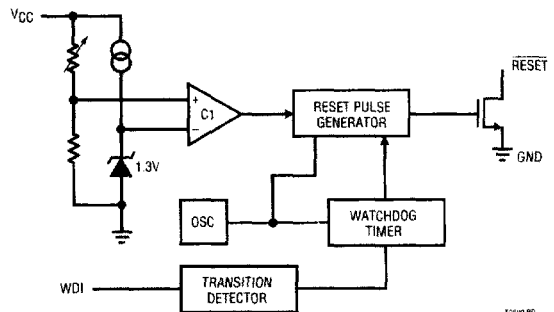
The LTC699 is offered in DIP and surface mount packages.

TYPICAL APPLICATION



MICROPROCESSOR RESET AND WATCHDOG TIMING IN A SINGLE CHIP FOR MICROPROCESSOR SYSTEMS.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Terminal Voltage

V_{CC} -0.3V to 6.0V

WDI Input -0.3V to V_{CC} + 0.3V

RESET Output -0.3V to 6V

Power Dissipation 500mW

Operating Temperature Range

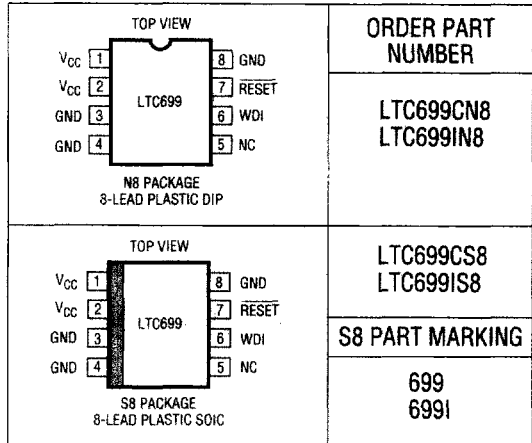
LTC699C 0°C to 70°C

LTC699I -40°C to 85°C

Storage Temperature Range -65°C to 150°C

Lead Temperature (Soldering, 10 sec.) 300°C

PACKAGE/ORDER INFORMATION



ELECTRICAL CHARACTERISTICS V_{CC} = +5V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	●	3.0		5.5	V
Supply Current	●		0.6	1.5	mA
	●		0.6	2.5	mA
Power Down Reset Assertion	●	4.5	4.65	4.75	V
Power Up Reset De-Assertion	●			4.75	V
Reset Threshold Hysteresis			40		mV
Reset Active Time		160	200	240	ms
	●	140	200	280	ms
Watchdog Time-out Period		1.2	1.6	2.0	sec
	●	1.0	1.6	2.25	sec
Reset Active Time PSRR			1		ms/V
Watchdog Time-out Period PSRR			8		ms/V
Minimum WDI Input Pulse Width	V _{IL} = 0.4, V _{IH} = 3.5V	●	200		ns
RESET output Voltage at V _{CC} = 1V (Note 3)	I _{SINK} = 10μA, V _{CC} = 1V		4	200	mV
RESET output Voltage	I _{SINK} = 1.6mA, V _{CC} = 4.25V			0.4	V
RESET Output Short Circuit Current	Output Sink Current		25		mA
WDI Input Threshold	Logic Low			0.8	V
	Logic High	2.0			V
WDI Input Current	WDI = V _{OUT}	●	4	50	μA
	WDI = 0V	●	-50	-8	μA

The ● denotes specifications which apply over the operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: RESET is active low, open drain output.

PIN FUNCTIONS

V_{CC}: +5V supply input. The V_{CC} pin should be bypassed with a 0.1 μ F capacitor.

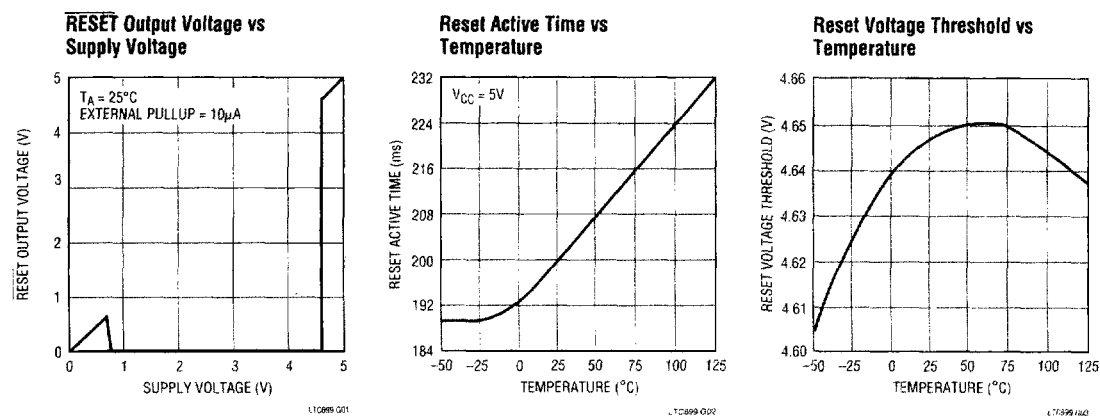
GND: Ground pin.

RESET: Open drain output for μ P reset control. When V_{CC} falls below the reset voltage threshold (4.65V typically), RESET goes active low. After V_{CC} returns to 5V, the reset pulse generator forces RESET to remain active low for a minimum of 140ms. When the watchdog timer is enabled

but not serviced prior to the time-out period, the reset pulse generator also forces RESET to active low for a minimum of 140ms for every time-out period (see Figure 2).

WDI: Watchdog Input, WDI, is a three level input. Driving WDI either high or low for longer than the watchdog time-out period forces RESET low. Floating WDI disables the Watchdog Timer. The timer resets itself with each transition of the Watchdog Input (see Figure 2).

TYPICAL PERFORMANCE CHARACTERISTICS



APPLICATIONS INFORMATION

Microprocessor Reset

The LTC699 uses a bandgap voltage reference and a precision voltage comparator C1 to monitor the 5V supply input V_{CC} (see BLOCK DIAGRAM). When V_{CC} falls below the reset voltage threshold, the RESET output is forced to active low state. The reset voltage threshold accounts for a 5% variation on V_{CC}, so the RESET output becomes active low when V_{CC} falls below 4.65V typical. On power-up, the RESET signal is held active low for a minimum of 140ms after reset voltage threshold is reached to allow the power supply and microprocessor to stabilize. On power-

down, the RESET signal remains active low even with V_{CC} as low as 1V. This capability helps hold the microprocessor in stable shutdown condition. Figure 1 shows the timing diagram of the RESET signal.

The precision voltage comparator, C1, typically has 40mV of hysteresis which ensures that glitches at V_{CC} pin do not activate the RESET output. Response time is typically 10 μ s. To help prevent mistriggering due to transient loads, V_{CC} pin should be bypassed with a 0.1 μ F capacitor with the leads trimmed as short as possible.

APPLICATIONS INFORMATION

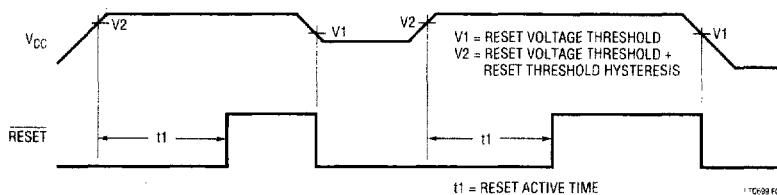


Figure 1. Reset Active Time

Watchdog Timer

The LTC699 provides a watchdog timer function to monitor the activity of the microprocessor. If the microprocessor does not toggle the Watchdog Input (WDI) within the time-out period, $\overline{\text{RESET}}$ is forced to active low for a minimum of 140ms. The watchdog time-out period is fixed at a 1.0 second minimum on the LTC699, which is adequate time for most systems to service the watchdog timer immediately after a reset. Figure 2 shows the timing diagram of watchdog time-out period and reset active time. The watchdog time-out period is restarted as soon

as $\overline{\text{RESET}}$ is inactive. When either a high-to-low or low-to-high transition occurs at the WDI pin prior to time-out, the watchdog time is reset and begins to time out again. To ensure the watchdog time does not time out, either a high-to-low or low-to-high transition on the WDI pin must occur at or less than the minimum time-out period. If the input to the WDI pin remains either high or low, reset pulses will be issued every 1.6 seconds typically. The watchdog time can be deactivated by floating the WDI pin. The timer is also disabled when V_{CC} falls below the reset voltage threshold.

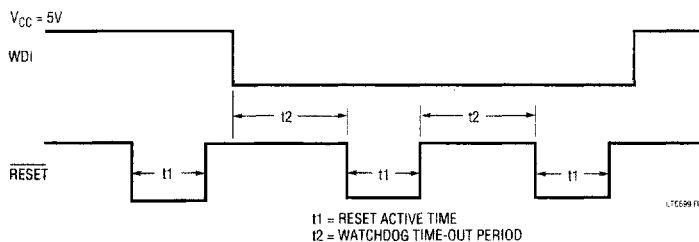


Figure 2. Watchdog Time-Out Period and Reset Active Time