KK74HCT244A

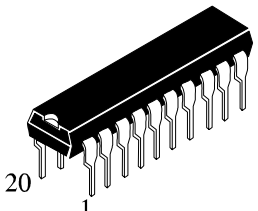
Octal 3-State Noninverting Buffer/Line Driver/Line Receiver

High-Performance Silicon-Gate CMOS

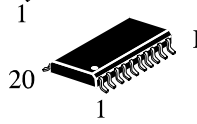
The KK74HCT244A is identical in pinout to the LS/ALS244. The device may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The KK74HCT244A is an octal noninverting buffer/line driver/line receiver designed to be used with 3-state memory address drivers, clock drivers, and other bus-oriented systems. The device has non-inverted outputs and two active-low output enables.

- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA



N SUFFIX
PLASTIC

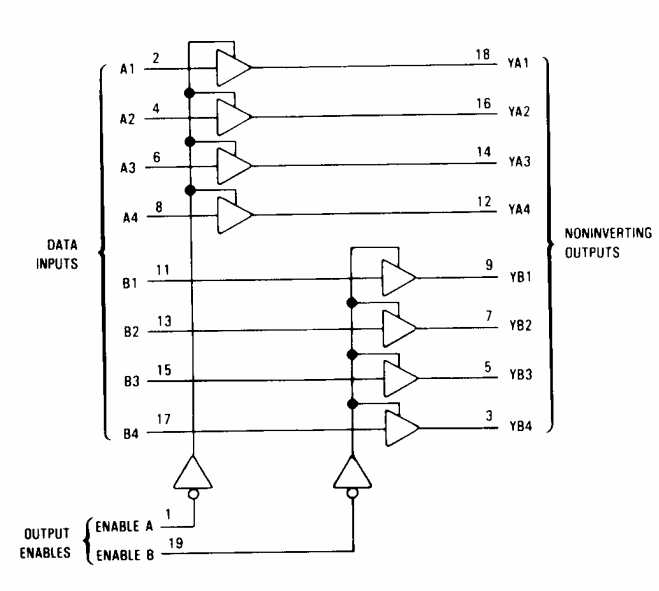


DW SUFFIX
SOIC

ORDERING INFORMATION

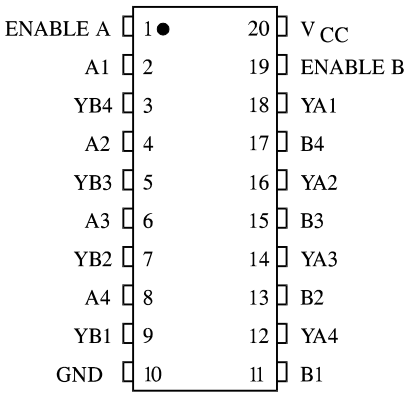
KK74HCT244AN Plastic
KK74HCT244ADW SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM



PIN 20=V_{CC}
PIN 10 = GND

PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A,B	YA,YB
L	L	L
L	H	H
H	X	Z

X=don't care;Z = high impedance

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V_{CC} +1.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Current, per Pin	±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±75	mA
P_D	Power Dissipation in Still Air, Plastic DIP** SOIC Package**	750 500	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
**Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	0	500	ns

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}= V_{CC}-0.1 V $\|I_{OUT}\| \le 20$ µA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.1 V $\|I_{OUT}\| \le 20$ µA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\| \le 20$ µA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{IN}=V_{IH} $\|I_{OUT}\| \le 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}= V_{IL} $\|I_{OUT}\| \le 20$ µA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{IN}= V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5	0.26	0.33	0.4	
I_{IH}	Minimum High-Level Input Leakage Current	V_{IN}=V_{CC}	5.5	0.1	1.0	1.0	µA
I_{IL}	Maximum Low-Level Input Leakage Current	V_{IN}=GND	5.5	-0.1	-1.0	-1.0	µA
I_{OZH}	Minimum High-Level Three-State Leakage Current	V_{IN}(01) =V_{IH} V_{IN}(19) =V_{IH} V_{IN} =V_{CC} (on other outputs) V_{OUT}=V_{CC}	5.5	0.5	5.0	10.0	µA
I_{OZL}	Maximum Low-Level Three-State Leakage Current	V_{IN}(01) =V_{IH} V_{IN}(19) =V_{IH} V_{IN} =V_{CC} (on other outputs) V_{OUT}=GND	5.5	-0.5	-5.0	-10.0	µA
I_{CC}	Maximum Quiescent Supply Current per Package)	V_{IL}=GND V_{IN}=V_{CC} I_{OUT}=0 µA	5.5	4.0	40	160	µA
ΔI_{CC}	Additional Quiescent Supply Current	V_{IN}=2.4 V, Any One Input V_{IN}=V_{CC} or GND, Other Inputs		≥-55°C		25°C to 125°C	mA
		I_{OUT}=0µA	5.5	2.9		2.4	

NOTE: Total Supply Current = I_{CC} + $\Sigma\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (V_{CC} =5.0 V ± 10%, C_L=50pF,Input t_r=t_f=6.0 ns)

Symbol	Parameter	Test Conditions	V_{CC} B	Guaranteed Limit			Unit
				25 °C to -55°C	≤85°C	≤125° C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to YA or B to YB (Figures 1 and 2)	V_{CC}=5 V±10% V_{IL}=0 V V_{IH}=3 V t_{LH}=t_{HL}=6 ns C_L=50 pF	5.0	20	25	30	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay , Output Enable to YA or YB (Figures 1 and 2)	V_{CC}=5 V±10% V_{IL}=0 V V_{IH}=3 V t_{LH}=t_{HL}=6 ns C_L=50 pF	5.0	26	33	39	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay , Output Enable to YA or YB (Figures 1 and 2)	V_{CC}=5 V±10% V_{IL}=0 V V_{IH}=3 V t_{LH}=t_{HL}=6 ns C_L=50 pF	5.0	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	V_{CC}=5 V±10% V_{IL}=0 V V_{IH}=3 V t_{LH}=t_{HL}=6 ns C_L=50 pF	5.0	12	15	18	ns
C_{IN}	Maximum Input Capacitance	V_{CC}=5 V±10%	5.0	10	10	10	pF
C_{OUT}	Maximum Three-State Output Capacitance (Output in High-Impedance State)	V_{CC}=5 V±10%	5.0	15	15	15	pF

C_{PD}	Power Dissipation Capacitance (Per Enabled Output) Used to determine the no-load dynamic power consumption: P_D=$C_{PD}V_{CC}^2f$+$I_{CC}V_{CC}$	Typical @25°C,V_{CC}=5.0 V 55	pF

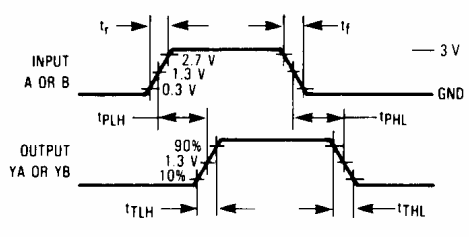


Figure 1. Switching Waveforms

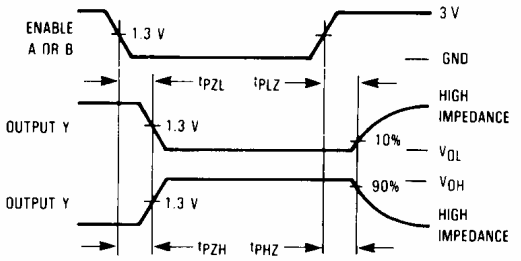


Figure 2. Switching Waveforms

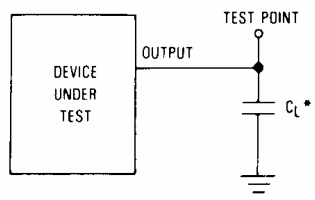


Figure 3. Test Circuit

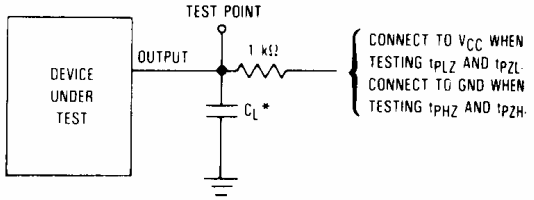
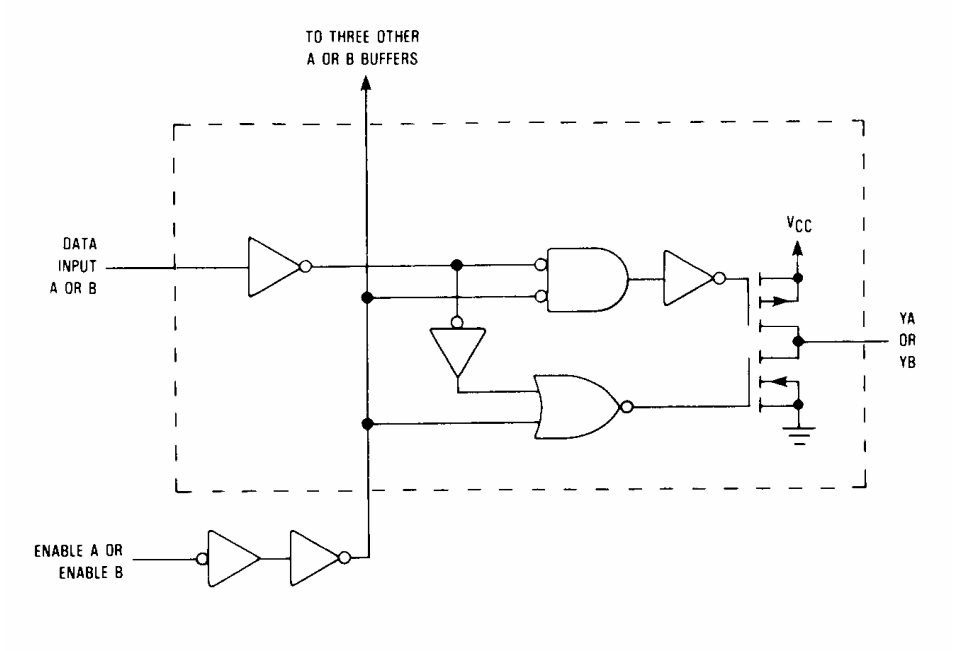


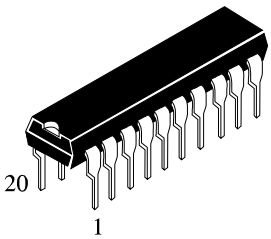
Figure 4. Test Circuit

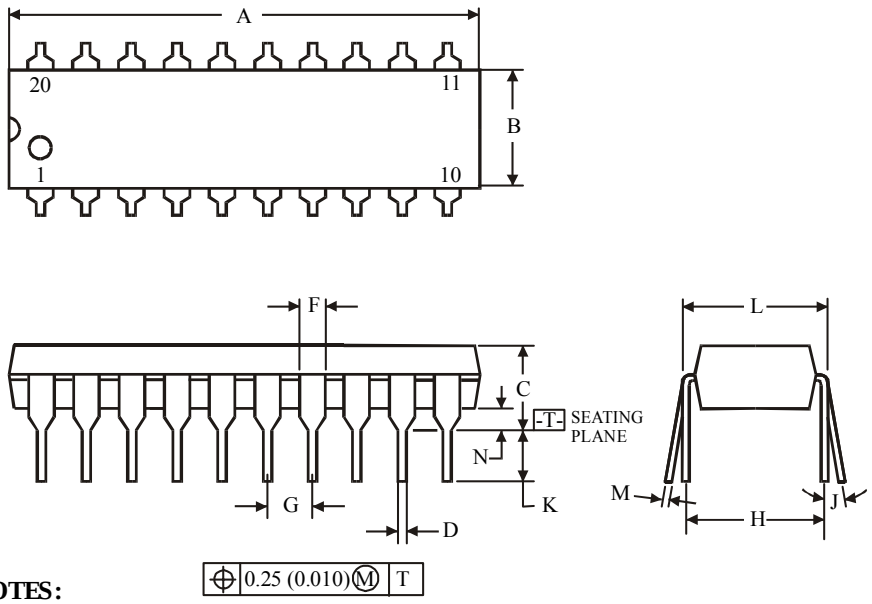
EXPANDED LOGIC DIAGRAM

(1/8 of the Device)



N SUFFIX PLASTIC DIP
(MS - 001AD)





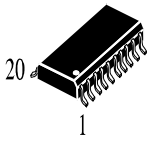
	Dimension, mm	
Symbol	MIN	MAX
A	24.89	26.92
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

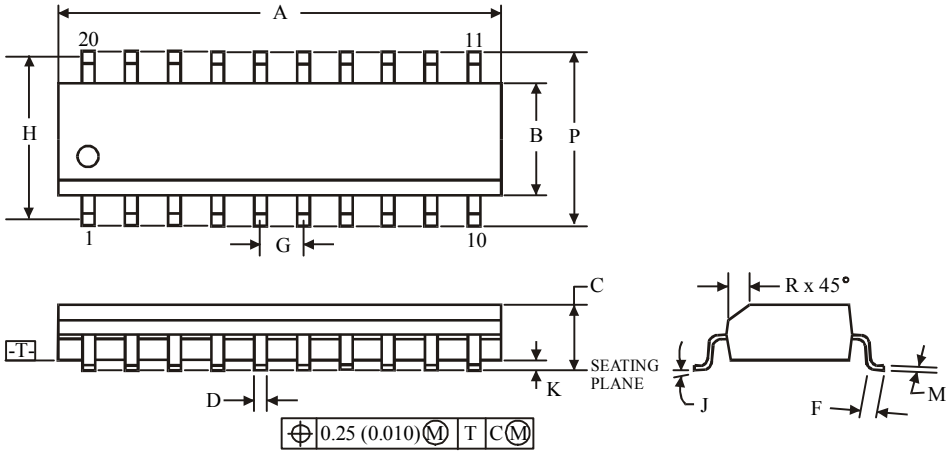
NOTES:

1. Dimensions “A”, “B” do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 013AC)





	Dimension, mm	
Symbol	MIN	MAX
A	12.6	13
B	7.4	7.6
C	2.35	2.65
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	9.53	
J	0°	8°
K	0.1	0.3
M	0.23	0.32
P	10	10.65
R	0.25	0.75

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.
2. Maximum mold flash or protrusion 0.15 mm (0.006) per side for A; for B – 0.25 mm (0.010) per side.