August 1983
PRELIMINARY

EUROTECHNIQUE

ETC 2716 16,384-BIT (2048 x 8) UV Erasable CMOS PROM

Parameter/Part Number	ETC 2716-1	ETC 2716	ETC 2716-5	ETC 2716-6
Access Time (ns)	350	450	550	650
Active Current (mA *a* 1 MHz)	5	5	5	5
Standby Current (mA)	0,1	0,1	0,1	0,1

General Description

The ETC 2716 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM ideally suited for applications where fast turn-around, pattern experimentation and low power consumption are important requirements.

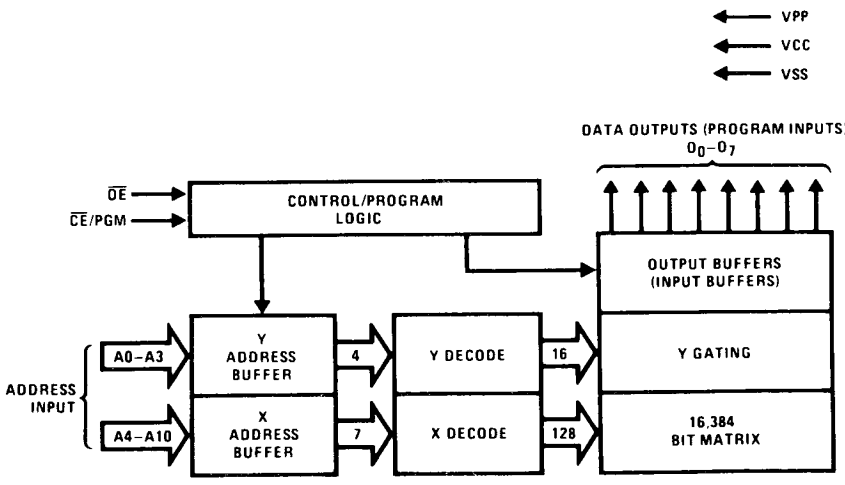
The ETC 2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

ThisEPROM is fabricated with the reliable, high volume, time proven, P²CMOS silicon gate technology.

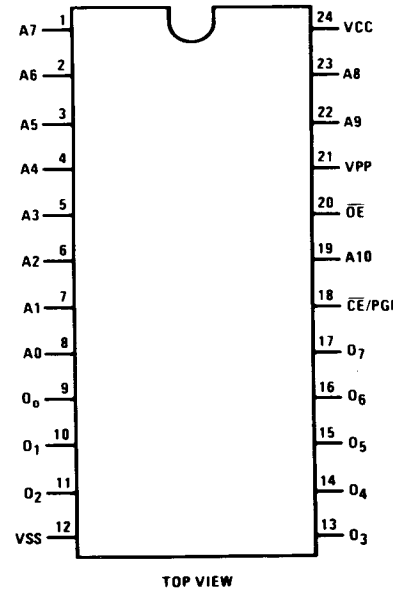
Features

- CMOS power consumption
- Performance compatible to ETC800 CMOS Microprocessor
- 2048 x 8 organization
- Pin compatible to 2716
- Access time down to 350 ns
- Single 5V power supply
- Static - no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- Three-state output with OR-tie capability

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Pin Connection During Read or Program

Mode	Pin Name/Number				
	CE/PGM 18	OE 20	VPP 21	VCC 24	Outputs 9-11, 13-17
Read	VIL	VIL	5	5	DOUT
Program	Pulsed VIL to VIH	VIH	25	5	DIN

Pin Names

A0-A10	Address Inputs
O_0-O_7	Data Outputs
CE/PGM	Chip Enable/Program
OE	Output Enable
VPP	Read 5V, Program 25V
VCC	5V
VSS	Ground

Printed in France

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to + 80°C	Output Voltages with Respect to VSS	VCC + 0.3V to VSS − 0.3V
Storage Temperature	−65°C to +125°C	Power Dissipation	1.0W
VPP Supply Voltage with Respect to VSS	26.5V to −0.3V	Lead Temperature (Soldering, 10 seconds)	300°C
Input Voltages with Respect to VSS (except VPP (Note 5)	6V to −0.3V		

READ OPERATION (Note 2)

DC Operating Characteristics TA = 0°C to +70°C, VCC = 5V ± 5%, VPP = VCC (Note 3), VSS = 0V, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
ILI	Input Current	VIN = VCC or GND				10	μA
ILO	Output Leakage Current	VOUT = 5.25V, $\overline{CE}$/PGM = VIH	27C16-45 27C16-55 27C16-65			10 10 10	μA
VIL	Input Low Voltage			−0.1		0.8	V
VIH	Input High Voltage	(Note 5)		2.2		VCC + 1	V
VOL1	Output Low Voltage	IOL = 2.1 mA				0.45	V
VOH1	Output High Voltage	IOH = −400 μA		2.4			V
VOL2	Output Low Voltage	IOL = 0 μA				0.1	V
VOH2	Output High Voltage	IOH = 0 μA		VCC − 0.1			V
IPP1	VPP Supply Current	VPP = 5.25V				10	μA
ICC1	VCC Supply Current Active (TTL Levels)	$\overline{CE}$/PGM, $\overline{OE}$ = VIL Addresses = VIH or VIL Frequency 1 MHz, I/O = 0 mA			2	10	mA
ICC2	VCC Supply Current Active (CMOS Levels)	$\overline{CE}$/PGM, $\overline{OE}$ = VIL (Note 5) Addresses = GND or VCC Frequency 1 MHz, I/O = 0 mA			1	5	mA
ICCSB1	VCC Supply Current Standby	$\overline{CE}$/PGM = VIH			0,1	1	mA
ICCSB2	VCC Supply Current Standby	$\overline{CE}$/PGM = VCC			0,01	0,1	mA

Capacitance (Note 4) TA = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ	Max	Units
CI	Input Capacitance	VIN = 0V	4	6	pF
CO	Output Capacitance	VOUT = 0V	8	12	pF

AC Test Conditions

Input Pulse Levels	0.8V to 2.2.V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and CL = 100 PF
Input and Output Timing Reference Levels	Input : 1V, 2V Output : 0.8V, 2V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Typical conditions are for operation at: TA = 25°C, VCC = 5V, VPP = VCC, and VSS = 0V.

Note 3: VPP may be connected to VCC except during program.

Note 4: Capacitance is guaranteed by periodic testing. TA = 25°C, f = 1 MHz.

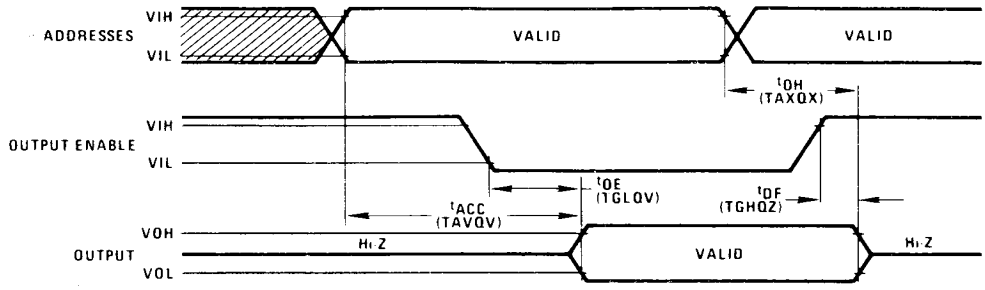
Note 5: The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V.

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, $V_{SS} = 0V$, unless otherwise noted.

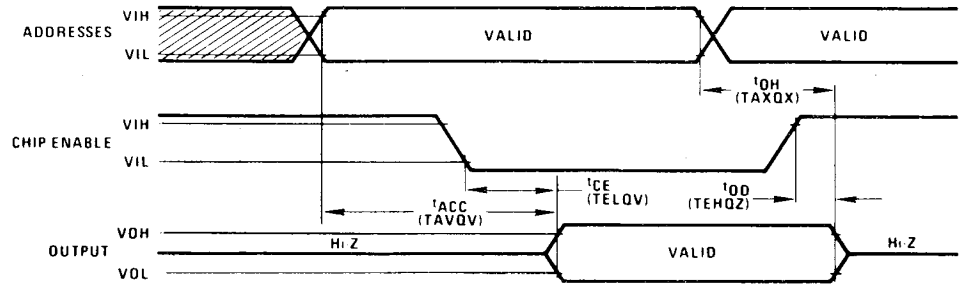
Symbol		Parameter	Conditions	ETC2716-1		ETC 2716		ETC 2716-5		ETC2716-6		UNITS
Alternate	Standard			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	TAVQV	Address to Output Delay	$\overline{CE}$/PGM = $\overline{OE}$ = VIL		350		450		550		650	ns
t_{CE}	TELQV	$\overline{CE}$ to Output Delay	$\overline{OE}$ = VIL		350		450		550		650	ns
t_{OE}	TGLQV	Output Enable to Output Delay	$\overline{CE}$/PGM = VIL		120		120		120		120	ns
t_{DF}	TGHQZ	Output Enable High to Output Hi-Z	$\overline{CE}$/PGM = VIL	0	100	0	100	0	100	0	100	ns
t_{OH}	TAXQX	Address to Output Hold	$\overline{CE}$/PGM = $\overline{OE}$ = VIL	0		0		0		0		ns
t_{OD}	TEHQZ	$\overline{CE}$ to Output Hi-Z	$\overline{OE}$ = VIL	0	100	0	100	0	100	0	100	ns

Switching Time Waveforms

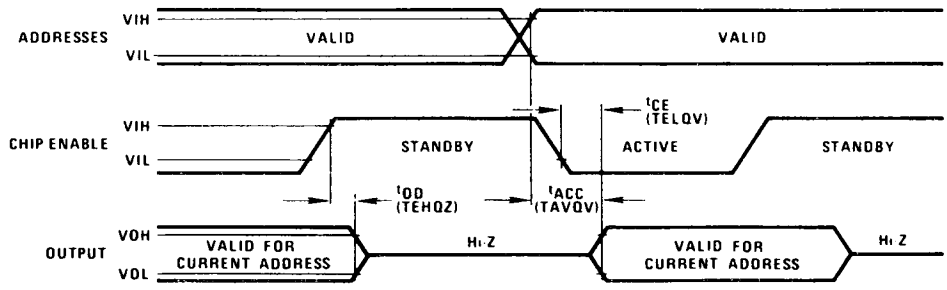
Read Cycle ($\overline{CE}$/PGM = VIL)



Read Cycle ($\overline{OE}$ = VIL)



Standby Power-Down Mode ($\overline{OE}$ = VIL)



PROGRAM OPERATION

DC Electrical Characteristics and Operating Conditions (Notes 1 and 2)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ± 1V)

Symbol	Parameter	Min	Typ	Max	Units
ILI	Input Leakage Current (Note 3)			10	μA
VIL	Input Low Level	−0.1		0.8	V
VIH	Input High Level (Note 7)	2.2		VCC+1	V
ICC	VCC Power Supply Current			10	mA
IPP1	VPP Supply Current (Note 4)			10	μA
IPP2	VPP Supply Current During Programming Pulse (Note 5)			30	mA

AC Characteristics and Operating Conditions (Notes 1, 2, and 6)

(TA = 25°C ± 5°C) (VCC = 5V ± 5%, VPP = 25V ±1V)

Symbol	Parameter	Min	Typ	Max	Units
t_{AS}	Address Set-up Time	2			μs
t_{OS}	$\overline{OE}$ Set-up Time	2			μs
t_{DS}	Data Set-up Time	2			μs
t_{AH}	Address Hold Time	2			μs
t_{OH}	$\overline{OE}$ Hold Time	2			μs
t_{DH}	Data Hold Time	2			μs
t_{DF}	Output Disable to Output Three state Delay (Note 4)	0		100	ns
t_{OE}	Output Enable to Output Delay (Note 4)			120	ns
t_{PW}	Program Pulse Width	45	50	55	ms
t_{PR}	Program Pulse Rise Time	5			ns
t_{PF}	Program Pulse Fall Time	5			ns
t_{VS}	VPP Set-Up Time	2			μs
t_{VH}	VPP Hold Time	2			μs

Note 1: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into a board with power applied.

Note 2: Care must be taken to prevent overshoot of the VPP supply when switching to + 26 V max

Note 3: O.V. ≤ VIN ≤ 5.25 V

Note 4: $\overline{CE}$/PGM = VIL, VPP = VCC.

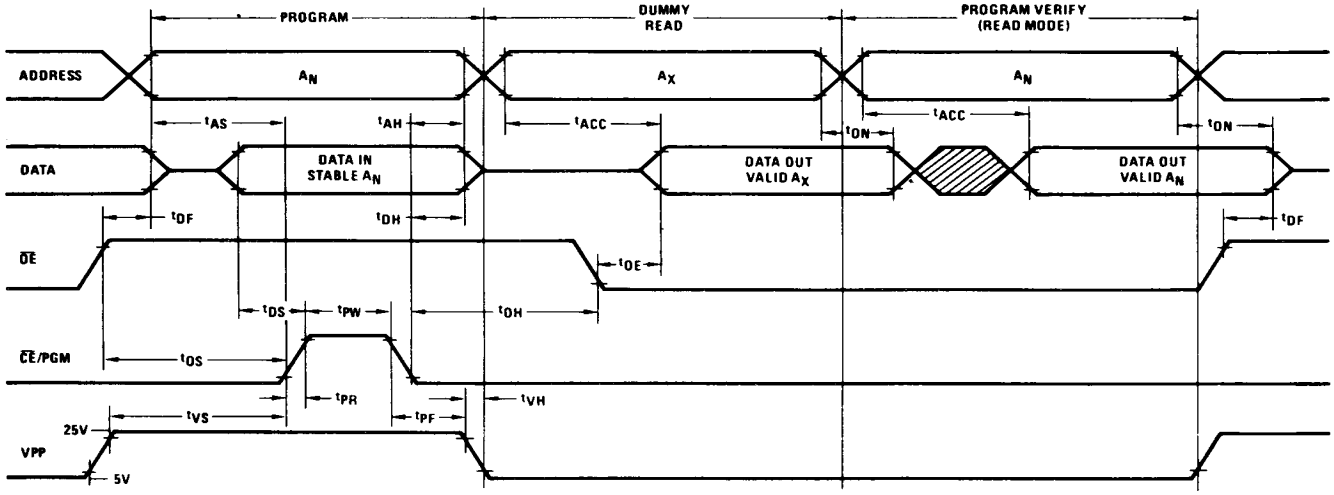
Note 5: VPP = 26 V

Note 6: Transition times ≤ 20 ns unless noted otherwise.

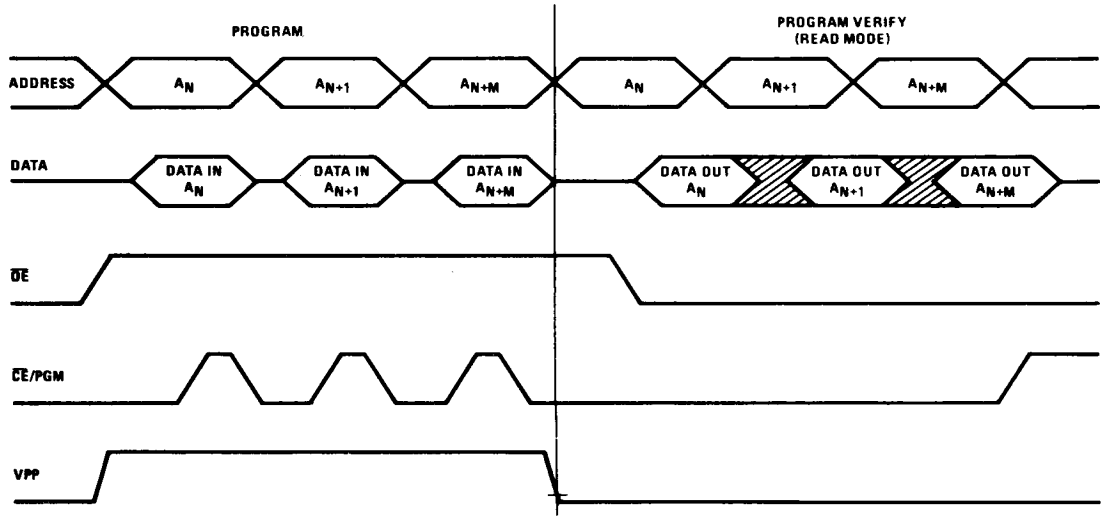
Note 7: The inputs (Address, $\overline{OE}$, $\overline{CE}$) may go above VCC by one volt with no latch up danger. Only the output (data inputs during programming) need be restricted to VCC + 0.3V to VSS − 0.3V.

PROGRAM Timing Diagrams

Single Address Programming Followed by a Verify Mode



Multiple Address Programming Followed by a Verify Mode*



* All timings are the same as the single address programming mode. A dummy read is required only if the last programmed byte is the first byte to be verified.

Functional Description

DEVICE OPERATION

The ETC 2716 has 3 modes of operation in the normal system environment. These are shown in Table I.

Read Mode

The ETC 2716 read operation requires that $\overline{OE}$ = VIL, $\overline{CE}$/PGM = VIL and that addresses A0–A10 have been stabilized. Valid data will appear on the output pins after t_{ACC}, t_{OE} or t_{CE} times (see Switching Time Waveforms) depending on which is limiting.

TABLE I. OPERATING MODES (VCC = 5V)

Mode	Pin Name/Number		
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	Outputs 9–11, 13–17
Read	VIL	VIL	DOUT
Deselect	Don't Care	VIH	Hi-Z
Standby	VIH	Don't Care	Hi-Z

Deselect Mode

The ETC 2716 is deselected by making $\overline{OE}$ = VIH. This mode is independent of $\overline{CE}$/PGM and the condition of the addresses. The outputs are Hi-Z when $\overline{OE}$ = VIH. This allows OR-tying 2 or more ETC 2716 for memory expansion.

Standby Mode (Power Down)

The ETC 2716 may be powered down to the standby mode by making $\overline{CE}$/PGM = VIH. This is independent of $\overline{OE}$ and automatically puts the outputs in their Hi-Z state. The power is reduced to 0.4% of the normal operating power. VCC must be maintained at 5V. Access time at power up remains either t_{ACC} or t_{CE} (see Switching Time Waveforms).

PROGRAMMING

The ETC 2716 is shipped from EUROTECHNIQUE completely erased. All bits will be at a "1" level (output high) in this initial state and after any full erasure. Table II shows the 3 programming modes.

Functional Description (Continued)

TABLE II. PROGRAMMING MODES (VCC = 5V)

Mode	Pin Name/Number			
	$\overline{CE}$/PGM 18	$\overline{OE}$ 20	VPP 21	Outputs Q 9-11, 13-17
Program	Pulsed VIL to VIH	VIH	25	DIN
Program Verify	VIL	VIL	25(5)	DOUT
Program Inhibit	VIL	VIH	25	Hi-Z

Program Mode

The ETC 2716 is programmed by introducing "0"s into the desired locations. This is done 8 bits (a byte) at a time. Any individual address, a sequence of addresses, or addresses chosen at random may be programmed. Any or all of the 8 bits associated with an address location may be programmed with a single program pulse applied to the chip enable pin. All input voltage levels, including the program pulse on chip enable are TTL compatible. The programming sequence is:

With VPP = 25V, VCC = 5V, $\overline{OE}$ = VIH and $\overline{CE}$/PGM = VIL, an address is selected and the desired data word is applied to the output pins. (VIL = "0" and VIL = "1" for both address and data.) After the address and data signals are stable the program pin is pulsed from VIL to VIH with a pulse width between 45 ms and 55 ms.

Multiple pulses are not needed but will not cause device damage. No pins should be left open. A high level (VIH or higher) *must not* be maintained longer than $t_{PW(MAX)}$ on the program pin during programming. ETC 2716 may be programmed in parallel with the same data in this mode.

Program Verify Mode

The programming of the ETC 2716 is verified in the program verify mode which has VPP at VCC (see Table II). **After programming an address, that same address cannot be immediately verified without an address change (dummy read).**

Program Inhibit Mode

The program inhibit mode allows programming several ETC 2716 simultaneously with different data for each one by controlling which ones receive the program pulse.
All similar inputs of the ETC 2716 may be paralleled.
Pulsing the program pin (from VIL to VIH) will program a unit while inhibiting the program pulse to a unit will keep it from being programmed and keeping $\overline{OE}$ = VIH will put its outputs in the Hi-Z state.

ERASING

The ETC 2716 is erased by exposure to high intensity ultraviolet light through the transparent window. This exposure discharges the floating gate to its initial state through induced photo current. It is recommended that the ETC 2716 be kept out of direct sunlight. The UV content of sunlight may cause a partial erasure of some bits in a relatively short period of time. Direct sunlight can also cause temporary functional failure. Extended exposure to room level fluorescent lighting will also cause erasure. An opaque coating (paint, tape, label, etc.) should be placed over the package window if this product is to be operated under these lighting conditions. Covering the window also reduces ICC due to photodiode currents.

An ultraviolet source of 2537Å yielding a total integrated dosage of 15 watt-seconds/cm^2 is required. This will erase the part in approximately 15 to 20 minutes if a UV lamp with a 12,000 μW/cm^2 power rating is used. The ETC 2716 to be erased should be placed 1 inch away from the lamp and no filters should be used.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at 1inch. The erasure time is increased by the square of the distance (if the distance is doubled the erasure time goes up by a factor of 4). Lamps lose intensity as they age. When a lamp is changed, the distance is changed, or the lamp is aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and system designs have been erroneously suspected when incomplete erasure was the basic problem.

Physical Dimensions inches (millimeters)