Am29C833A/Am29C853A

High-Performance CMOS Parity Bus Transceivers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-speed CMOS bidirectional bus transceivers**
  - T-R delay = 5 ns typical
  - R-Parity delay = 8 ns typical
- **Error flag with open-drain output**
- **Generates odd parity for all-zero protection**
- **Low standby power**
- **200 mV typical input hysteresis on input data ports**
- **Very high output drive**
  - I_{OL} = 48 mA Commercial, 32 mA Military
- **Proprietary edge-rate controlled outputs dramatically reduce ground bounce, overshoots and undershoots**
- **Power up/down disable circuit provides for glitch-free power supply sequencing**
- **Minimal speed degradation with multiple outputs switching**
- **Can be powered off while in 3-state, ideal for card edge interface applications**
- **JEDEC FCT-compatible specs**

GENERAL DESCRIPTION

The Am29C833A and Am29C853A are high-performance CMOS parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with the $\overline{ERR}$ flag showing the results of the parity test. Each of these devices is produced with AMD's exclusive CS11SA CMOS process, and features a typical propagation delay of 5 ns, as well as an output current drive of 48 mA.

In the Am29C833A, the error flag is clocked and stored in a register which is read at the open drain $\overline{ERR}$ output, the $\overline{CLR}$ input is used to clear the error flag register. In the Am29C853A, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29C833A and Am29C853A, parity logic defaults to the transmit mode so that the $\overline{ERR}$ pin reflects the parity of the R port.

The output enables, $\overline{OER}$ and $\overline{OET}$, are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both $\overline{OER}$ and $\overline{OET}$ simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

The Am29C833A and Am29C853A incorporate AMD's proprietary edge-controlled outputs in order to minimize simultaneous switching noise (ground bounce), overshoots and undershoots. By controlling the output transient currents, ground bounce and output ringing have been greatly reduced. A modified AMD output provides a stable, usable voltage level in less time than a non-controlled output.

Additionally, speed degradation due to increasing number of outputs switching is reduced. Together, these benefits of edge-rate control result in significant increase in system performance despite a minor increase in device propagation delay.*

A unique I/O circuit provides for high-impedance outputs during power-off and power-up/down sequencing, thus providing glitch-free operation for card-edge and other active bus applications.

The Am29C833A and Am29C853A are available in the standard package options: DIPs, PLCCs, and SOICs.

* For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

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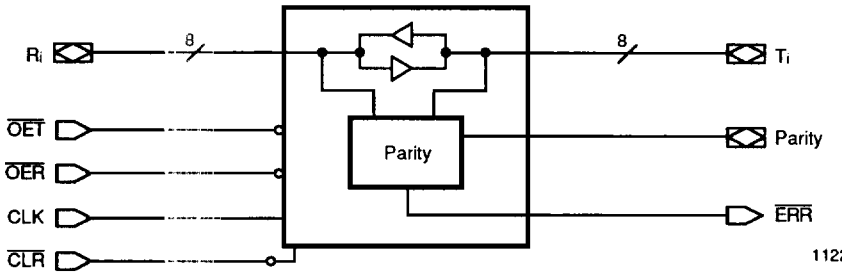
LOGIC SYMBOLS

Am29C833A



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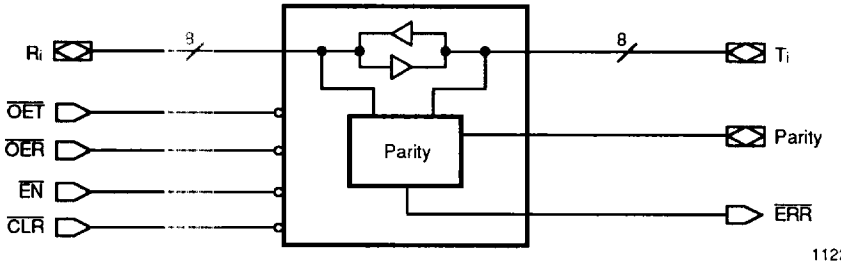
Am29C853A



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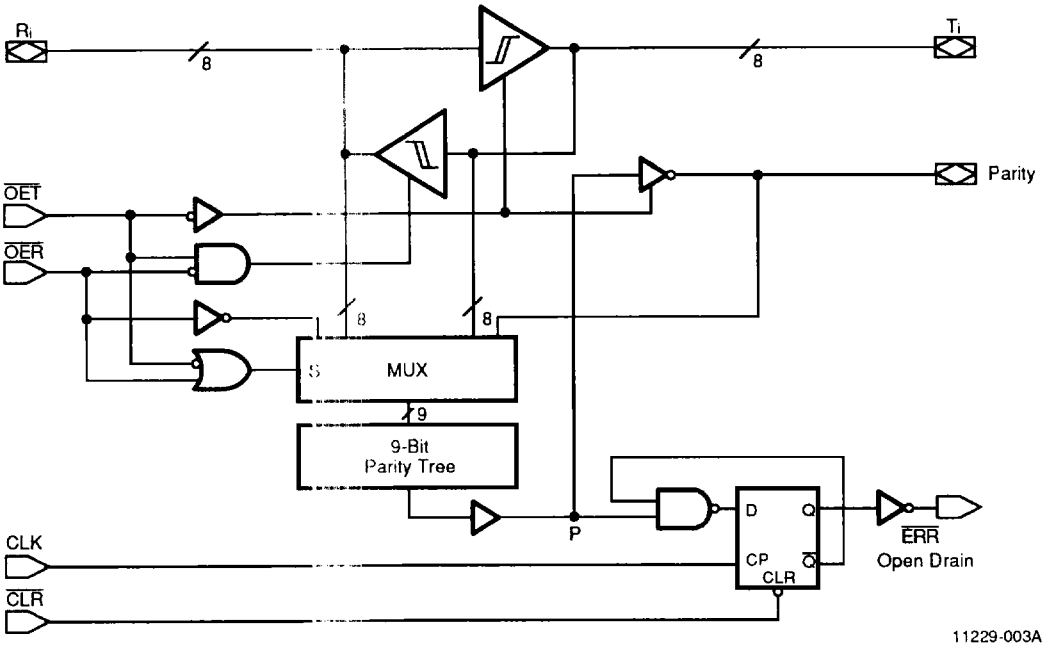
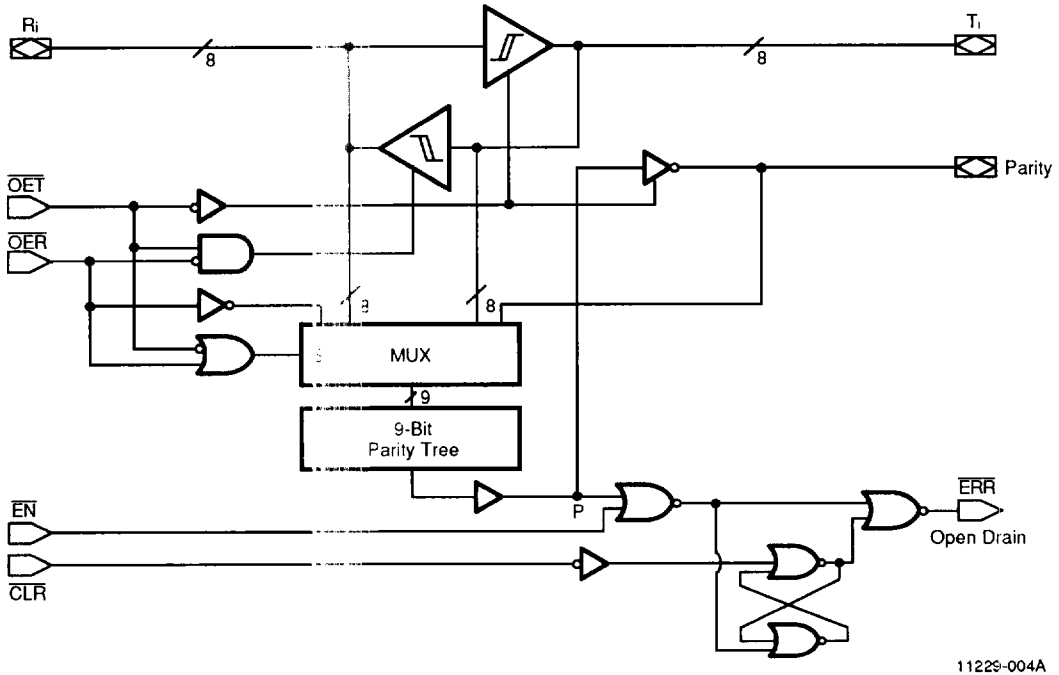
BLOCK DIAGRAMS

Am29C833A



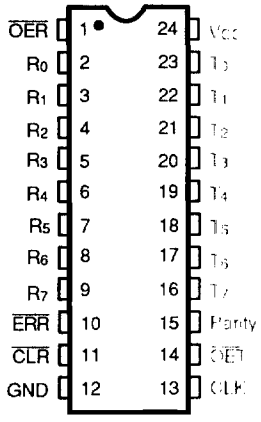
Am29C853A



CONNECTION DIAGRAMS (Top View)

Am29C833A

DIPs*



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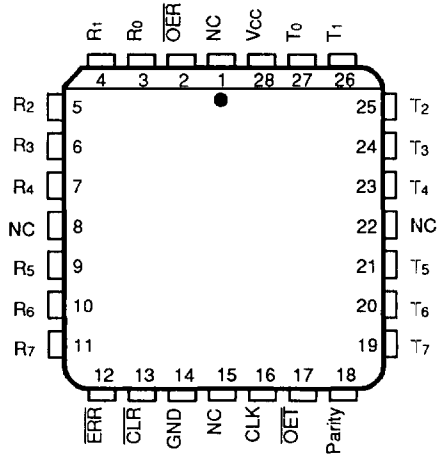
PLCC



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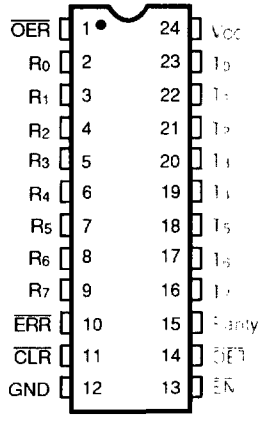
Am29C853A

DIPs*



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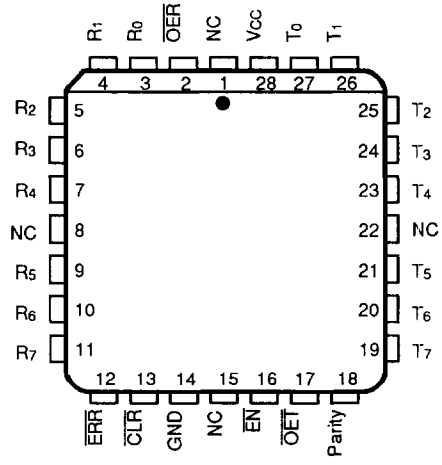
PLCC



11229-008A

*Also available in 24-Pin Small Outline package; pinout identical to DIPs.

FUNCTION TABLES

Am29C833A (Register Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	R	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care or Irrelevant
Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle
ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

Am29C853A (Latch Option)

Inputs								Outputs				
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	$\overline{EN}$	R_i	Sum of H's of R_i	T_i	Sum of H's (T_i + Parity)	R_i	T_i	Parity	$\overline{ERR}$	Function
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port, passes parity test resulting in error flag. Transmit path is disabled.
H	L	H	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	H	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	H	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH
L = LOW
↑ = LOW-to-HIGH Transition
X = Don't Care or Irrelevant
Z = High Impedance
NA = Not Applicable
* = Store the State of the Last Receive Cycle
ODD = Odd Number
EVEN = Even Number
i = 0, 1, 2, 3, 4, 5, 6, 7

TRUTH TABLES

Error Flag Output
Am29C833A

Inputs		Internal to Device	Outputs Pre-state	Output	
CLR	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

Error Flag Output
Am29C853A

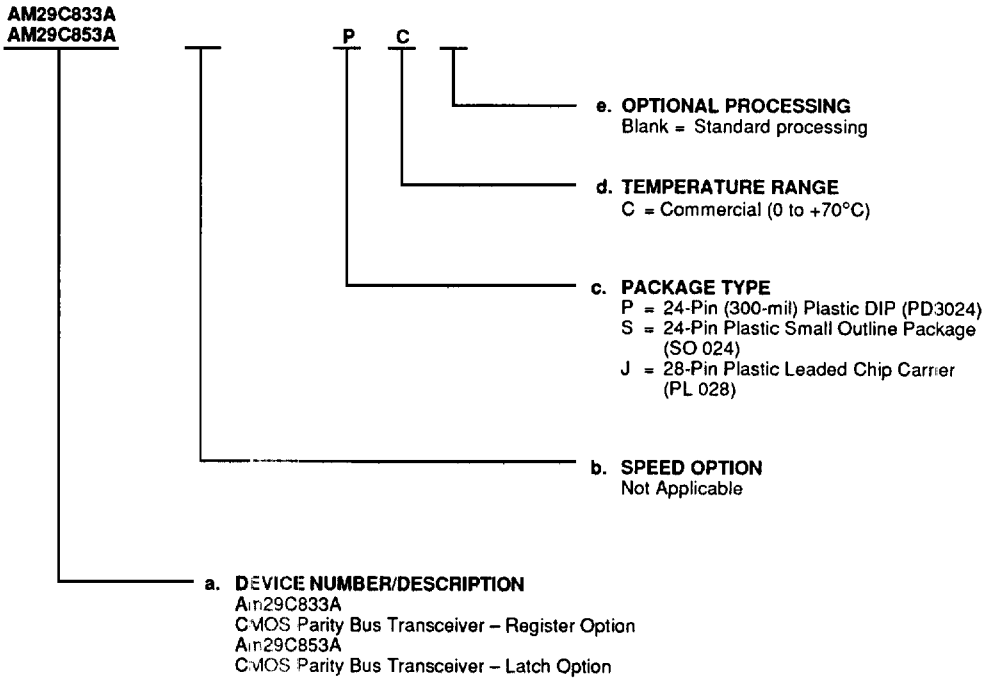
Inputs		Internal to Device	Outputs Pre-state	Output	
EN	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	Function
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's Capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note:
$\overline{OET}$ is HIGH and $\overline{OER}$ is LOW.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29C833A	PC, SC, JC
AM29C853A	

Valid Combinations

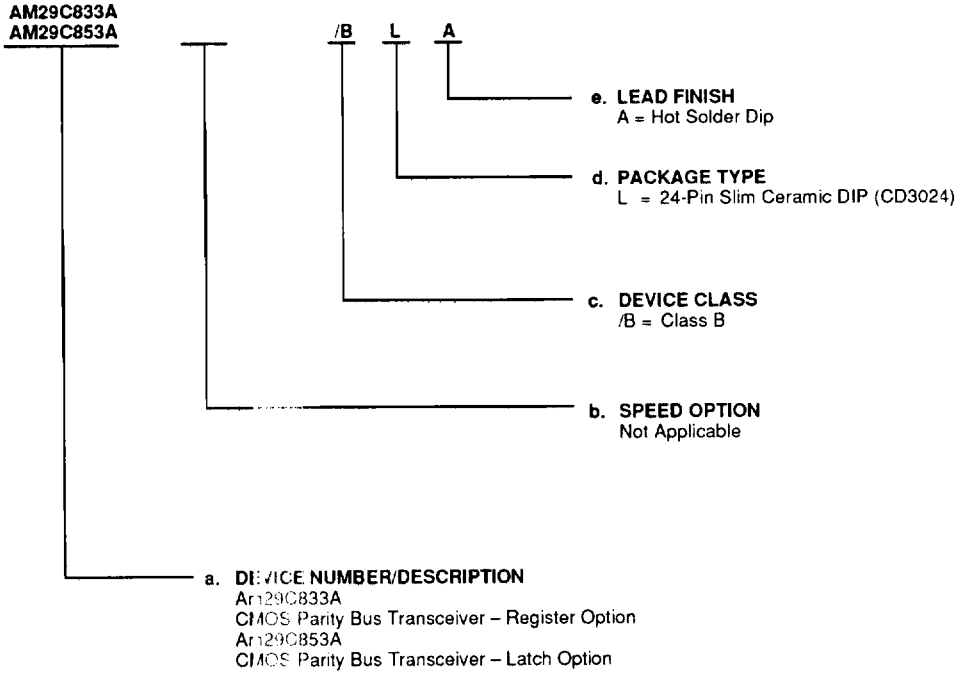
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. **Device Number**
b. **Speed Option (if applicable)**
c. **Device Class**
d. **Package Type**
e. **Lead Finish**



Valid Combinations	
AM29C833A	/BLA
AM29C853A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am29C833A/Am29C853A

$\overline{OER}$

Output Enable Receive (Input, Active LOW)

When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i and Parity are inputs).

$\overline{OET}$

Output Enable Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i and Parity are outputs).

R_i

Receive Port (Input/Output, Three-State)

R_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode

T_i

Transmit Port (Input/Output, Three-State)

T_i are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode

Parity

Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the T_i and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

Am29C833A Only

$\overline{ERR}$

Error Flag (Output, Open Drain)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the register is cleared.

$\overline{CLR}$

Clear (Input, Active LOW)

When $\overline{CLR}$ goes LOW, the Error Flag Register is cleared ($\overline{ERR}$ goes HIGH).

CLK

Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

Am29C853A Only

$\overline{ERR}$

Error Flag (Output, Open Drain)

In the Receive mode, the parity of the T_i bits is calculated and compared to the Parity input. $\overline{ERR}$ goes LOW when the comparison indicates a parity error. $\overline{ERR}$ stays LOW until the latch is cleared.

$\overline{CLR}$

Clear (Input, Active LOW)

When $\overline{CLR}$ goes LOW, the Error Flag latch is cleared ($\overline{ERR}$ goes HIGH).

$\overline{EN}$

Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Output Voltage	−0.5 V to +6.0 V
DC Input Voltage	−0.5 V to +6.0 V
DC Output Diode Current:	
Into Output	+50 mA
Out of Output	−50 mA
DC Input Diode Current:	
Into Input	+20 mA
Out of Input	−20 mA
DC Output Current per Pin:	
Into Output	+100 mA
Out of Output	−100 mA
Total DC Ground Current	
($n \times I_{OL} + m \times I_{CCT}$) mA (Note 1)	
Total DC V_{CC} Current	
($n \times I_{OH} + m \times I_{CCT}$) mA (Note 1)	

Note:

1. n = number of outputs, m = number of inputs.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Military (M) Devices

Ambient Temperature (T_A)	−55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V,	MIL I_{OL} = 32 mA			0.5	V
		V_{IN} = V_{IH} or V_{IL}	COM'L I_{OL} = 48 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage (Note 1)	Am29C853A	All Inputs	2		V
			Am29C833A				
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, Input Only		V_{IN} = 0.0 V		−5	µA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, Input Only		V_{IN} = 5.5 V		5	µA
I_{OZH}	Output Off-State Current	V_{CC} = 5.5 V, I/O Port		V_{OUT} = 5.5 V		10	µA
I_{OZL}	(High Impedance)	V_{CC} = 5.5 V, I/O Port		V_{OUT} = 0.0 V		−10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_O = 0 V (Note 2)			−60		mA
I_{CCQ}	Static Supply Current	V_{CC} = 5.5 V Outputs Open	V_{IN} = V_{CC} or GND	MIL		1.5	mA
				COM'L		1.2	
I_{CCT}			V_{IN} = 3.4 V	R_i, T_i, Parity		1.5	mA/ Bit
				$\overline{CLR}$, CLK, (Note 4) $\overline{OET}$, $\overline{OER}$		3.0	
I_{CCD}†	Dynamic Supply Current	V_{CC} = 5.5 V (Note 3)		Outputs Open		275	µA/ MHz/ Bit
				Outputs Loaded		400	

Notes:

1. Input thresholds are tested in combination with other DC parameters or by correlation.
2. Not more than one output shorted at a time, duration should not exceed 100 milliseconds.
3. Measured at a frequency ≤ 10 MHz with 50% duty cycle.
4. For Am29C853A, replace CLK with $\overline{EN}$.

† Not included in Group A tests.

SWITCHING CHARACTERISTICS for light capactive loading over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Symbol	Parameter Description		Test Conditions*	Commercial		Military		Unit
				Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay to R_i to T_i,		C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω	2	10.5	2	12	ns
t_{PHL}	T_i to R_i (Note 3)			2	10.5	2	12	ns
t_{PLH}	Propagation Delay R_i to Parity			4	13	4	14.5	ns
t_{PHL}				4	13	4	14.5	ns
t_{ZH}	Output Enable Time ($\overline{OER}$, $\overline{OET}$ to R_i, T_i			2	10.5	2	12	ns
t_{ZL}	and Parity			2	10.5	2	12	ns
t_{HZ}	Output Disable Time ($\overline{OER}$, $\overline{OET}$ to R_i, T_i			1.5	10.5	1.5	12	ns
t_{LZ}	and Parity			1.5	10.5	1.5	12	ns
t_S	T_i, Parity to CLK Setup Time (Note 1)			8		10		ns
t_H	T_i, Parity to CLK	Am29C833A		0		2		ns
	Hold Time (Note 1)	Am29C853A		1		3		ns
t_{REC}	Clear ($\overline{CLR}$ ↓) to CLK Setup Time (Note 2)			2		4		ns
t_{PWH}	Clock Pulse Width (Note 1)	HIGH		6		9		ns
t_{PWL}		LOW		6		9		ns
t_{PWL}	Clear Pulse Width	LOW		6		9		ns
t_{PHL}	Propagation Delay CLK to $\overline{ERR}$ (Note 1)			2	10	2	14	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$			8	18	8	21	ns
t_{PLH}	Propagation Delay T_i Parity to $\overline{ERR}$			6	19	6	21	ns
t_{PHL}	(PASS Mode Only) Am29C853A			6	19	6	21	ns
t_{PLH}	Propagation Delay $\overline{OE}$ to Parity			2	13	2	15	ns
t_{PHL}				2	13	2	15	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For Am29C853A, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833A.
3. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).

SWITCHING CHARACTERISTICS for heavy capacitive loading over operating ranges unless otherwise specified (Note 4)

Symbol	Parameter Description	Test Conditions*	Commercial		Military		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay to R_i to T_i,	C_L = 300 pF R_1 = 500 Ω R_2 = 500 Ω	2	14	2	15.5	ns
t_{PHL}	T_i to R_i (Note 3)		2	15	2	16.5	ns
t_{PLH}	Propagation Delay T_i to Parity		4	18	4	19.5	ns
t_{PHL}			4	18	4	19.5	ns
t_{ZH}	Output Enable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i		2	14	2	15.5	ns
t_{ZL}	and Parity		2	18.5	2	20.0	ns
t_{PLH}	Propagation Delay $\overline{OER}$ to Parity		2	18	2	20	ns
t_{PHL}			2	17	2	19	ns
t_{HZ}	Output Disable Time $\overline{OER}$, $\overline{OET}$ to R_i, T_i	C_L = 5 pF R_1 = 500 Ω R_2 = 500 Ω	1.5	7	1.5	8.5	ns
t_{LZ}	and Parity		1.5	7	1.5	8.5	ns

*See Test Circuit and Waveforms listed in Chapter 2.

Notes:

1. For Am29C853A, replace CLK with $\overline{EN}$.
2. Applies only to Am29C833A.
3. For more details refer to a Minimization of Ground Bounce Through Output Edge-Rate Control Application Note (See Chapter 3).
4. These parameters are guaranteed by characterization but not production tested.