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AK4213

Mono Class-D SPK-Amp with Stereo Cap-less HP-Amp

GENERAL DESCRIPTION

The AK4213 is an audio mono class-D speaker amplifier with stereo cap-less headphone amplifier. The AK4213 features analog mixing circuit that allow easy interfacing in mobile phone and portable A/V player designs. The input circuit supports both of single-ended and differential modes, and headphone supports stereo and mono modes. The speaker amplifier includes ALC (Automatic Level Control) circuit which is able to stabilize each output sound levels. The AK4213 is available in CSP package (3.0mm x 3.0mm), utilizing less board space than competitive offerings.

FEATURE

- ☐ **Single-ended / Differential Input**
- ☐ **Analog Mixing Circuit**
- ☐ **Analog Input Volume: +10dB to –20dB, 2dB step**
- ☐ **µP Interface: I^2C Bus (Ver1.0, 400 kHz Fast-Mode)**
- ☐ **Thermal Shutdown / Short Protection circuit**
- ☐ **Mono Class-D Speaker Amplifier:**
  - **BTL output**
  - **Output Power: 1.6W @ 8Ω, SVDD=5V**
    0.8W @ 8Ω, SVDD=3.6V
  - **THD+N: -65dB @ 8Ω, Po = 0.25W, SVDD=3.6V**
  - **Output Noise Level: 85µVrms**
  - **ALC (Automatic Level Control) Circuit**
  - **Bypass Mode**
  - **Pop Noise Free at Power-ON/OFF and Mute**
  - **External filter-less**
- ☐ **Stereo Cap-less Headphone Amplifier:**
  - **Mono / Stereo Mode**
  - **Output Power: 64mW x 2ch @ 16Ω, SVDD=3.3V, THD+N=-40dB**
  - **THD+N: -58dB @ 16Ω, Po=30mW, SVDD=3.3V**
  - **Output Noise Level: 24µVrms**
  - **Output Volume: +12dB to –50dB, 2dB Step**
  - **Pop Noise Free at Power-ON/OFF and Mute**
- ☐ **Power Supply:**
  - **Analog: 2.6V ~ 3.6V**
  - **Headphone Amplifier: 2.6V ~ 3.6V**
  - **Speaker Amplifier: 3.0V ~ 5.5V**
  - **Digital Interface: 1.6V ~ 3.6V**
- ☐ **Ta: –40 ~ 85°C**
- ☐ **Package: 29pin CSP (3.0mm x 3.0mm, 0.5mm pitch)**

■ Block Diagram

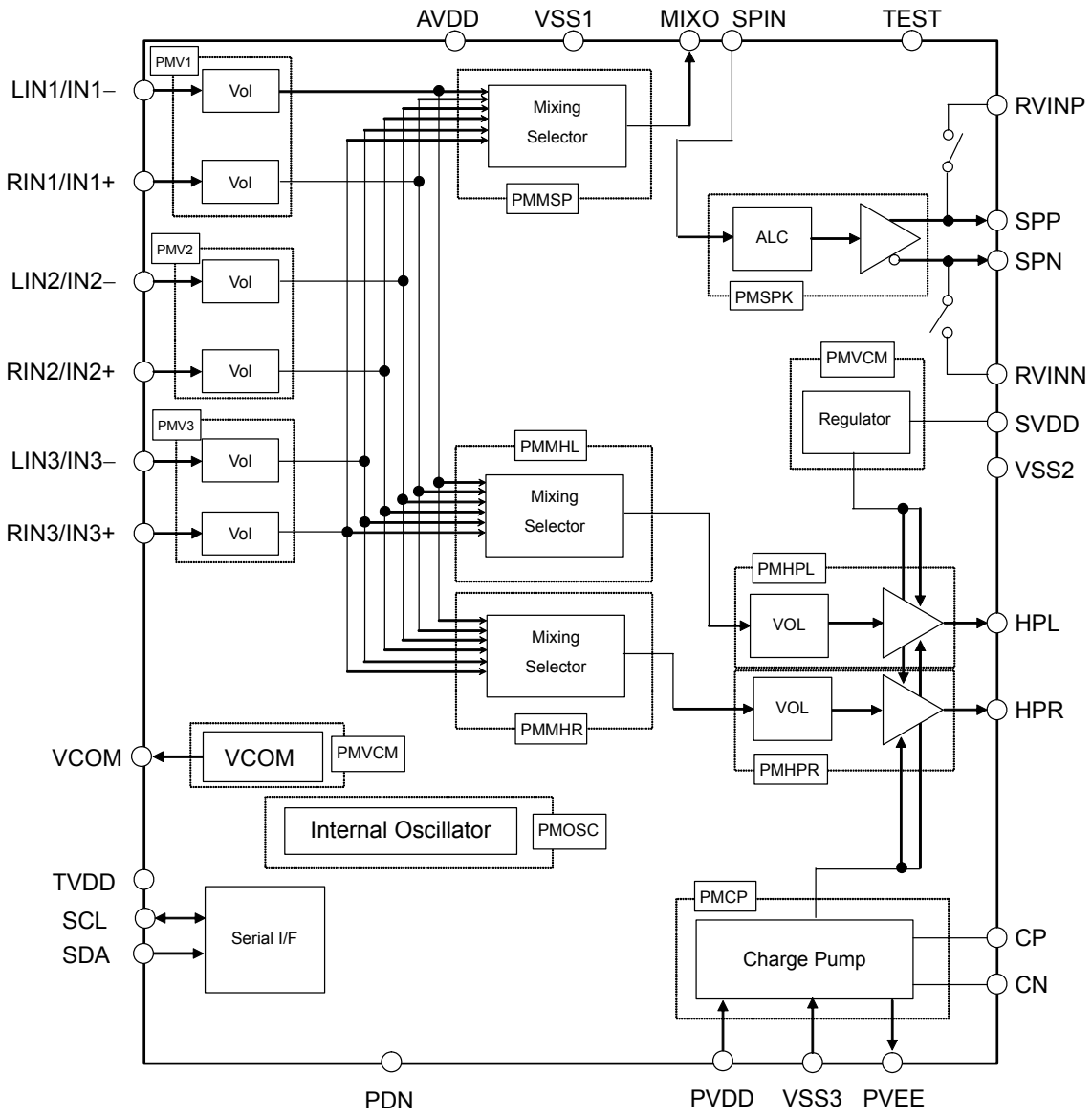
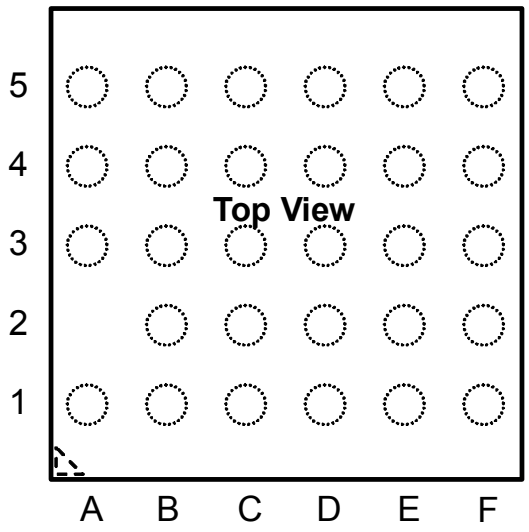


Figure 1. AK4213 Block Diagram

■ Ordering Guide

AK4213ECB	–40 ~ +85°C	29pin CSP (3.0mm x 3.0mm, 0.5mm pitch)
AKD4213	Evaluation board for AK4213	

■ Pin Layout



5	HPR	LIN3/IN3-	VCOM	RIN1/IN1+	SVDD	LIN1/IN1-
4	HPL	RIN3/IN3+	RIN2/IN2+	SPN	VSS2	SPP
3	PVEE	VSS3	PDN	LIN2/IN2-	TEST	SPIN
2		PVDD	SDA	TVDD	RVINN	RVINP
1	CP	CN	SCL	VSS1	AVDD	MIXO
	A	B	C	D	E	F

Top View

PIN / FUNCTION

No.	Pin Name	I/O	Function
E1	AVDD	-	Analog Power Supply Pin
D1	VSS1	-	Ground 1 Pin
E3	TEST	O	Test Pin This pin must be open.
D2	TVDD	-	Digital Interface Power Supply Pin
C1	SCL	I	Control Data Clock Pin
C2	SDA	I/O	Control Data Input/Output Pin
C3	PDN	I	Power-Down Mode Pin "H": Power-up, "L": Power-down, resets and initialization of the control register. The AK4213 must be reset once upon power-up.
A1	CP	I	Positive Charge Pump Capacitor Terminal Pin
B1	CN	I	Negative Charge Pump Capacitor Terminal Pin
B2	PVDD	-	Charge Pump Circuit Positive Power Supply Pin
B3	VSS3	-	Ground 3 Pin
A3	PVEE	O	Charge Pump Circuit Negative Voltage Output Pin
A4	HPL	O	Lch Headphone-Amp Output Pin
A5	HPR	O	Rch Headphone-Amp Output Pin
F2	RVINP	I	Receiver Positive Input Pin
E2	RVINN	I	Receiver Negative Input Pin
B4	RIN3/IN3+	I	Analog Input Pin
B5	LIN3/IN3-	I	Analog Input Pin
C5	VCOM	O	Analog Common Voltage Output Pin
C4	RIN2/IN2+	I	Analog Input Pin
D3	LIN2/IN2-	I	Analog Input Pin
D5	RIN1/IN1+	I	Analog Input Pin
F5	LIN1/IN1-	I	Analog Input Pin
E5	SVDD	-	Speaker-Amp Power Supply Pin
E4	VSS2	-	Speaker-Amp Ground Pin (Ground 2 Pin)
F4	SPP	O	Positive Speaker-Amp Output Pin
D4	SPN	O	Negative Speaker-Amp Output Pin
F1	MIXO	O	MIX-Amp Output Pin
F3	SPIN	I	Speaker-Amp Input Pin

Note 1. Do not allow all input pins except analog input pins (LIN1/IN1-, RIN1/IN1+, LIN2/IN2-, RIN2/IN2+, LIN3/IN3-, RIN3/IN3+, SPIN, RVINP and RVINN) to float.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	HPL, HPR, MIXO, SPIN, SPP, SPN, LIN1/IN1-, RIN1/IN1+, LIN2/IN2-, RIN2/IN2+, LIN3/IN3-, RIN3/IN3+, RVINP, RVINN, TEST	These pins must be open.

ABSOLUTE MAXIMUM RATING

(VSS1=VSS2=VSS2=0V; Note 2)

Parameter		Symbol	min	max	Units
Power Supplies: (Note 3)	Analog	AVDD	–0.3	6.0	V
	Digital I/F	TVDD	–0.3	6.0	V
	Speaker-Amp & Headphone-Amp	SVDD	–0.3	6.0	V
	Charge Pump	PVDD	–0.3	4.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Analog Input Voltage (Note 4)		VINA1	–0.3	(AVDD + 0.3) or 6.0	V
(Note 5)		VINA2	–0.3	(SVDD + 0.3) or 6.0	V
Digital Input Voltage (Note 6)		VIND	–0.3	(TVDD + 0.3) or 6.0	V
Ambient Temperature (powered applied)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 7)	Ta=85ºC (Note 8)	Pd1	-	0.65	W
	Ta=70ºC (Note 9)	Pd2	-	0.8	W

Note 2. All voltages with respect to ground.
Note 3. VSS1, VSS2, and VSS3 must be connected to the same analog plane.
Note 4. LIN1/IN1-, RIN1/IN1+, LIN2/IN2-, RIN2/IN2+, LIN3/IN3-, RIN3/IN3+ and SPIN pins
The maximum value is low value either (AVDD+0.3)V or 6.0V.
Note 5. RVINP and RVINN pins
The maximum value is low value either (SVDD+0.3)V or 6.0V.
Note 6. SDA, SCL and PDN pins.
The maximum value is low value either (TVDD+0.3)V or 6.0V.
Pull-up resistors at SCL and SDA pins should be connected to (TVDD + 0.3)V or less voltage.
Note 7. In case that PCB wiring density is 300% or more. This power is the AK4213 internal dissipation that does not include power of externally connected headphone and speaker.
Note 8. In the case of Ta=85ºC, HP-Amp and SPK-Amp must not be powered-up simultaneously. When SPK-Amp be used, HP-Amp should power-down, and the power of SPK-Amp should less than 1.3W @8Ω.
Note 9. In the case of Ta=70ºC, HP-Amp and SPK-Amp can be powered-up simultaneously. When HP-Amp and SPK-Amp be used simultaneously, the power of HP-Amp should less than 30mW @16Ω, and the power of SPK-Amp should less than 1.2W @8Ω.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1=VSS2=VSS3=0V; Note 2)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 10)	Analog	AVDD	2.7	3.3	3.6	V
	Digital I/F	TVDD	1.6	1.8	3.6	V
	Speaker-Amp & Headphone-Amp	SVDD	3.0	3.6	5.5	V
	Charge Pump	PVDD	2.7	3.3	3.6	V
	Difference	AVDD - PVDD	-0.3	0	0.3	V
		SVDD - AVDD	-0.3	-	-	V

Note 10. The power up sequence among AVDD, TVDD, SVDD, and PVDD is not critical. The PDN pin must be held to "L" when power-up. The PDN pin must be set to "H" after power supplies are powered-up. The AK4213 should be operated by the recommended power-up/down sequence shown in "System Design" to avoid pop noise at speaker output and headphone output.

The AK4213 supports the following two cases of partial power ON/OFF. In these cases, the PDN pin must be "L".

1. **TVDD=SVDD=ON: AVDD=PVDD can be power ON/OFF.**
2. **TVDD=ON: AVDD=PVDD=SVDD can be power ON/OFF.**

When the power state is changed from OFF to ON in the above cases, the PDN pin must be changed from "L" to "H" after all power supply pins are supplied. "L" time of 150ns or more is needed to reset the AK4213.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=PVDD=3.3V, SVDD=3.6V, TVDD=1.8V, VSS1=VSS2=VSS3=0V; Input Signal Frequency =1 kHz; Measurement band width=10Hz ~ 20kHz; Headphone-Amp: R_L =16Ω; Speaker-Amp: R_L =8Ω + 10μH; Charge Pump Circuit External Capacitance: C1=C2= 2.2μF (Figure 4); unless otherwise specified)

Parameter	min	typ	max	Units
LIN1, RIN1, LIN2, RIN2, LIN3, RIN3 pins				
Input Resistance	25	50	110	kΩ
Input Analog Volume: L1V3-0, R1V3-0, L2V3-0, R2V3-0, L3V3-0, R3V3-0 bits				
Step Size	1	2	3	dB
Gain Control Range	-20	-	+10	dB
MIX-Amp: MIXO pin				
Load Resistance	10	-	-	kΩ
Load Capacitance	-	-	30	pF
Headphone-Amp: LIN/RIN → HPL/HPR pins, HPGA = 0dB				
Output Power (THD+N=1%) SVDD=3.3V	- -	 64	 -	 mW
THD+N: 0.7Vrms Single-ended Input, Po = 30mW	-	-58	-40	dB
Output Noise Level (A-weighted) (Note 11)	-	24	40	μVrms
Interchannel Gain Mismatch	-	0.2	0.8	dB
Load Resistance	16	-	-	Ω
Load Capacitance	-	-	300	pF
Output Voltage: 0.7Vrms Single-ended Input	0.62	0.69	0.76	Vrms
PSRR 217Hz (Note 12) 1kHz (Note 12) 217Hz (Note 13) 1kHz (Note 13)	 - - - -	 70 70 100 80	 - - - -	 dB dB dB dB
Interchannel Isolation	60	80	-	dB
Headphone Analog Volume (HPGA4-0 bits)				
Step Size	0.5	2	3.5	dB
Gain Control Range	-50	-	+12	dB
Class-D Speaker-Amp: LIN or RIN → SPP/SPN; BTL, ALC = OFF, Input Volume=SPGA=0dB, ALC OFF				
Output Power (THD+N=10%) SVDD=5.0V SVDD=3.6V	 - -	 1.6 0.8	 - -	 W W
Output Level SVDD=5.0V, Input Level = 0.85Vrms (Note 14) SVDD=3.6V, Input Level = 0.64Vrms (Note 15) SVDD=3.6V, Input Level = 0.46Vrms (Note 16)	 - - 1.33	 2.7 2.0 1.48	 - - 1.63	 Vrms Vrms Vrms
THD+N: Po=0.25W, Input Level =0.46Vrms (Note 16)	-	-65	-40	dB
Output Noise Level (A-weighted) (Note 17)	-	85	150	μVrms
Load Resistance	8	-	-	Ω
Load Capacitance (Note 21)	-	-	300	pF
PSRR 217Hz (Note 18) 1kHz (Note 18) 217Hz (Note 19) 1kHz (Note 19)	 - - - -	 60 50 50 50	 - - - -	 dB dB dB dB
Switching Frequency	150	250	400	kHz
Current Limit at Short (Note 20)	-	40	120	mA
Start-Up Time	18	30	48	ms

Parameter			min	typ	max	Units
SPIN pins						
Input Resistance			15	26	36	kΩ
Speaker Analog Volume: SPGA5-0 bits						
Step Size			0.1	0.5	0.9	dB
Gain Control Range			-12	-	+19.5	dB
Bypass Mode: Figure 2, **Input Level = 1.13Vrms, Common Voltage = 1.8V, Measured by SPP/SPN pins**						
THD+N	1.13Vrms, 3.2Vpp		-	-50	-	dB
	0.71Vrms, 2.0Vpp		-	-60	-50	dB
Output level			-	0.46	-	Vrms
Switch ON Resistance (BYPE bit = "1")			-	2.8	-	Ω
Switch Off Isolation ; 3.6V_{DC} Input, Figure 3 (SPP/SPN pins– RVINP/RVINN pins)			-	90	-	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")						
AVDD+TVDD:	ALL ON	(Note 22)	-	4.0	6.5	mA
	HP-Amp ON	(Note 23)	-	2.0	-	mA
	SPK-Amp ON	(Note 24)	-	2.8	-	mA
PVDD (No Output):	HP-Amp ON		-	1.3	3.2	mA
SVDD (No Output):	HP-Amp ON		-	2.0	4.0	mA
	SPK-Amp ON			1.0	4.0	mA
Power-Down Mode (PDN pin = "L")		(Note 25)				
AVDD+PVDD+SVDD+TVDD			-	1	30	μA

Note 11. In case of singled-ended mode. Only mixer path of inputting signal is ON. (In case of differential mode, this value is typically 29μVrms.)
Note 12. PSR is applied to AVDD and PVDD with 100mpVpp sine wave.
Note 13. PSR is applied to SVDD with 0.89Vpp sine wave.
Note 14. In case of single-ended mode. (In case of differential mode, the input signal level is 0.425Vrms. The signals with amplitude and inverted phase should be input to positive input pin and negative input pin.)
Note 15. In case of single-ended mode. (In case of differential mode, the input signal level is 0.32Vrms. The signals with amplitude and inverted phase should be input to positive input pin and negative input pin.)
Note 16. In case of single-ended mode. (In case of differential mode, the input signal level is 0.23Vrms. The signals with amplitude and inverted phase should be input to positive input pin and negative input pin.)
Note 17. In case of singled-ended mode. Only mixer path of inputting signal is ON. (In case of differential mode, this value is typically 90μVrms.)
Note 18. PSR is applied to AVDD with 100mpVpp sine wave.
Note 19. PSR is applied to SVDD with 100mpVpp sine wave.
Note 20. Average current between SVDD and VSS2 when the SPP and SPN pins are shorted and 0.85Vrms, 1kHz sine wave is input to the AK4213 in single-ended mode.
Note 21. This is capacitance value between output pin and VSS1. When a capacitor is connected between output pins, load capacitance for each output pin doubles. Therefore, it is necessary to decide load capacitance in consideration of these.
Note 22. All Circuits are powered-up.
(PMVCM = PMOSC = PMCP = PMHPL = PMHPR = PMMHL = PMMHR = PMSPK = PMMSP = PMV1 = PMV2 = PMV3 bits= "1")
Note 23. Minimum blocks for Headphone-Amp path are powered-up.
(PMVCM = PMOSC = PMCP = PMHPL = PMHPR = PMMHL = PMMHR = PMV1 bits= "1", PMSPK = PMMSP = PMV2 = PMV3 bits= "0")
Note 24. Minimum blocks for Speaker-Amp path are powered-up
(PMVCM = PMOSC = PMCP = PMSPK = PMMSP = PMV1 bits= "1", PMHPL = PMHPR = PMMHL = PMMHR = PMV2 = PMV3 bits= "0")
Note 25. All digital input pins are held at VSS1.

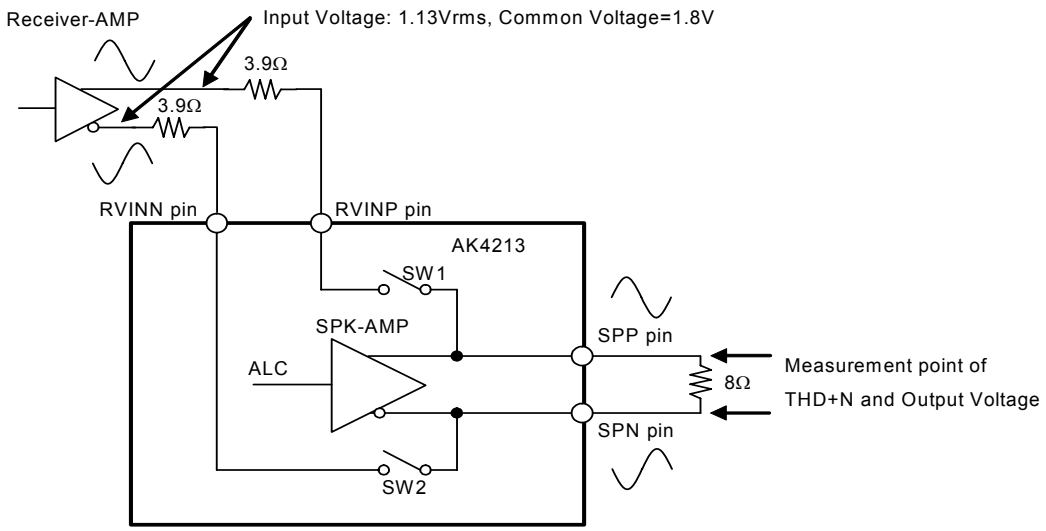


Figure 2. Connection with external RCV-Amp

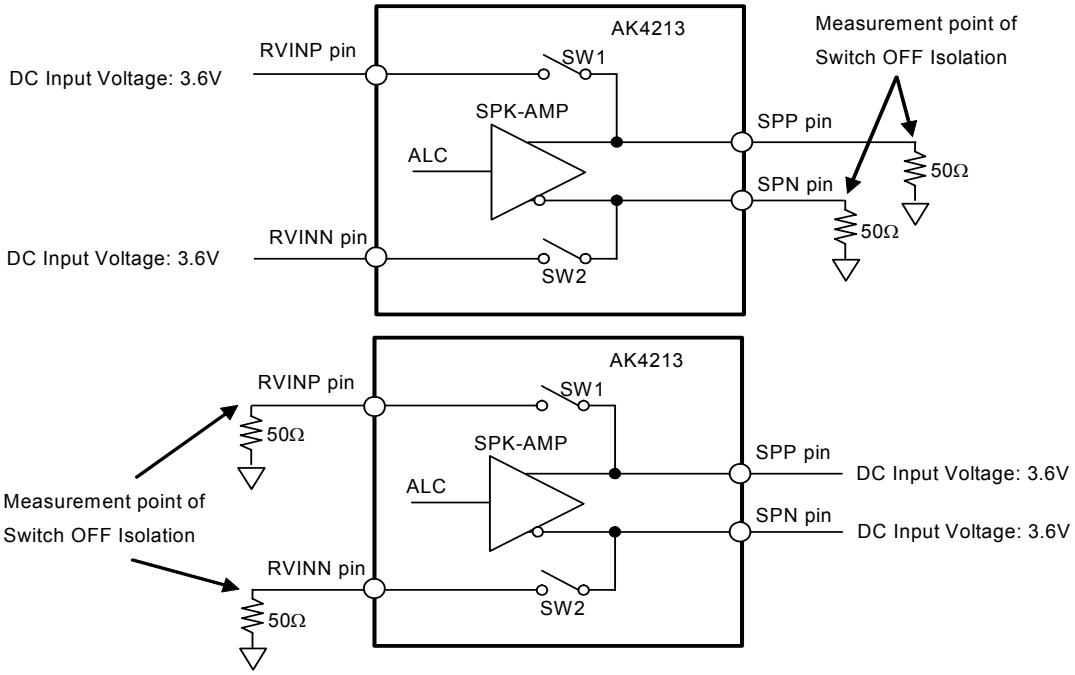


Figure 3. Measurement Circuit of Switch OFF Isolation

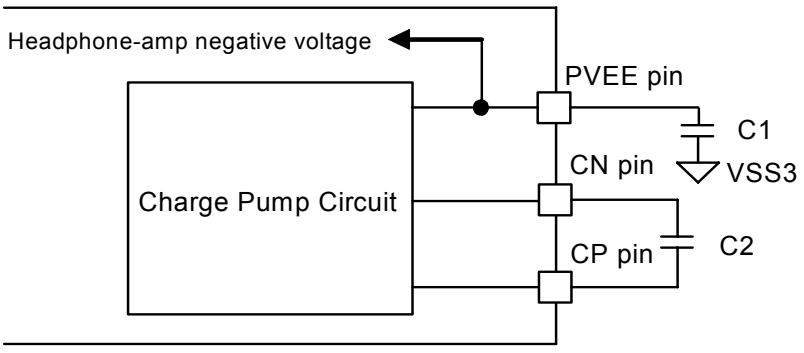


Figure 4. Charge Pump Circuit External Capacitor

DC CHARACTERISTICS

(Ta= -40~85°C; AVDD=PVDD=2.6 ~ 3.6V; SVDD=2.6 ~ 5.5V; TVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(2.2V ≤ TVDD ≤ 3.6V)	VIH	70%TVDD	-	-	V
	(1.6V ≤ TVDD < 2.2V)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	(2.2V ≤ TVDD ≤ 3.6V)	VIL	-	-	30%TVDD	V
	(1.6V ≤ TVDD < 2.2V)	VIL	-	-	20%TVDD	V
Low-Level Output Voltage						
(2.0V ≤ TVDD ≤ 3.6V: Iout = 3mA)		VOL	-	-	0.4	V
(1.6V ≤ TVDD < 2.0V: Iout = 3mA)		VOL	-	-	20%TVDD	V
Input Leakage Current		Iin	-	-	±2	μA

SWITCHING CHARACTERISTICS

(Ta= -40~85°C; AVDD=PVDD =2.6 ~ 3.6V; SVDD=2.6 ~ 5.5V; TVDD=1.6 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing: (Note 26)					
SCL Clock Frequency	FSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 27)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive load on bus	Cb	-		400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 28)	tPD	150	-	-	ns

Note 26. I^2C is a registered trademark of Philips Semiconductors.

Note 27. Data must be held long enough to bridge the 300ns-transition time of SCL.

Note 28. The PDN pin must change from “L” to “H” after all power supply pins are supplied. The AK4213 can be also reset by bringing the PDN pin = “L” to “H”.

■ Timing Diagram

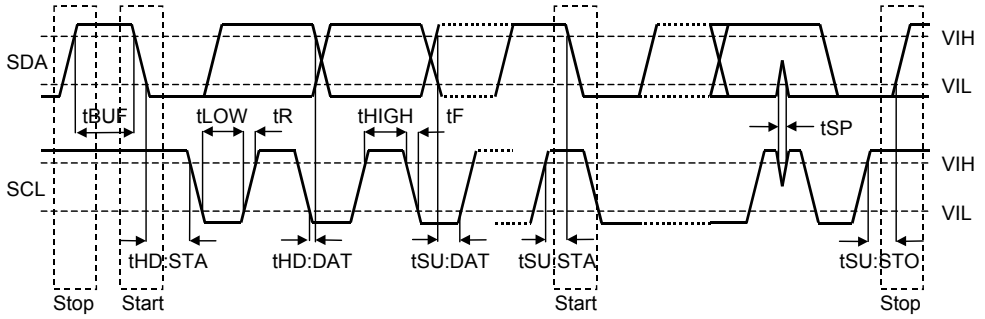


Figure 5. I^2C Bus Mode Timing

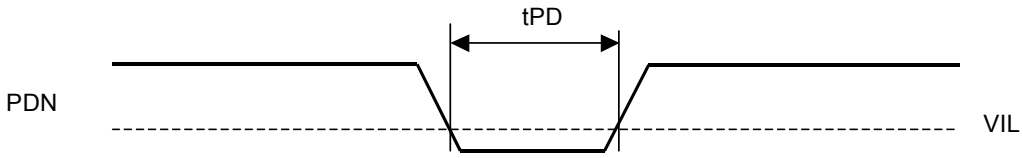


Figure 6. Power-down & Reset Timing

OPERATION OVERVIEW

■ Input Selector & Volume

The AK4213 has two input modes that are singled-ended and differential. Single-end and differential modes are selected by SD3-1 bits. In the differential mode, the input path and volume are controlled via the left channel registers, and the right channel registers are ignored. The AK4213 has three mixing circuits that used for L/R channels of headphone amplifier and speaker amplifer. The each mixing circuit can be controlled independently. When all input paths are OFF, the mixing circuit outputs common voltage. The input volume can control each input path independently. The input volume ranges from +10 dB to –20dB in 2dB step. When changing the input volume, pop noise may occur. Each input volume has power management mode which is common to the left and right channels. The power-up/down of input volume can be controlled by PMV3-1 bits. The power-up time is 16.4ms(typ.) and 26.3ms(max). AC coupling capacitor of 0.22μF or less should be connected to LINx/RINx (x=1~3) pins to reduce the pop noise at the power-up of the input volume block.

L1V3-0 bit R1V3-0 bit L2V3-0 bit R2V3-0 bit L3V3-0 bit R3V3-0 bit	GAIN (dB)	Step	
FH	+10	2dB	(default)
EH	+8		
:	:		
CH	+4		
BH	+2		
AH	0		
9H	–2		
8H	–4		
:	:		
2H	–16		
1H	–18		
0H	–20		

Table 1. Input Volume Setting

SD3 bit SD2 bit SD1 bit	Input Mode	
0	Single-ended Mode	(default)
1	Differential Mode	

Table 2. Input Mode Setting

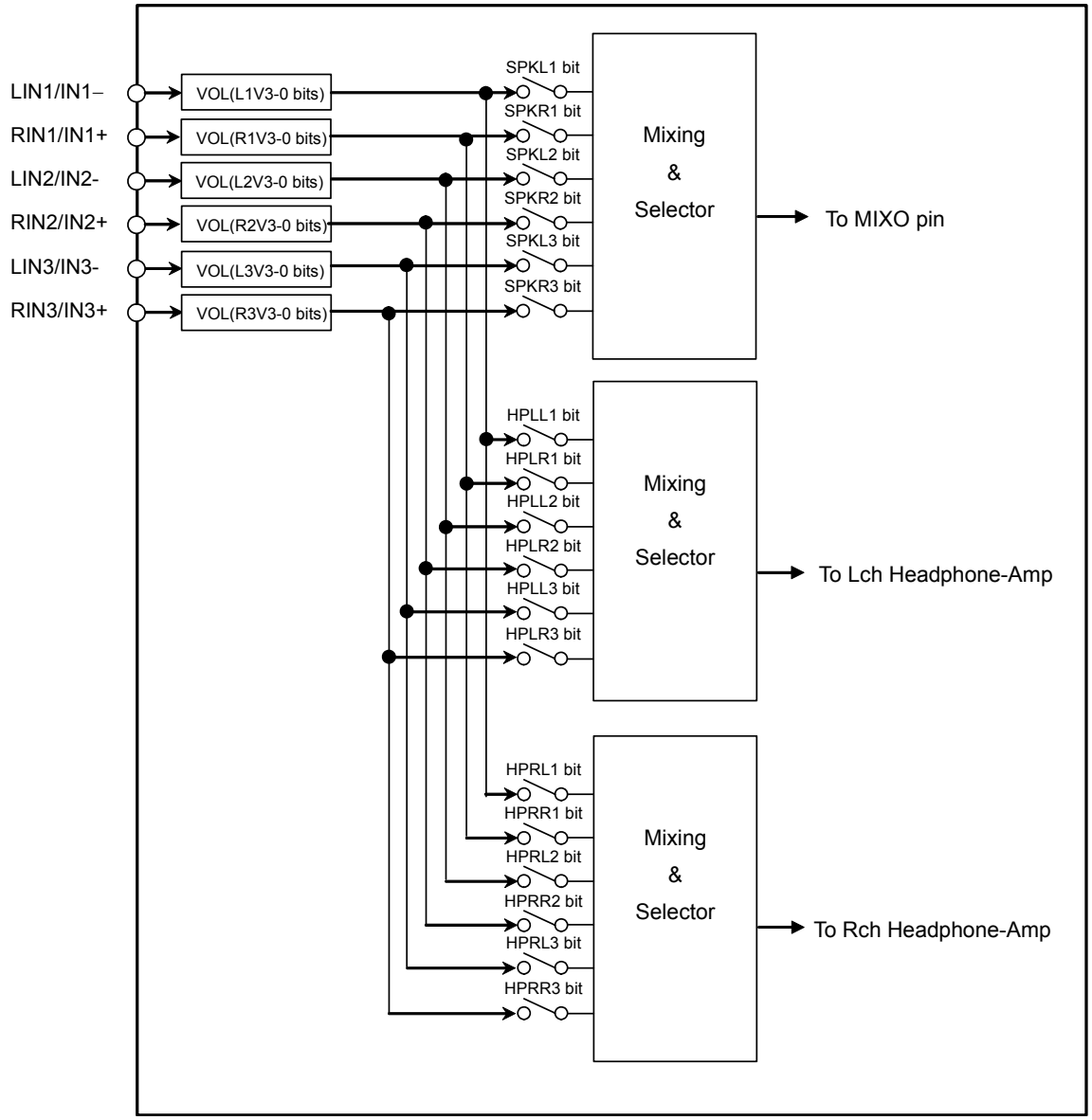


Figure 7. Input Selector & Volume in Single-ended Mode (SD3-1 bits = “000”)

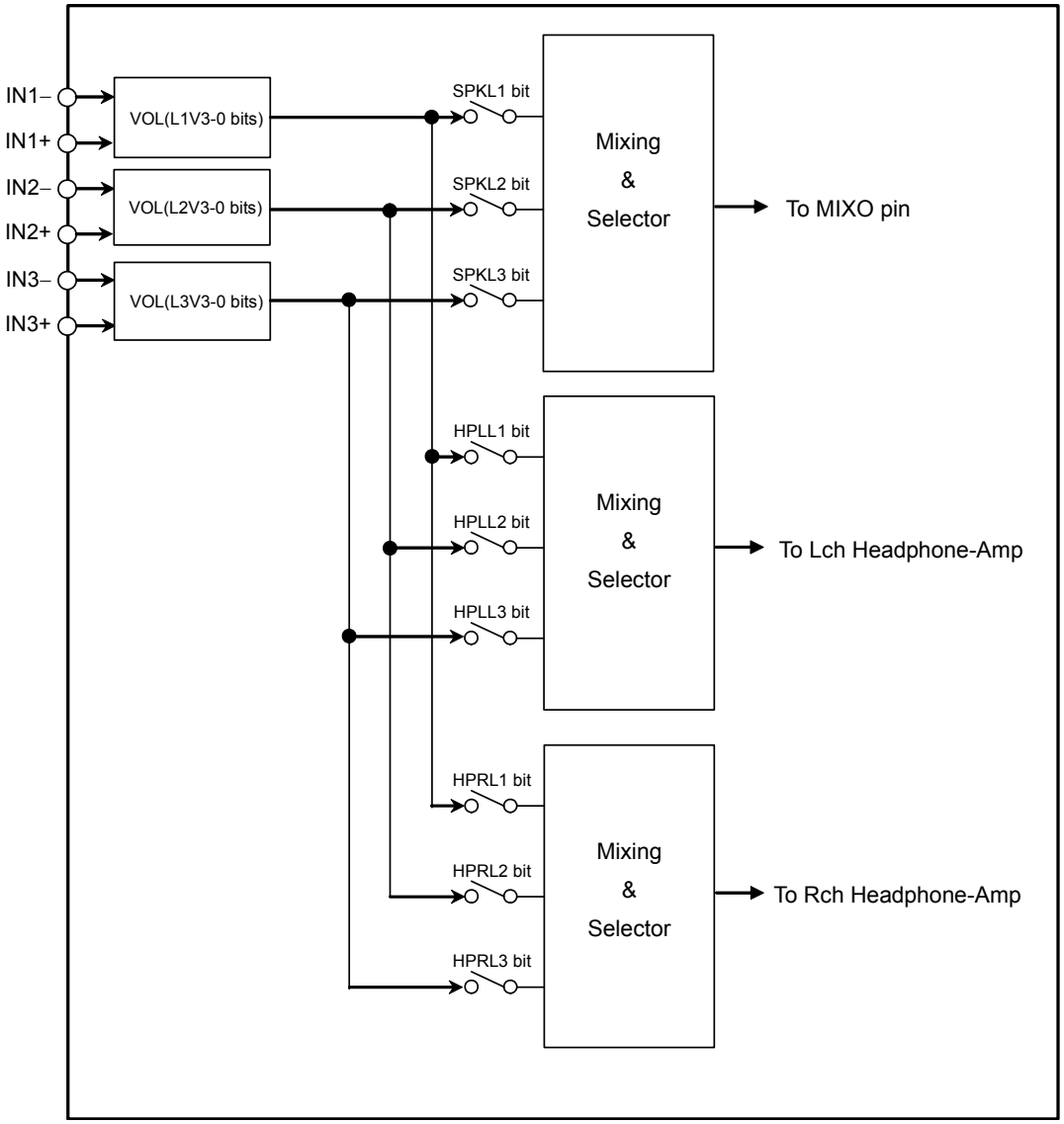


Figure 8. Input Selector and Volume in Differential Mode (SD3-1 bits = “111”)

■ Class-D Speaker-Amp

The output signal from ALC block is converted by PWM and is outputted from the SPP/SPN pins by BTL. The signal of ALC block is inputted from the SPIN pin. The BPF (Band Pass Filter) is made by inserting the capacitor and resistor between the MIXO pin and the SPIN pin. A 0.1uF capacitor must be connected between the MIXO pin and the SPIN pin in order to cancel DC offset of Mixing & Selector circuit, if the BPF is not needed.

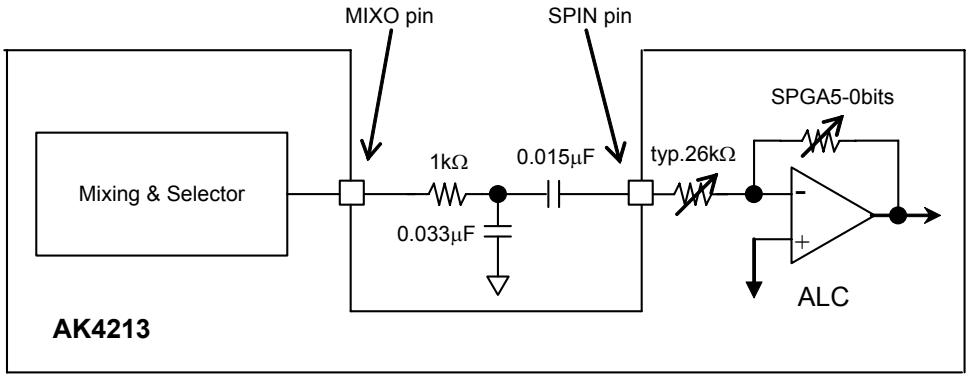


Figure 9. Example of Band-Pass-Filter for Speaker (BPF = typ. 442Hz to 4.83kHz @ -3dB)

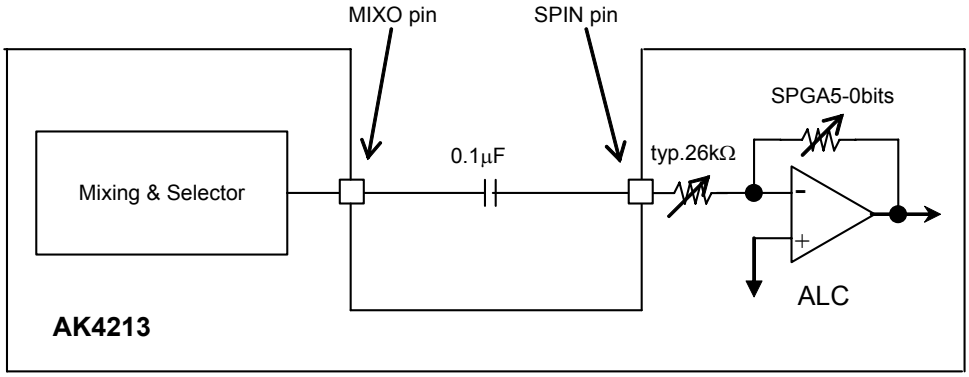


Figure 10. Example of normal connection for Speaker (fc = typ. 66Hz @ -3dB)

When the input signal level is 0.7Vrms in single-ended mode, the speaker-amp outputs 0.6W at ALC=OFF and SPGA=0dB. When the stereo signal is input to the AK4213 in single-ended mode, the input volume of left and right channels should be set to "-6dB" and left and speaker mixer path of left and right channels should be ON. In this case, the speaker outputs the signal level of "(L +R)/2".

The default internal gain is +9.82dB.When ALC is ON (ALC bit = "1"), ALC output level is automatically adjusted to −7.5dBV ~ −9.5dBV at LMTH bit = "0" and −11.5dBV ~ −13.5dBV at LMTH bit = "1". The reference level is set by REF5-0 bits. The internal gain of Class-D SPK-amp is fixed to +11.76dB

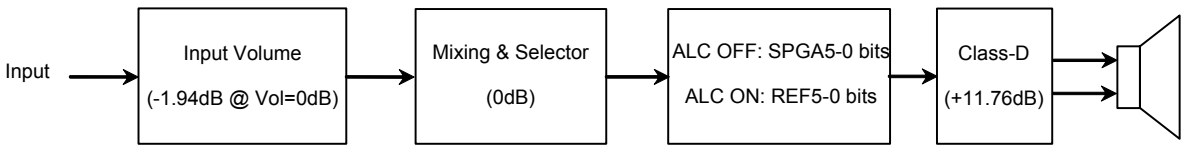


Figure 11. Speaker-Amp Path Level Diagram

When PMSPK bit is set to "0", the speaker block (ALC + Speaker-Amp) can be powered-down completely. The power-up / down transition time is 30ms (typ.) and 48ms (max).

The write operation to SPGA5-0 bits is prohibited within 1.6ms after PMSPK bit is set to "1".

PMSPK bits	Speaker-Amp	
0	Power-down	(default)
1	Power-up & Output	

Table 3. Speaker-Amp output state

■ Bypass Mode

When BYPE bit is "1" (SW1=SW2=ON), input signals to the RVINP pin and the RVINN pin are output from the SPP pin and the SPN pin respectively. Then SPK-Amp is in Hi-Z. When BYPE bit is "0" (SW1=SW2=OFF), the signal of SPK-Amp are output from the SPP/SPN pin. In case of PMSPK bit = "1", BYPE bit is ignored.
Bypass Mode can be ON when all power management register are "0" setting including VCOM and inter-oscilloscope. In case of Bypass Mode setting, PMVCM bit should be set to "1" if thermal shut-down function is used.

PMSPK bit	BYPE bit	Mode
0	0	Power-down (SPP/SPN pins are Hi-Z)
0	1	Bypass Mode
1	x	Speaker Mode

Table 4. Speaker and Receiver Modes (x: Don't care)

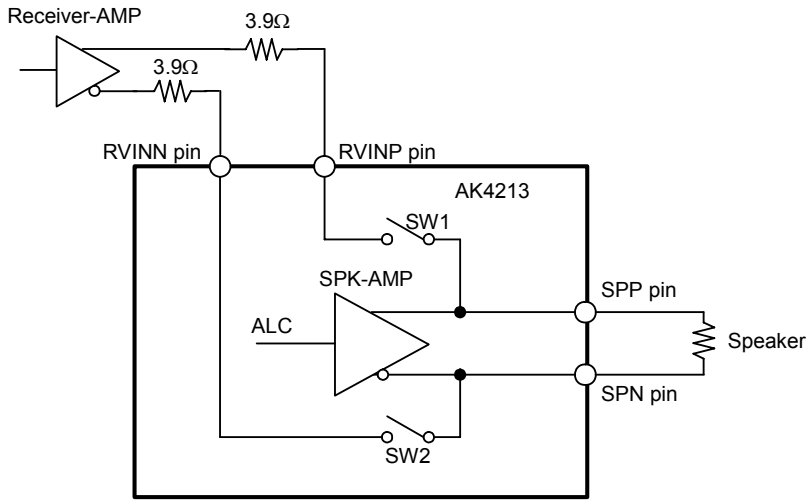


Figure 12. Bypass Mode

<Example of control sequence>

1. Speaker Mode ➔ Bypass Mode

a. Spkeaer Amp Power -down : PMSPK bit = "1" ➔ "0"(Figure 18 show the details of sequence)
b. Wait more than 500μs
c. Bypass Mode enable(SW1=SW2=ON): BYPE bit = "0" ➔ "1"

2. Bypass Mode ➔ Speaker Mode

a. Bypass Mode ignore (SW1=SW2=OFF): BYPE bit = "1" ➔ "0"
b. Speaker-Amp power-up: Figure 18 shows the details of sequence.

■ ALC Operation

The ALC (Automatic Level Control) operation of speaker-amp output is operated by ALC block when ALC bit = "1". When ALC bit is "0", the speaker volume depends on the setting value of SPGA5-0 bits.

(1) ALC Limiter Operation

During the ALC limiter operation, when ALC output level exceeds the ALC limiter detection level (LMTH bit), the SPGA value is attenuated automatically to the amount defined by ALC limiter ATT step (LMTH1-0 bits).

When ZELMN bit is set to "0" (zero crossing detection is enabled), the SPGA value is changed by the ALC limiter operation at the zero crossing point or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout periods of both the ALC limiter and recovery operation.

When ZELMN bit = "1" (zero crossing detection is disabled), SPGA value is immediately (period: typ. 125μs, max. 200μs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuate operation is executed continuously until the ALC output level becomes ALC limiter detection level or less. After completing the attenuate operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH bit.

LMTH bit	ALC Limiter Detection Level	ALC Recovery Waiting Counter Reset Level	
0	ALC Output ≥ -7.5dBV	–7.5dBV > ALC Output ≥ –9.5dBV	(default)
1	ALC Output ≥ -11.5dBV	–11.5dBV > ALC Output ≥ –13.5dBV	

Note: ALC limiter detection level and ALC recovery waiting counter reset level do not depend on operation voltage.

Table 5. ALC Limiter Detection Level / Recovery Counter Reset Level

ZELMN bit	LMAT1	LMAT0	ALC Limiter ATT Step		
0	0	0	1 step	0.5dB	(default)
	0	1	2 step	1.0dB	
	1	0	4 step	2.0dB	
	1	1	8 step	4.0dB	
1	x	x	1step	0.5dB	

Table 6. ALC Limiter ATT Step (x: Don't care)

ZTM1 bit	ZTM0 bit	Zero Crossing Timeout		
		typ.	max	
0	0	16.4ms	26.3ms	
0	1	32.8ms	51.5ms	(default)
1	0	65.6ms	105.0ms	
1	1	131.2ms	210.0ms	

Table 7. ALC Zero Crossing Timeout Period

(2) ALC Recovery Operation

The ALC recovery operation waits for the WTM2-0 bits to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" during wait time, the ALC recovery operation is executed. The SPGA value is automatically incremented by RGAIN1-0 bits up to the set reference level (REF5-0 bits) with zero crossing detection which timeout period is set by ZTM1-0 bits. The ALC recovery operation period is set by WTM2-0 bits. When zero cross is detected during the wait period set by WTM2-0 bits, the ALC recovery operation waits until WTM2-0 period and the next recovery operation is executed. The setting period of WTM2-0 bits should be same as ZTM1-0 bits or longer period.

When RGAIN 1-0 bits are set to "10", the ALC recovery operation is not executed even the ALC limiter operation is executed.

During the ALC recovery operation, when the ALC output level exceeds ALC limiter detection level (LMTH bit), the ALC limiter operation is executed immediately. When

"ALC recovery waiting counter reset level ≤ ALC Output Signal < ALC limiter detection level (LMTH1-0)"

during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When

"ALC recovery waiting counter reset level > ALC Output Signal",

the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small singal level in the large noise can be improved by this fast recovery operation.

WTM2 bit	WTM1 bit	WTM0 bit	Recovery Waiting Timer		
			typ.	max	
0	0	0	16.4ms	26.3ms	
0	0	1	32.8ms	51.5ms	
0	1	0	65.6ms	105.0ms	
0	1	1	131.2ms	210.0ms	
1	0	0	262.4ms	419.9ms	
1	0	1	524.8ms	839.7ms	(default)
1	1	0	1049.6ms	1679.4ms	
1	1	1	2099.2ms	3358.8ms	

Table 8. ALC Recovery Waiting Timer Period

RGAIN1	RGAIN0	GAIN STEP		
0	0	1 step	0.5dB	(default)
0	1	2 step	1.0dB	
1	0	0 step	0dB	(Only limiter operation)
1	1	Reserved		

Table 9. ALC Recovery GAIN Step

REF5-0	GAIN (dB)	Step	
3FH	+19.5	0.5dB	
3EH	+19.0		
3DH	+18.5		
3CH	+18.0		(default)
:	:		
19H	+0.5		
18H	0.0		
17H	–0.5		
:	:		
02H	–11.0		
01H	–11.5		
00H	–12.0		

Table 10. Reference Level at ALC Recovery Operation

(3) Example of ALC Operation

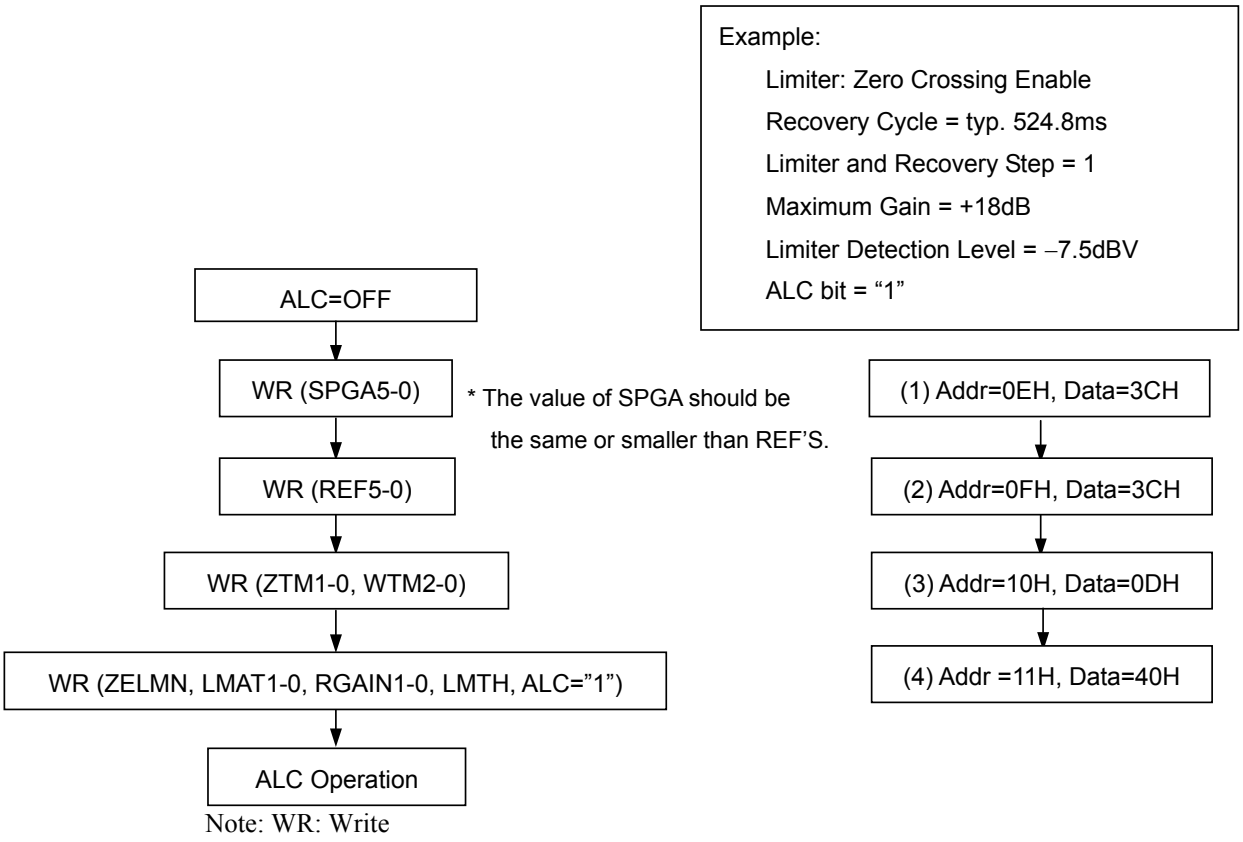
Table 11 shows the example of the ALC setting. The ALC starts from the value of SPGA5-0 bits.

Register Name	Comment	Data	Parameter
LMTH	Limiter detection Level	0	–7.5dBV
ZELMN	Limiter Zero crossing Enable	0	Limiter Zero Crossing Enable
WTM2-0	Recovery waiting period	101	typ. 524.8ms
REF5-0	Maximum gain at recovery operation	3CH	+18dB
LMAT1-0	Limiter ATT Step	00	0.5dB
RGAIN1-0	Recovery GAIN Step	00	0.5dB
ZTM1-0	Zero-crossing Timeout	01	typ. 32.8ms
ALC	ALC Enable bit	1	Enable

Table 11. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0".

- LMTH, LMAT1-0, WTM2-0, RGAIN1-0, REF5-0, ZTM1-0 and ZELMN bits



Note: WR: Write

Figure 13. Registers set-up sequence at ALC operation

■ Speaker Volume (SPGA: Manual Mode)

The speaker volume becomes manual mode when ALC bit is "0". This mode is used in the case shown below.

1. Set-up the registers for the ALC operation (ZTM1-0, LMTH and etc).
2. Set-up the initial value of SPGA when ALC starts.
3. When SPGA is used as a manual volume.

SPGA5-0 bits set the gain of the volume control. The SPGA value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits. When PMSPK bit is "0", SPGA5-0 bits does not write to anything. After PMSPK bit is changed from "0" to "1", writing to SPGA5-0 bits is inhibit within 1.6ms.

When changing from PMSPK bit = "0" to PMSPK bit = "1", SPGA volume becomes default value (0dB) regardless of the setting of SPGA5-0 bits.

SPGA5-0 bits	GAIN (dB)	Step	
3FH	+19.5	0.5dB	
3EH	+19.0		
3DH	+18.5		
3CH	+18.0		
:	:		
19H	+0.5		
18H	0.0		(default)
17H	–0.5		
:	:		
02H	–11.0		
01H	–11.5		
00H	–12.0		

Table 12. Speaker-Amp Volume Setting

When writing to the SPGA5-0 bits continuously, the control register should be written with an interval more than zero crossing timeout.

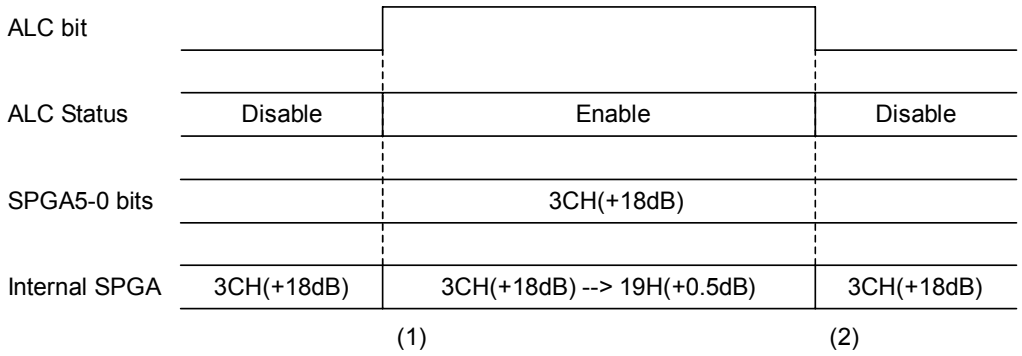


Figure 14. SPGA value during ALC operation

(1) ALC operation starts from the SPGA value when ALC bit is changed to "1".
(2) Writing to SPGA registers is ignored during ALC operation. After ALC is disabled, the SPGA changes to the last written data by twice period of zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" in an interval more than zero crossing timeout period after ALC bit = "0".

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage(PVEE) from PVDD voltage for headphone amplifiers. When PMCP bit is set to "1", the charge pump circuit is powered-up. Then PMOSC and PMVCM must be set to "1".

The power up time of charge pump circuit is typically 6.2ms and maximum 10ms.When PMHPL bit = "1" or PMHPR bit = "1", the Headphone-Amp is powered-up after the charge pump circuit is powered-up (Figure 17).

■ Headphone-Amp (HPL/HPR pins)

Power supply voltage for headphone amplifiers is applied from a regulator for positive power and charge-pump for negative power. Regulator is driven by SVDD and charge-pump is driven by PVDD. The PVEE pin outputs the negative voltage generated by the internal charge pump circuit. The headphone amplifier output is single-ended and centered on 0V (VSS3). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16 Ω. When the input signal level is 0.7Vrms at single-ended mode, the output voltage is 0.69Vrms (= 30mW @ 16Ω) at HPG43-0 bits = "19H" (0dB). The output level of headphone-amp can be controlled by HPGA4-0 bits. This volume setting is common to L/R channels and can attenuate / gain the mixer output from +12dB to –50dB in 2dB step.

HPGA4-0 bits	GAIN (dB)	Step	
1FH	+12	2dB	
1EH	+10		
:	-		
1AH	+2		
19H	0		(default)
18H	–2		
17H	–4		
16H	–6		
:	:		
2H	–46		
1H	–48		
0H	–50		

Table 13. Headphone-Amp Volume Setting

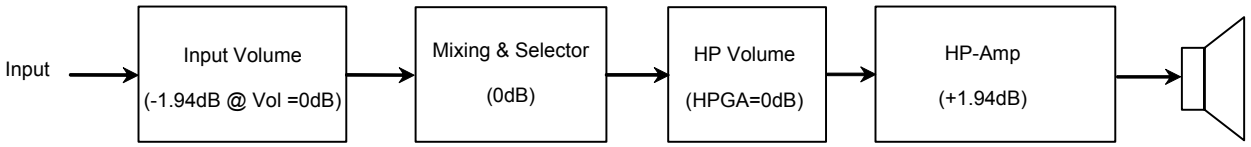


Figure 15. Headphone-Amp Path Level Diagram

The headphone output is enabled when HPMTN bit is "1" and muted when HPMTN bit is "0". The mute ON/OFF time is set by PTS1-0 bits when MOFF bit is "0". When MOFF bit is "1", the mute ON/OFF is switched immediately.

When PMHPL and PMHPR bits are "0", the headphone-amps are powered-down completely. At that time, the HPL and HPR pins go to VSS3 voltage via the internal pulled-down resistor. The pulled-down resistor is 20Ω(typ) at HPZ bit = "0", 25kΩ(typ) at HPZ bit = "1". The power-up time is 16.4ms (typ.) and 26.3ms (max.), and power up/down is executed immediately.

PMCP/PMVCM	PMHPL/R	HPMTN	HPZ	Mode	HPL/R pins	
x	0	x	0	Power-down & Mute	Pulled-down by 20Ω (typ)	(default)
x	0	x	1	Power-down	Pulled-down by 25kΩ(typ)	
1	1	0	0	Mute	VSS3	
1	1	1	0	Normal Operation	Normal Operation	

Table 14. Headphone amplifier Mode Setting (x: Don't care)

<Wired OR with External Headphone-Amp>

When PMVCM=PMCP=PMOSC=HPZ bits are "1"(charge pump circuit is powered-up), the AK4213 HP-Amp can be connected to external single supply HP-Amp by "wired OR". The external HP-Amp can output the single up to ±PVDD [Vpp] after the charge pump circuit is powered-up.

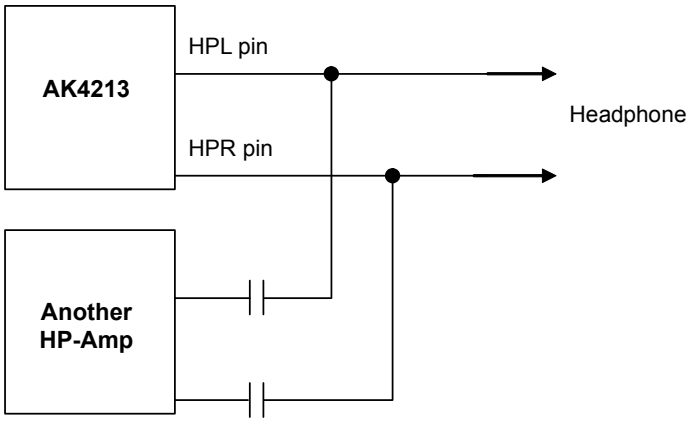


Figure 16. Wired OR with External HP-Amp

■ Transition Time

The mute ON/OFF time of headphone-amp is set to PTS1-0 bits. These operations are soft transition.

The Enable/Disable for the soft transition is set by MOFF bit. The soft transition is disabled while MOFF bit is "1", the mute ON/OFF is switched immediately.

As shown in Table 15, if the soft transition is enabled, the register value of the same address must be changed in an interval more than transition time. The write operation is ignored if the same values are written as the previous write operation.

	Address	Register Name	Enable / Disable
PTS1-0 bits	0DH	HPMTN bit	MOFF bit

Table 15. Registers with Transition Time

PTS1	PTS0	MUTE ON/OFF Time		
		typ.	max.	
0	0	16.4ms	26.3ms	(default)
0	1	32.8ms	51.5ms	
1	0	65.6ms	105.0ms	
1	1	131.2ms	210.0ms	

Table 16. Headphone-Amp Mute ON/OFF Transition Time

■ Thermal Shutdown Function

When the internal device temperature rises up irregularly (E.g. Output pins of speaker amplifier are shortened.), the charge pump, headphone amplifier, and speaker amplifier are automatically powered-down and then THDET bit becomes "1". The powered-down charge pump circuit, headphone amplifier and speaker amplifier do not return to normal operation unless HP/SPK-Amp blocks of the AK4213 are reset by the PDN pin "L". The device status can be monitored by THDET bit.

<Recommend sequence>

1. VCOM Power-Up; PMVCM bit = "0" → "1"
2. Wait more than 1ms
3. Bypass Mode Enable: BYPE bit = "0" → "1"
4. Bypass Mode Disable: BYPE bit = "1" → "0"
5. VCOM Power-down; PMVCM bit = "1" → "0"

■ System Reset

The PDN pin must keep "L" until all power supply pins (AVDD, PVDD, SVDD and TVDD) are supplied. After they are applied, the PDN pin must be set to "H". After exiting reset (PDN pin: "L" → "H"), all blocks (Input Volume, VCOM, Oscillator, Mixer, Headphone-Amp, Speaker-Amp and charge pump circuit) switch to the power-down state. The contents of the control register are maintained until reset is executed.

■ Power-Up/Down Sequence

1) HP-Amp

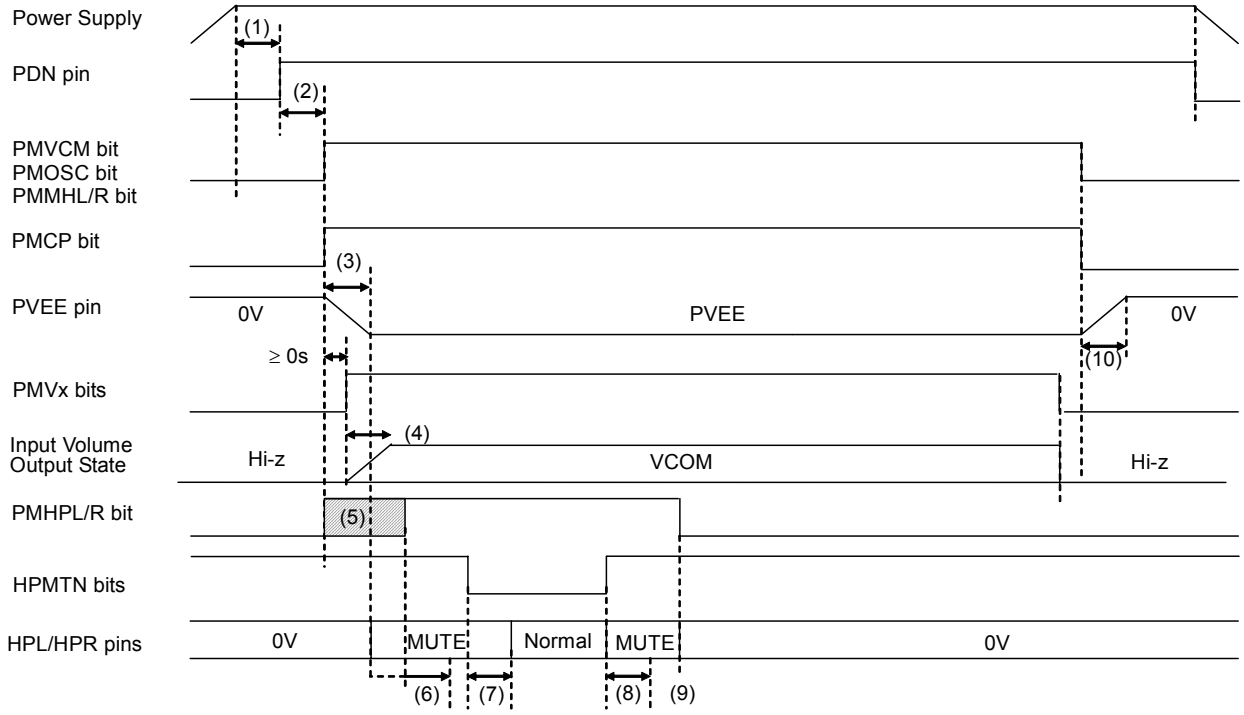


Figure 17. HP-Amp Power-up/down sequence example

(1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4213.
The power must be ON in the state of the PDN pin = "L". The PDN pin must be set to "H" after power supply (AVDD, TVDD, PVDD, SVDD) ON.

(2) PTS1-0, MOFF, HPGA4-0, and SD3-1 bits must be set during this period.

(3) Regulator, Power-up of Charge Pump, internal oscillator, VCOM, and HP-Amp Mixer & Selector: PMCP = PMMHL = PMMHR = PMOSC = PMVCM bits = "0" → "1"
The PVEE pin becomes PVEE voltage within 10ms (max.).

(4) Power-up of input volume: PMVx bit = "0" → "1"
Input Volume setting (L1V3-0, L2V3-0, L3V3-0, R1V3-0, R2V3-0, R3V3-0 bits)
Input path setting (HPLL3-1, HPLR3-1, HPRR3-1, HPRL3-1 bits)
Input volume block is powered-up within 26.3ms (max.). Input path and volume can be set when input volume block is powered-up.

(5) If PMCP and PMHPL/R bits are set to "1" at the same time or PMHPL/R bits are set to "1" during the power-up time of the Charge Pump circuit, Headphone-Amp is powered-up after the Charge Pump circuit is powered-up.

(6) Power-up of Headphone-Amp: PMHPL/R bits = "0" → "1"
Headphone-Amp is in the mute state and becomes ground level. Headphone-Amp power-up time is 26.3ms (max.).

(7) Headphone-Amp mute release: HPMTN bit = "0" → "1"
Headphone-Amp goes to the normal operation after the transition time. Headphone-Amp mute release time depends on the setting of PTS1-0 and MOFF bits.

(8) Headphone-Amp mute: HPMTN bit = "1" → "0"
Headphone-Amp goes to the mute state after the transition time set by PTS1-0 and MOFF bits.

(9) Headphone-Amp power-down: PMHPL/R bits = "1" → "0"
Headphone-Amp is powered-down immediately.

(10) Power-down of Charge Pump, internal oscillator, VCOM, and HP-Amp Mixer & Selector: PMCP = PMMHL = PMMHR = PMOSC = PMVCM bits = "1" → "0"
The PVEE pin becomes 0V according to the time constant of the capacitor at the PVEE pin and the internal resistor. The internal resistor is 17.5kΩ (typ.). Charge Pump Circuit can be powered-up during this period.

2) SPK-Amp

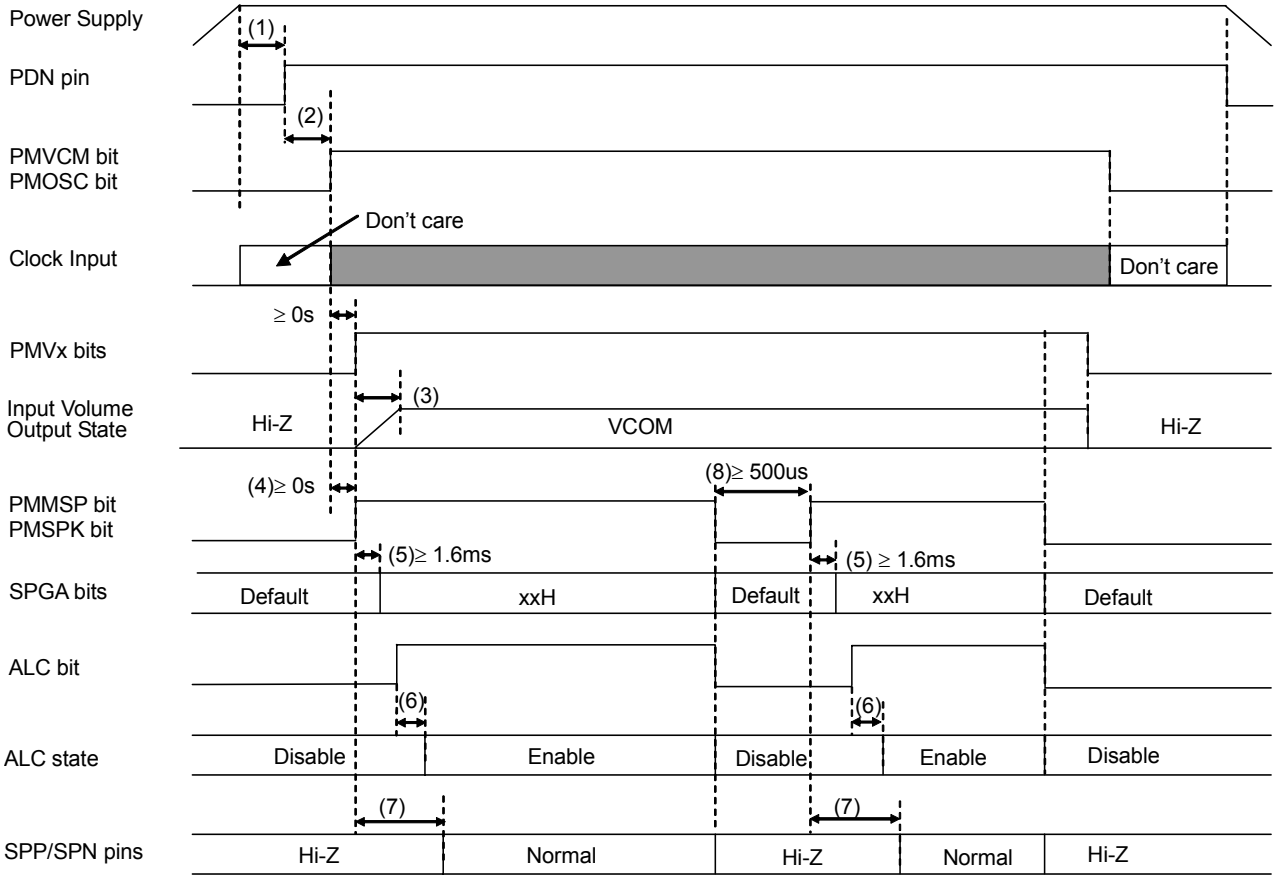


Figure 18. SPK-Amp Power-up/down Sequence Example

(1) After Power Up, PDN pin = "L" → "H". "L" time of 150ns or more is needed to reset the AK4213.
The power must be ON in the state of PDN pin = "L". The PDN pin must be set to "H" after power supply (AVDD, TVDD, PVDD, SVDD) are ON.

(2) Power-up of VCOM and the internal oscillator: PMVCM= PMOSC: "0" → "1"
SD3-1 bits must be set during this period.

(3) Power-up of input volume: PMVx bit = "0" → "1"
Input volume setting (L1V3-0, L2V3-0, L3V3-0, R1V3-0, R2V3-0, R3V3-0 bits)
Input path setting (SPKL3-1, SPKR3-1 bits)
Input volume block is powered-up within 26.3ms (max.). Input path and volume can be set when input volume block is powered-up.

(4) Power-up of SPK-Amp and SPK-Amp Mixer & Selector: PMMSP = PMSPK bits ="0"→ "1"

(5) SPGA5-0 bits setting: The setting of SPKG5-0 and ALC bits is enabled at 1.6ms or more after PMSPK bit is set to "1".

(6) ALC setting: ALC is enabled at 30ms (max.). Refer to "Registers set-up sequence at ALC operation".

(7) Speaker-Amp goes to the normal operation at 48ms (max.) after PMSPK bit is changed to "1".

(8) Once Speaker-Amp is powered-down, Speaker-Amp can be powered-up again at 500μs or more lately. When PMMSP, PMSPK bit = "1" → "0", before PMVCM,PMOSC bit = "1" → "0", please wait more than 0.5ms.

3) Change of the signal path to HP-Amp or SPK-Amp

Example: The signal path changes from LIN1/RIN1 to LIN2/RIN2 when HP-Amp is powered-up.

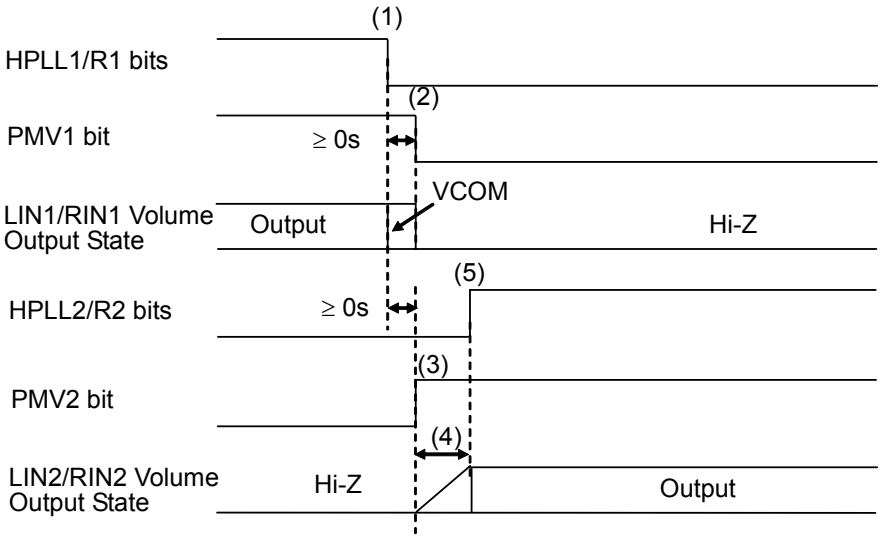


Figure 19. Example of changing signal path during HP-Amp is powered-up

(1) Signal path OFF from LIN1/RIN1 to HP-Amp: HPLL1 = HPLR1 bits = "1" → "0"
(2) Input volume of LIN1/RIN1 is powered-down: PMV1 bit = "1" → "0"
(3) Input volume of LIN2/RIN2 is powered-up: PMV2 bit = "0" → "1"
(4) Input volume of LIN2/RIN2 is powered-up at 26.3ms (max.).
(5) Signal path ON from LIN2/RIN2 to HP-Amp: HPLL2 = HPLR2 bits = "0" → "1"

■ Serial Control Interface

The AK4213 supports a fast-mode I^{2}C-bus system (max: 400kHz). Pull-up resistors at the SCL and SDA pins should be connected to (TVDD + 0.3)V or less voltage.

1. WRITE Operations

Figure 20 shows the data transfer sequence for the I^{2}C-bus mode. All commands are preceded by START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates START condition (Figure 26). After the START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as "0010011"(Figure 21). If the slave address matches that of the AK4213, the AK4213 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 27). An R/W bit value of "1" indicates that the read operation is to be executed. "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4213. The format is MSB first, and those most significant 3-bit are fixed to zero (Figure 22). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 23). The AK4213 generates an acknowledge after each byte is received. A data transfer is always terminated by STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 26).

The AK4213 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4213 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 12H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 28) except for the START and STOP conditions.

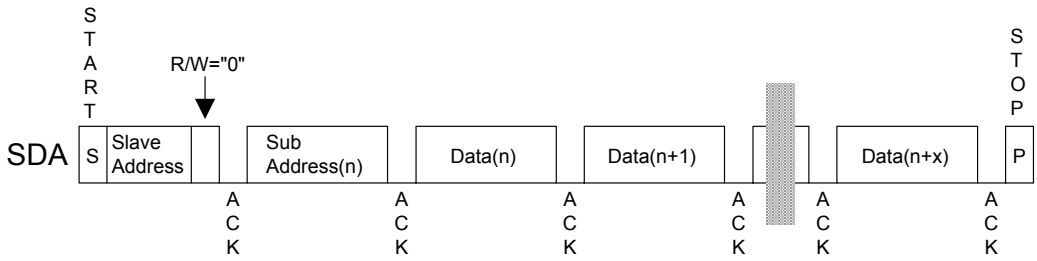


Figure 20. Data Transfer Sequence

0	0	1	0	0	1	1	R/W

Figure 21. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 22. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 23. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4213. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented, and the next data is automatically taken into the next address. If the address exceeds 12H prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4213 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4213 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address "n", the next CURRENT READ operation would access data from the address "n+1". After receipt of the slave address with R/W bit "1", the AK4213 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge but generates stop condition, the AK4213 ceases transmission.

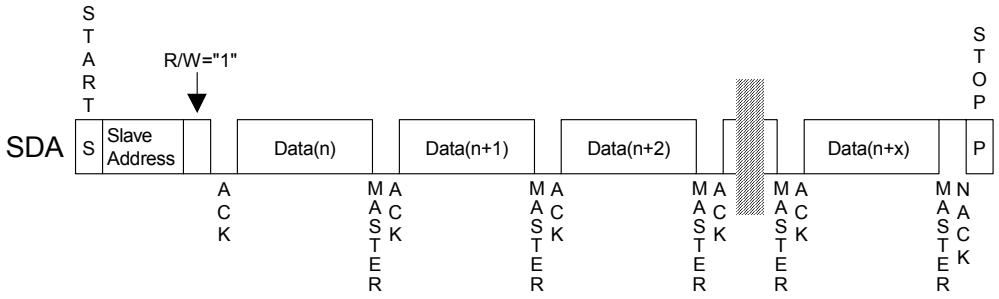


Figure 24. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit "1", the master must first perform a "dummy" write operation. The master issues start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit "1". The AK4213 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but generates a stop condition, the AK4213 ceases transmission.

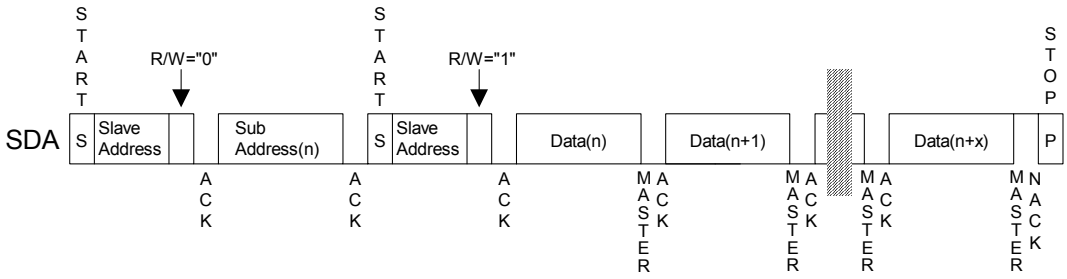


Figure 25. RANDOM ADDRESS READ

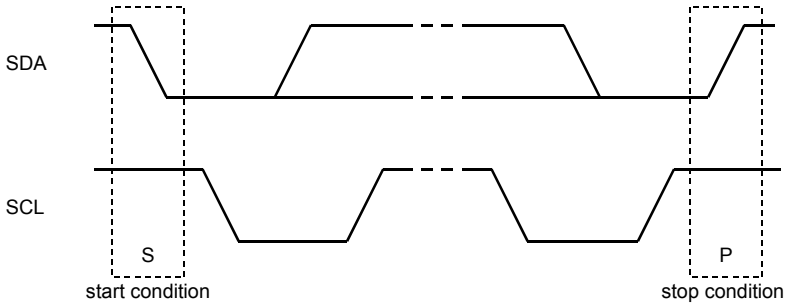


Figure 26. START and STOP Conditions

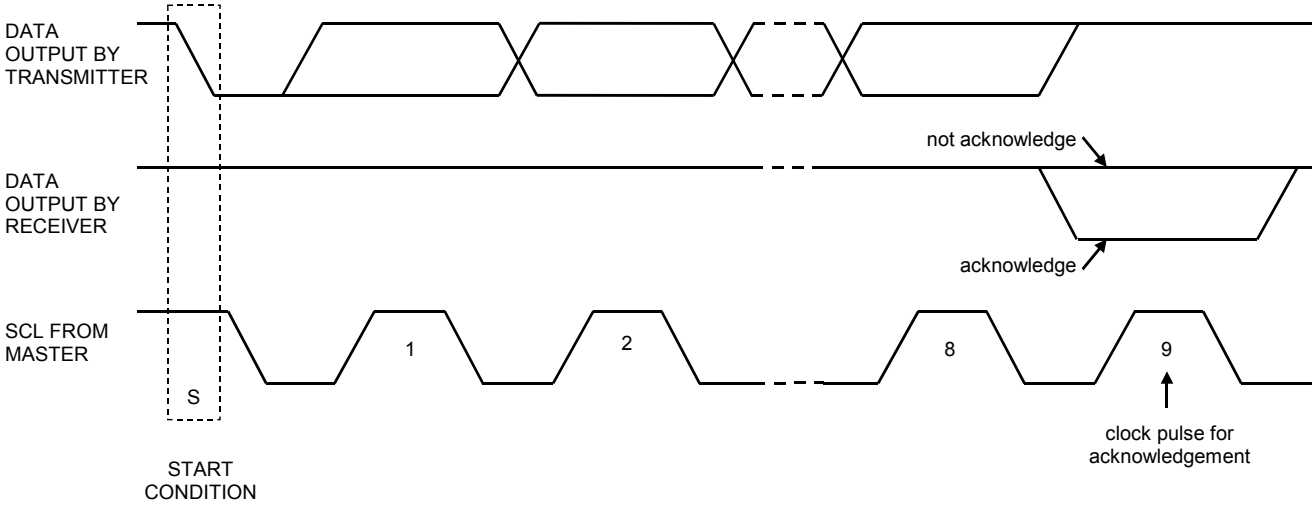


Figure 27. Acknowledge on the I^2C-Bus

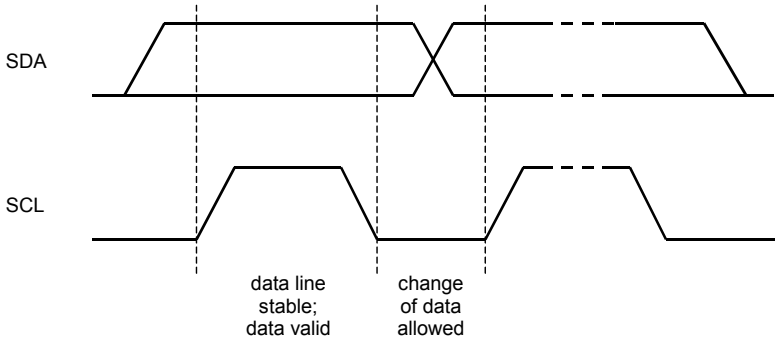


Figure 28. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMMHR	PMMHL	PMHPR	PMHPL	PMCP	PMOSC	PMVCM
01H	Power Management 1	0	0	0	0	0	PMMSP	0	PMSPK
02H	Power Management 2	0	0	0	0	0	PMV3	PMV2	PMV1
03H	Mode Control 0	THDET	0	0	BYPE	0	SD3	SD2	SD1
04H	Lch Headphone Mixer	0	0	HPLR3	HPLL3	HPLR2	HPLL2	HPLR1	HPLL1
05H	Rch Headphone Mixer	0	0	HPRR3	HPRL3	HPRR2	HPRL2	HPRR1	HPRL1
06H	Speaker Mixer	0	0	SPKR3	SPKL3	SPKR2	SPKL2	SPKR1	SPKL1
07H	Reserved	0	0	0	0	0	0	0	0
08H	Input Volume #1	R1V3	R1V2	R1V1	R1V0	L1V3	L1V2	L1V1	L1V0
09H	Input Volume #2	R2V3	R2V2	R2V1	R2V0	L2V3	L2V2	L2V1	L2V0
0AH	Input Volume #3	R3V3	R3V2	R3V1	R3V0	L3V3	L3V2	L3V1	L3V0
0BH	Reserved	0	0	0	0	0	0	0	0
0CH	Mode Control 1	0	0	MOFF	0	PTS1	PTS0	0	0
0DH	Headphone PGA Control	0	HPZ	HPMTN	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
0EH	Speaker PGA Control	0	0	SPGA5	SPGA4	SPGA3	SPGA2	SPGA1	SPGA0
0FH	ALC Mode Control 1	0	0	REF5	REF4	REF3	REF2	REF1	REF0
10H	ALC Mode Control 2	0	0	0	ZTM1	ZTM0	WTM2	WMT1	WMT0
11H	ALC Mode Control 3	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH
12H	TEST	0	0	0	0	0	0	0	0

All registers writing are inhibited at PDN pin = "L".
The PDN pin = "L" resets the registers to their default value.

Note 29. The bit indicated as "0" in the register map must contain a "0" value.
Note 30. Only write to address 00H to 12H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management 0	0	PMMHR	PMMHL	PMHPR	PMHPL	PMCP	PMOSC	PMVCM
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM and Regulator which used for Headphone-Amp
0: Power OFF (default)
1: Power ON

PMOSC: Power Management for Internal Oscillator
0: Power OFF (default)
1: Power ON

PMCP: Power Management for Charge Pump Circuit
0: Power OFF (default)
1: Power ON

PMHPL: Power Management for Lch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMHPR: Power Management for Rch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMMHL: Power Management for Mixing & Selector Circuit of Lch Headphone-Amp
0: Power OFF (default)
1: Power ON

PMMHR: Power Management for Mixing & Selector Circuit of Rch Headphone-Amp
0: Power OFF (default)
1: Power ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Power Management 1	0	0	0	0	0	PMMSP	0	PMSPK
R/W		RD	RD	RD	RD	RD	R/W	RD	R/W
Default		0	0	0	0	0	0	0	0

PMSPK: Power Management for Speaker-Amp
0: Power OFF (default)
1: Power ON
When PMSPK bit is "0", SPP pin and SPN pin becomes Hi-Z.

PMMSP: Power Management for Mixing & Selector Circuit of Speaker-Amp
0: Power OFF (default)
1: Power ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management 2	0	0	0	0	0	PMV3	PMV2	PMV1
R/W		RD	RD	RD	RD	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMV1: Power Management for Input Volume #1
0: Power OFF (default)
1: Power ON

PMV2: Power Management for Input Volume #2
0: Power OFF (default)
1: Power ON

PMV3: Power Management for Input Volume #3
0: Power OFF (default)
1: Power ON

All blocks can be powered-down by setting the PDN pin to "L" regardless of register values setup. In this case, all control register values are initilized.

When all power management bits are "0" in the 00H, 01H and 02H addresses, all blocks are powered-down. The register values will remain unchanged. Power supply current is 18uA (typ) in this case. For fully shut down, The PDN pin should be "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 0	THDET	0	0	BYPE	0	SD3	SD2	SD1
R/W		RD	RD	RD	R/W	RD	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

SD1: Input mode setting of LIN1/IN1- and RIN1/IN1+ pins
0: Single-ended Mode (default)
1: Differential Mode

SD2: Input mode setting of LIN2/IN2- and RIN2/IN2+ pins
0: Single-ended Mode (default)
1: Differential Mode

SD3: Input mode setting of LIN3/IN3- and RIN3/IN3+ pins
0: Single-ended Mode (default)
1: Differential Mode

BYPE: Bypass Mode Enable
0: Disable (default)
1: Enable
When BYPE bit is changeed from "0" to "1" at PMSPK bit = "1", the AK4213 changes to Bypass mode after the speaker amp is powered-down. When BYPE bit is changed from "1" to "0", SPK-Amp starts operating according to the setting of PMSPK bit after exiting Bypass mode.

THDET: Thermal Shutdown Detection
0: Normal Operation (default)
1: Thermal Shutdown status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch Headphone Mixer	0	0	HPLR3	HPLL3	HPLR2	HPLL2	HPLR1	HPLL1
05H	Rch Headphone Mixer	0	0	HPRR3	HPRL3	HPRR2	HPRL2	HPRR1	HPRL1
06H	Speaker Mixer	0	0	SPKR3	SPKL3	SPKR2	SPKL2	SPKR1	SPKL1
07H	Reserved	0	0	0	0	0	0	0	0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

Input Mixers: (Figure 7)
0: OFF (default)
1: ON

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Input Volume #1	R1V3	R1V2	R1V1	R1V0	L1V3	L1V2	L1V1	L1V0
09H	Input Volume #2	R2V3	R2V2	R2V1	R2V0	L2V3	L2V2	L2V1	L2V0
0AH	Input Volume #3	R3V3	R3V2	R3V1	R3V0	L3V3	L3V2	L3V1	L3V0
0BH	Reserved	0	0	0	0	0	0	0	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	1	0	1	0	1	0

Input Volumes: Default: 0dB (Table 1)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0CH	Mode Control 1	0	0	MOFF	0	PTS1	PTS0	0	0
	R/W	RD	RD	R/W	RD	R/W	R/W	RD	RD
	Default	0	0	0	0	0	0	0	0

PTS1-0: Headphone-Amp Mute ON/OFF Transition Time
Default: "00", typ. 16.4ms (Table 16)

MOFF0: Soft transition for changing HPMTN bit
0: Enable (default)
1: Disable

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0DH	Headphone PGA Control	0	HPZ	HPMTN	HPGA4	HPGA3	HPGA2	HPGA1	HPGA0
	R/W	RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	1

HPGA4-0: Headphone-Amp Volume Setting
Default: 19H; 0dB (Table 13)

HPMTN: Headphone-Amp Mute
0: Mute (default)
1: Normal Output

HPZ: Headphone-Amp Pull-down Control
0: Ground Mode (default)
HPL/HPR pins are shorted to VSS3.
1: Hi-Z Mode
HPL/HPR pins are pulled-down by 25kΩ(typ) to VSS3.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0EH	Speaker PGA Control	0	0	SPGA5	SPGA4	SPGA3	SPGA2	SPGA1	SPGA0
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	0	1	1	0	0	0

SPGA5-0: Speaker-Amp Volume Setting
Default: 18H; 0dB (Table 12)

When PMSPK bit is set to "0", reading and writing of SPGA5-0 bits are inhibited. When changing from PMSPK bit = "0" to PMSPK bit = "1", SPGA volume becomes default value (0dB) regardless of the setting of SPGA5-0 bits.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0FH	ALC Mode Control 1	0	0	REF5	REF4	REF3	REF2	REF1	REF0
	R/W	RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
	Default	0	0	1	1	1	1	0	0

REF5-0: Reference value at ALC Recovery Operation
Default: 3CH; +18dB (Table 10)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
10H	ALC Mode Control 2	0	0	0	ZTM1	ZTM0	WTM2	WTM1	WTM0
R/W		RD	RD	RD	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	1	0	1

WTM2-0: ALC Recovery Waiting Period
Default: "101", 524.8ms (typ.) (Table 8)

ZTM1-0: ALC Zero Crossing Timeout Period
Default: "01", 32.8ms (typ.) (Table 7)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
11H	ALC Mode Control 3	0	ALC	ZELMN	LMAT1	LMAT0	RGAIN1	RGAIN0	LMTH
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

LMTH: ALC Limiter Detection Level / Recovery Wainting Counter Reset Level
Default: "0" (Table 5)

RGAIN1-0: ALC Recovery GAIN Step
Default: "00"; 1 step (Table 9)

LMAT1-0: ALC Limiter ATT Step
Default: "00"; 1 step (Table 6)

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
0: Enable (default)
1: Disable

ALC: ALC Enable
0: ALC Disable (default)
1: ALC Enable
When ALC bit is set to "1", the ALC operation is enabled. The initial value is "0" (Disable).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
12H	TEST	0	0	0	0	0	0	0	0
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

Write "0" into the "0" registers.

SYSTEM DESIGN

Figure 29 shows the system connection diagram for the AK4213. The evaluation board [AKD4213] demonstrates the optimum layout, power supply arrangement and measurement results.

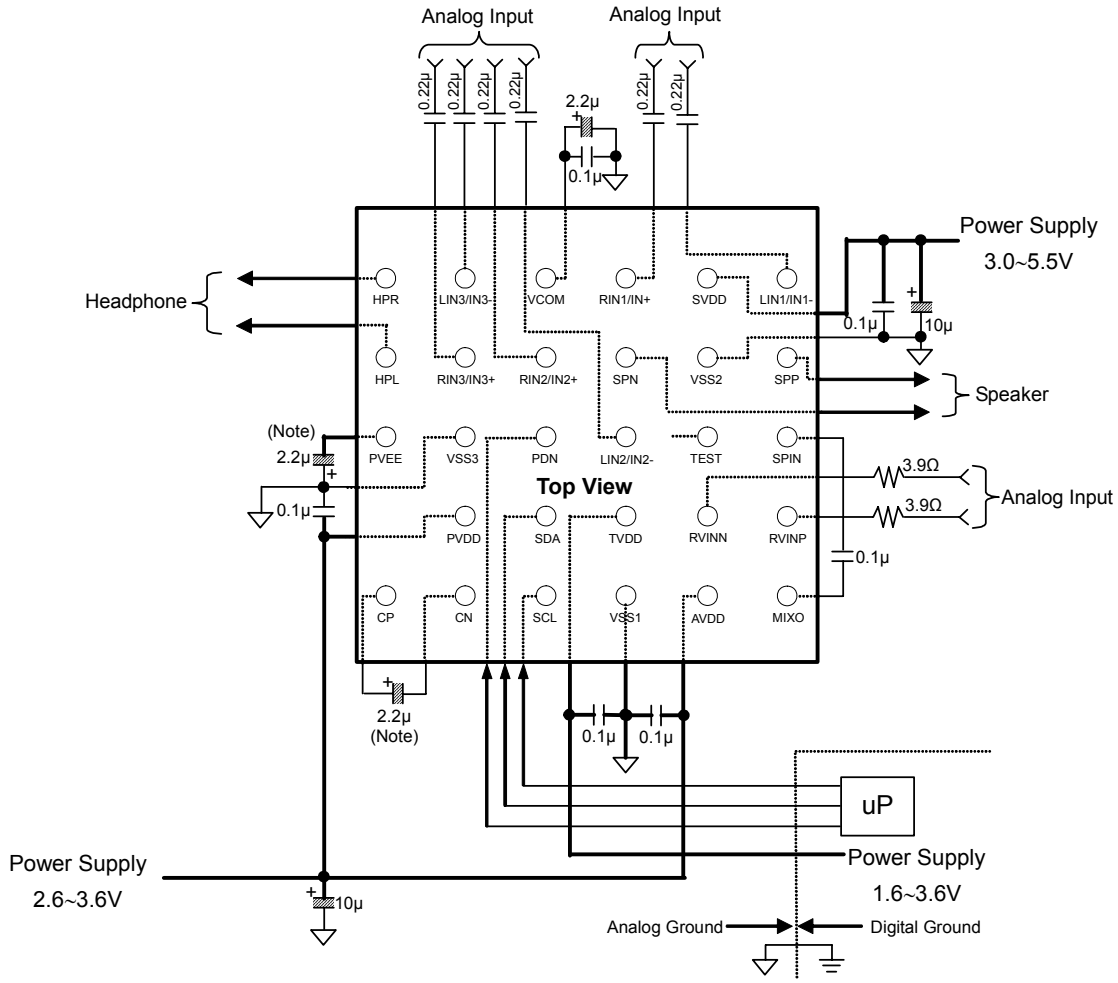


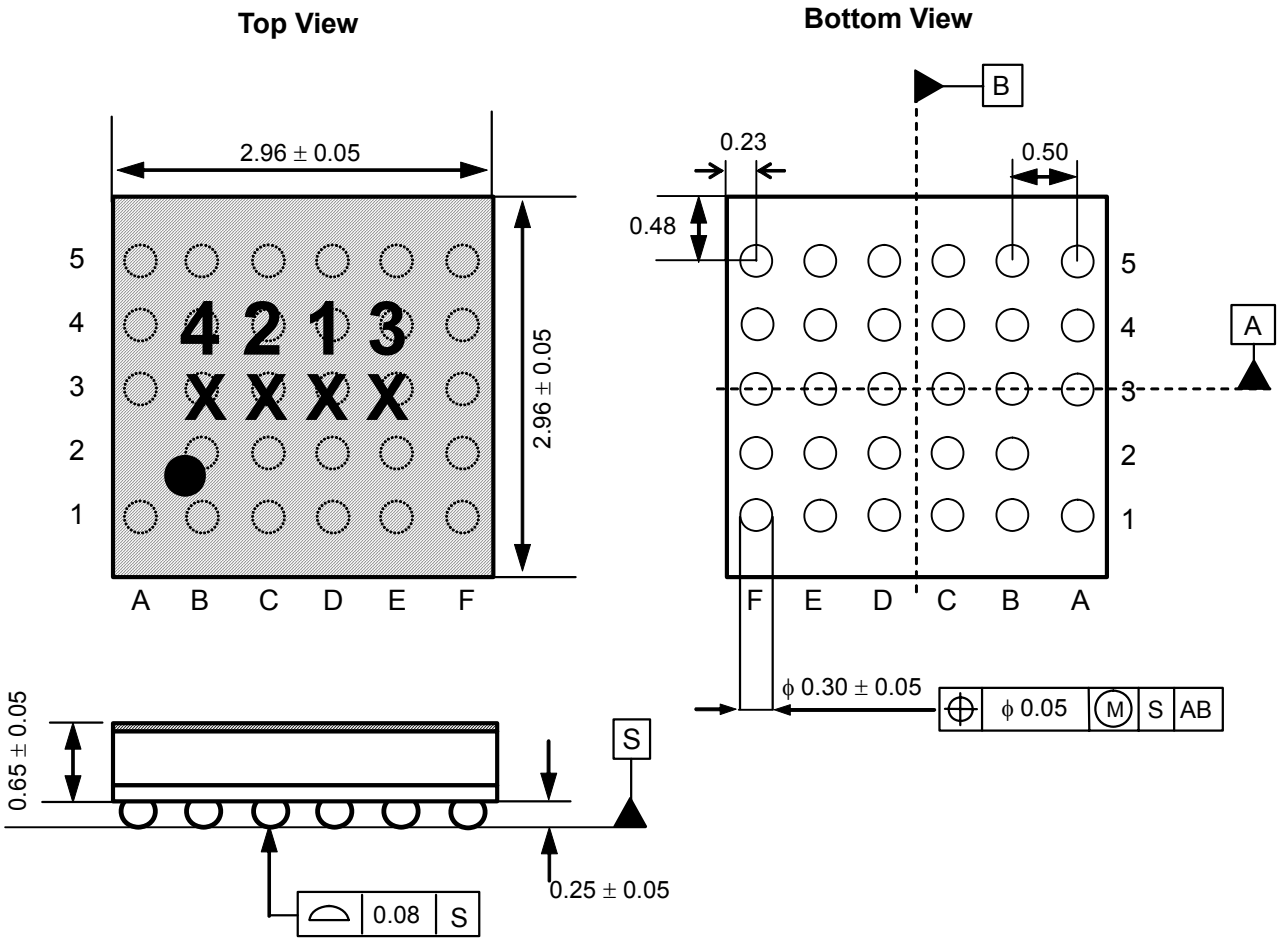
Figure 29. Typical Connection Diagram

Notes:

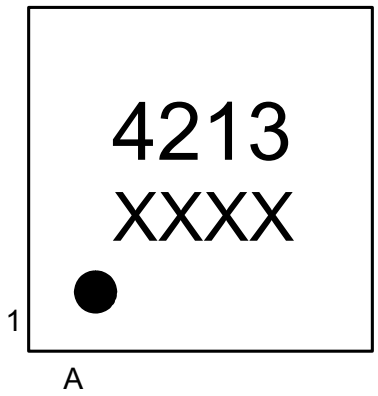
- These capacitors should use low ESR(Equivalent Series Resistance) over all temperature range. When these capacitors are polarized, the positive side should be connected CP pin or analog ground.
- VSS1, VSS2, and VSS3 should be connected to same analog ground plane.
- A 2.2µF electrolytic capacitor in parallel with a 0.1µF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be taken from the VCOM pin.
- AC coupling capacitor of 0.22µF should be connected to LIN/RIN pins to reduce pop noise at the power-up of the input volume block.

PACKAGE

29pin CSP (3.0mm x 3.0mm, 0.5mm pitch, BGA)



MARKING



XXXX: Date code (4 digit)
Pin #A1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/05/19	00	First Edition		
08/07/09	01	Spec Change	3	■ Ordering Guide AK4213EC → AK4213ECB
			32	■ Register Definitions 01H, GDDLY bit was deleted.
			37	PACKAGE Package plan was changed. Black type.